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The list of papers in which the author has been involved and that are related to the chapters in this book:

Journal Publications

- J1. Davide Bertozzi, Antoine Jalabert, Srinivasan Murali, Rutuparna Tamhankar, Stergios Stergiou, Luca Benini, Giovanni De Micheli, "NoC synthesis flow for customized domain spe-

- cific multiprocessor systems-on-chip”, IEEE Transactions on Parallel and Distributed Systems, Vol. 16, No. 2, pp. 113–129, Feb. 2005.
- J2. Srinivasan Murali, Theocharis Theocharides, Luca Benini, Giovanni De Micheli, N. Vijaykrishan, Mary Jane Irwin, “Analysis of error recovery schemes for networks on chips”, IEEE D&T, Vol. 22, No. 5, pp. 434–442, Sep./Oct. 2005.
- J3. Rutuparna Tamhankar, Srinivasan Murali, Stergios Stergiou, Antonio Pullini, Federico Angiolini, Luca Benini, and Giovanni De Micheli, “Timing error tolerant network-on-chip design methodology,” IEEE Transactions on Computer Aided Design, Vol. 26, No. 7, pp. 1297–1310, July 2007.
- J4. Srinivasan Murali, Paolo Meloni, David Atienza, Salvatore Carta, Luca Benini, Giovanni De Micheli, Luigi Raffo, “Synthesis of predictable networks-on-chip based interconnect architectures for chip multi-processors,” IEEE Transactions on VLSI, Vol. 15, No. 8, pp. 869–880, August 2007.
- J5. Srinivasan Murali, Luca Benini, Giovanni De Micheli, “An application-specific design methodology for on-chip crossbar generation,” IEEE Transactions on Computer Aided Design, Vol. 26, No. 7, pp. 1283–1296, July 2007.
- J6. Srinivasan Murali, David Atienza, Luca Benini, and Giovanni De Micheli, “A method for routing packets across multiple paths in nocs with in-order delivery and fault-tolerance guarantees,” VLSI-Design Journal, Hindawi Publications, 2007.

Conference Publications

- C1. Antoine Jalabert, Srinivasan Murali, Luca Benini, Giovanni De Micheli, “xpipesCompiler: a tool for instantiating application specific networks on chip”, Proc. DATE 2004.
- C2. Srinivasan Murali, Giovanni De Micheli, “Bandwidth constrained mapping of cores onto networks on chips”, Proc. DATE 2004.
- C3. Srinivasan Murali, Giovanni De Micheli, “SUNMAP: a tool for automatic topology selection and generation for NoCs”, Proc. DAC 2004.
- C4. Srinivasan Murali, Luca Benini, Giovanni De Micheli, “Mapping and physical planning of networks on chip architectures with quality-of-service guarantees”, Proc. ASPDAC 2005.
- C5. Rutuparna Tamhankar, Srinivasan Murali, Giovanni De Micheli, “Performance driven reliable link design for networks on chips”, Proc. ASPDAC 2005.
- C6. Srinivasan Murali, Giovanni De Micheli, “An application specific design methodology for sbus crossbar generation”, Proc. DATE 2005.
- C7. Srinivasan Murali, Martijn Coenen, Andrei Radulescu, Kees Goossens, Giovanni De Micheli, “Mapping and configuration methods for multi-use-case networks on chips”, ASP-DAC 2006.
- C8. Srinivasan Murali, Martijn Coenen, Andrei Radulescu, Kees Goossens, Giovanni De Micheli, “A methodology for mapping multiple use-cases onto networks on chips”, DATE 2006.
- C9. Srinivasan Murali, David Atienza, Luca Benini, Giovanni De Micheli, “A multi-path routing strategy with guaranteed in-order packet delivery and fault tolerance for networks on chips”, DAC 2006.
- C10. Srinivasan Murali, Paolo Meloni, Federico Angiolini, David Atienza, Salvatore Carta, Luca Benini, Giovanni De Micheli, Luigi Raffo, “Designing message-dependent deadlock free networks on chips for application-specific systems on chips”, VLSI-SoC 2006.
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