

Index

Note: Page numbers followed by 'f' and 't' refer to figures and tables respectively.

A

Accelerator surface diffusion, 241
Acetylacetonate, 171
Acid-bath chemistry, 177
Adherent surface coating, 73
Adhesion promoter, 270, 316
Adsorption, 148
Agglomeration of polycrystalline NiSi layer, 126
Air bridge Cu interconnects, 153–154
 methods of simulation
 calculation of effective elastic modulus, B, 157
 electrical simulation, 156
 model structure, 154
 results and discussion, 160
 stress simulation, 157
 volume-averaged stresses, 162
Air-gap formation method, 149f
Al/Cu wiring, comparison, 278f
ALD, *see* Atomic layer deposition (ALD)
ALD TaN, step coverage of, 215f
Alloy, selection rules of, 140f
Al-negative patterning *vs.* single damascene-positive patterning, 9f
Amyloid nano-fibrils, self assembly
 aromatic dipeptide nanotubes, identification, 533–534
 formation of nanostructures, 533f
 aromatic homo-dipeptides, modified types, 535–536
 nano-spheres formation, aromatic dipeptides, 535
 peptide building blocks, technological advantages of, 536
 peptide tubes, technological applications, 534–535
 coaxial nanocables formation, 534f

 role of aromatic residues, 531–532
Anode blanks, pilot plant production, 77f
Anti-reflective layer (ARL), 281
Area routers, 43
Atomic layer deposition (ALD), 32, 107, 169, 178, 198–199, 264, 277
 application in high aspect ratio structures, 214f
 behaviors, 213f
 characteristics of, 209f
 cycle, steps of, 208f
 ULSI manufacturing, 207–218, 217–218
 ALD cycle, 207
 ALD process window, 208
 applications, 210
 PLC, 218
Autocatalytic ELD, 222
Axial stress difference, 162

B

Back-end-of-line (BEOL), 82, 275
 ALD TaN grown on SiO₂, 215f
 applications, 214–217
 ALD ruthenium adhesion layer, 216
 dual-damascene metallization, 215
 pentakis-(dimethylamido)tantalum (PDMAT), 214
 Cu wiring, 291
 low-cost processing, 291
 low-*k* integration, 291
 low-*k* materials, 277–278
 metallization issue, 278
 SiV failure mode, 279f
65 nm/45 nm technology node, 284
 controllability, 285
 cross section SEM of 65nm node, 285f
 EB curing process, application, 285–290
 integration issues, 284–285

- Back-end-of-line (*cont.*)
 90 nm technology node, 279–280
 patterned low-*k* films, characterization,
 293–294
 robust process development, 291–293
- Back End Process (BEP), 145
- Back grind, 148
- Barrier layer, 5, 259
- Barrier self-formation/sputtered Cu alloy films,
 138 *f*
- Bath components controlling and monitoring
 tools, 435
 analysis of chemical constituents, 436
 model-based closed-loop chemical
 control system, 443 *f*
 open-loop replenishment system, 442 *f*
 replenishment and system designs,
 442–443
 titration, 436–437
 X-ray fluorescence, 437
- chemical management process,
 automation, 435
- electroanalytical techniques, 437
 chronoamperometry, 439
 CPVS, 437–438
 CVS, 437–438
 ion-specific electrodes, 440
 liquid chromatography, 440–441
 mass spectrometry, 441
 ORP electrodes, 440
 overview of, 441–442
 photometric techniques, 440
 pH probe, 440
 pulsed cyclic galvanostatic analysis
 (PGCA), 439
 spectrophotometric techniques, 440
- electrolyte components, classification,
 435–436
- Bath constituents used for ELD, 227 *t*
- BEM, *see* Boundary element
 method (BEM)
- Benzocyclobutene (BCB), 84, 278
- BEOL, *see* Back-end-of-line (BEOL)
- BEP, *see* Back end process (BEP)
- Bias thermal stress (BTS), 95
- Bio-inspired biological nano-assemblies, 531
- Biological and related templates of ELD,
 227 *t*–228 *t*
- Bonding process, 85
- Boundary element method (BEM), 240
- Boundary value problem (BVP), 242
- Brightening mechanism, 241
- BTS, *see* Bias thermal stress (BTS)
- Bumping, 148
- “Buried oxide,” *see* Insulating silicon dioxide
- Butler–Volmer equation, 224, 240
- C**
- CAD, *see* Computer-aided design (CAD)
- Capacitance–voltage curves, 113 *f*
- Capping layer, 148
- Carbon-doped silicon oxide (SiOC), 266
- Catalyst deactivating leveler, 241
- CD, *see* Critical dimension (CD)
- CEAC, *see* Curvature-enhanced accelerator
 coverage (CEAC) mechanism
- Chemical mechanical polishing (CMP), 9, 64,
 84, 148, 183–186, 259, 343, 344 *f*
 application of Cu-CMP, 345–347
 dishing and erosion problems, 347 *f*
 five layers MPU, 346 *f*
 planarization performances defined,
 347 *f*
 tool, 346 *f*
 categorization, PVT dependence, 349–350
 conventional, 259
- Cu processing, 257, 343
- dissolution law, chemical etching (CE), 355
 principle of etching polishing, 355 *f*
 removal rate, 354, 355
- polish principles and performances, 348
- principles, 373 *f*
 planarization diagram, 356 *f*
 planarization technologies, types,
 351–352, 352 *f*; 355–356
 polishing, 352 *f*
 slurry requirements, 348–349
 PVT dependence, 349 *f*
 subsystems, 345, 345 *f*
 surface cleaning, 350, 350 *f*
- Chemical-selective etching, 125
- Chemical vapor deposition (CVD), 6, 17, 32,
 145, 169, 185–186, 198, 241, 264,
 277
 types, 145
- Chip-scale package (CSP), 80
- CMOS, *see* Complementary metal oxide
 semiconductor (silicon) (CMOS)
- CMP, *see* Chemical mechanical polishing
 (CMP)
- Co alloy capping process/systems
 crystalline/amorphous dependence,
 449–450
 deposition chemistry, 450–451
- Co alloy capping tools, 445
 application, 446–447

- Black's law, 447
- EM improvement results, 447*t*
- copper damascene process, 445
 - electromigration (EM) void, 445*f*, 446*f*
 - properties and requirements, film
 - crystalline/amorphous dependence, 449
 - sample, 448*t*
 - TDDB, 448
- Coefficient of thermal expansion (CTE), 153
- Cold-pressing technology, 78
- Complementary metal oxide semiconductor (silicon) (CMOS), 3, 47
 - n-MOS and p-MOS transistors, 15
 - trends in miniaturization
 - Moore's law, 23–25
 - roadmaps, 25–27
 - scaling and power dissipation, 29–32
 - scaling theory, 27–29
- Computer-aided design (CAD), 42
- Conductor, ULSI ICs, 5
- Copper damascene module issues, 276*f*
- Copper dual damascene technology, 359
 - nitric acid (HNO₃)-base, 364–367
 - addition of citric acid, 365
 - advantages in HNO₃-BTA slurry, 365
 - effect of BTA, 367*f*
 - evaluation of anodic current transient measurement, 367*f*
 - optimum BTA, concentration, 364
 - potentiodynamic curves of copper, 366*f*
 - peroxide-base, 368–372
 - anodic current peak range, 370*f*
 - anodic potentiodynamic curves, 372*f*
 - effect of BTA, 371*f*
 - etching rate of copper, 368–369
 - utilization of H₂O₂, 368
- Copper electrodeposition, 67–68
- Copper interconnects, electrochemical
 - processing tools, 389
 - damascene capping, electroless processes, 393–394
 - dual damascene process, 389–390
 - electropolishing for planarization, 392–393
 - methods for improving copper electromigration, 394
 - novel processing methods (node and beyond), 391–392
 - PECVD Si(C) N cap technology, 393
 - processing methods, (node and beyond), 391–392
 - PVD-sputtered Ta(N) liner, 393
 - redundant ruthenium (Ru) liner approach, 394
 - tooling requirements, 390–391
- Copper metallization/motivation, 93–94
- Copper post-CMP cleaning, 257
- Copper-to-copper via-first cross section, 85*f*
- Copper wiring, formation, 149
- Core computation engine, 156
- Co-rich phase silicide, 125
- Courant–Freidricks–Levy number (cflNumber), 251
- Critical dimension (CD), 260, 265, 282
- CSP, *see* Chip-scale package (CSP)
- CTE, *see* Coefficient of thermal expansion (CTE)
- C54-TiSi₂/CoSi₂/NiSi, properties, 124*t*
- Cu damascene interconnects
 - hard masks (HM) process, 305–308
 - alignment shift between upper lines (M2) and vias, 306*f*
 - double-layered/triple-layered HM, 305*f*
 - leakage currents between adjacent lines, 308*f*
 - SEM micrographs, shouldering of LTS and LER, 307*f*
 - sidewall protection layer formation, 307*f*
 - limitations of multi-hard mask (MHM) processes, 308
 - lithography process
 - pure organic/inorganic ILD film, 301*f*
 - SEM micrographs, 300*f*
 - technical trends, 300*f*
 - photoresist (PR) mask, 302–305
 - cross-sectional SEM micrographs, 303*f*
 - Mises stress distributions and electrical properties, 304*f*
 - via-first process for inorganic low-*k* ILD films, 302*f*
 - via-first process with RM, formation mechanism, 304*f*
 - via poisoning, 303*f*
- Cu dual damascene process, 9
 - vs. Al lithography, 10
- Cu metallization/difficulties of implementing, 94–98
 - copper adhesion to dielectric, 96
 - copper diffusion/degradation of dielectric, 95–96
 - copper diffusion/reaction with Si, 96–98
 - copper passivation, 96

- Cu metallization (*cont.*)
 diffusion barrier and capping (or cladding) layer, 94
 processing, 98
- Cu metallization/diffusion barriers/evaluation of, 107–114
 analytical techniques
 SIMS, detection limits of, 108
 electrical devices/evaluation of diffusion barriers, 109–111
 metal-oxide-semiconductor (MOS) capacitor, 111
 reverse-biased Schottky diodes, 110
 reverse-biased shallow p–n junctions, 109
 Schottky diodes, 110
 equilibrium C–V curve, 113
 flat-band voltage of equilibrium capacitance–voltage, 112
 hybrid organosiloxane polymer, 108
 microscopic-based techniques, 108
 plasma enhanced CVD (PECVD), 112
 quasi-static C–V measurements, 114
- Current–voltage plots of Cu/TiN/p–Si, 111 *f*
- Curvature-enhanced accelerator coverage (CEAC) mechanism, 241, 242, 244
- Cu thin films/grain growth mechanism, 135–139
 nano-scale self-formation/Ti diffusion barrier layers/Cu(Ti) alloy films, 138–140
 annealing and low film resistivity/Cu(Ti) alloy films, 140
 melting point reduction, 140
 Rutherford backscattering spectrometry, 139
 sputter-deposition techniques, 138
 TEM-EDS elemental mapping image, 139
 strain energy criterion model, 135
 TEM experiment, 137
- CVD, *see* Chemical vapor deposition (CVD)
- Cyclic pulsed voltammetric stripping (CPVS), 437–438
- Cyclic voltammetric stripping (CVS), 437
- D**
- Damascene, 269
 capping, electroless processes, 393–394
 damage-free process, 269
 low-k integration challenges, 266
 plating, 64
 process, 8, 259, 263
 technique, 257, 259
- Dc plating, 66
- Delaminated area of Cu film, 269 *f*
- Density of state (DOS), 293
- Deposition chemistry, 452–455
 brush clean chambers, 455 *f*
 chambers, 455 *f*
 cleaning and activation chambers, 454 *f*
 functions of chemicals, 451
 UV–Vis spectroscopic measurement, 453 *f*
- Deposition process and tools, electrochemical, 397–408
 damascene copper electrodeposition, 403–407
 component separation of plating chemistry, 403–405
 current density profile, 404 *f*
 potential field distribution technique, 402–403, 403 *f*
 rinsing procedure, wafer, 404–405
 electro chemical processes, types of, 400–401
 electrografting, 406–407
 electrophoretic deposition, 407–408
 processing chamber of wafer, 399–400
 chamber configuration of ECMD, 399
 properties of fountain reactor, 399
 safety guidelines, electro chemical processes, 400
 semiconductor and microelectronic processes, 405–406
 through-mask electrodeposition, 405–406
 conductive base layer stack, 406–407
 general class of ECD processes, 405 *f*
 using photoresist, 406
 tool configuration, 400
 safety guidelines, 400
 safety of tool design, 400
 wafer handling automation, 397–398
 wafer processing equipment, 397
- DG-FET, *see* FinFET
- Dielectric constant (k_{eff}), 265, 269, 275
 effective, 161 *f*
 extraction of effective, 157 *f*
 for single-via level model structure, 161 *f*
 trends, 276 *f*
- Dielectric films, 264
- Die-on-wafer, 81
 3D integration, 81 *f*
- Diffusion barriers, 98–107
 amorphous barriers, 104
 deposition methods, 106–107
 passive metallic thin films, 99–101

- diffusion kinetics, 99
 - failure time of barrier, 99
 - high segregation factor, 99
 - significant Cu diffusion, 101
 - sacrificial barriers, 103–104
 - self-assembled molecular layers, 105–106
 - ionized metal plasma (IMP), 107
 - PVD TaN film, 107
 - self-assembled molecular (SAM), 105
 - synchrotron X-ray diffraction analysis, 107
 - vapor or wet-chemical methods, 106
 - self-forming barriers, 104
 - single crystalline barriers, 104
 - “stuffed” barriers
 - tantalum films/high-vacuum (HV), ultra-high-vacuum (UHV), 103
 - TiN, diffusion barrier for Al metallization, 103
 - TiN/Al/TiN for Cu metallization/multi-layered diffusion barrier of, 102
 - “thermal budget,” 99
 - thermodynamically stable barriers, 101–102
 - TaN, by PVD and CVD, 101
 - Diffusion driven theory of leveling, 239
 - 3D integration, ULSI interconnects, 79
 - BEOL-based wafer-level, 84
 - types, 80
 - Double-gate MOSFET, 36
 - Drain-induced barrier lowering (DIBL), 28
 - DRAM, *see* Dynamic random access memories (DRAM)
 - Drift-diffusion model, 20
 - 3D stacked imager circuit, 88
 - Dual damascene process, 9
 - barrier/etch-stop SiCN process, 283
 - cross second TEM images, 284*f*
 - modified edge liftoff test (m-ELT), 284
 - strength of adhesion, 284
 - plating, 65
 - SiO₂ capping, 282
 - photoresist poisoning process, 283*f*
 - SiOC/SiCN, impact, 283*f*
 - via-first patterning, 281
 - DD shape, comparison, 282*f*
 - Dynamic random access memories (DRAM), 5, 211
- E**
- EB curing process, application
 - Par/SiOC hybrid scheme, integration, 288
 - porous Par/SiOC, hybrid DD, 290*f*
 - SiV performance of 45 nm node, 289*f*
 - SiV test results, 289*f*
 - porous low-*k* MSQ evaluation, 286
 - EB curing time, function, 287*f*
 - EB total dose, function, 286*f*
 - FT-IR spectrum, 287*f*
 - interface fracture energy (G_c) vs. EB total dose, 288*f*
 - ECD, *see* Electrochemical deposition (ECD)
 - ECMD, *see* Electrochemical mechanical deposition (ECMD)
 - ECP, *see* Electrochemical polishing (ECP)
 - EDTA, *see* Ethylenediaminetetraacetic acid(EDTA)
 - EELS, *see* Electron energy loss spectroscopy (EELS)
 - Elastic modulus, 160
 - for multi-via level structures, 165*f*
 - ELD, tools and processes, 413
 - copper
 - chemistry of, 414–415
 - deposition process, 418–419
 - palladium and direct surface activation, usage of, 417–418
 - sensitization and surface activation, 417
 - substrate and self activation, 422
 - design criteria, 429
 - gap filling, 418
 - gold, 425
 - autocatalytic deposition, 426–428
 - cyanide base, 425–426
 - immersion deposition, 426
 - non-cyanide, 428–429
 - immersion reactors, 429
 - nickel
 - aluminum substrates and activation, 422–425
 - catalyzed deposition, 428
 - deposition process, overview of, 425
 - deposition and chemistry, 419–421
 - substrate activation, 421
 - Electrical chemical mechanical polisher (ECMP), 354
 - Electrical degradation, NiSi, 126
 - Electrical resistance of Al, 258
 - Electrical resistivity, 259
 - Electrical resistivity/nitrogen content of TaN_x films, 102*f*
 - Electrochemical deposition (ECD), 279
 - Electrochemical mechanical deposition (ECMD), 392

- Electrochemical polishing (ECP), 258
 Faraday's law, 353–354
 principle of, 353 *f*
- Electrochemical processes for ULSI
 Interconnects, 183
 copper plating chemistry, 186–198
 Bath composition, 189 *t*
 Bath composition for void-free filling, 186–187
 bis(3-sulfopropyl)disulfide (SPS), 188–189
 bottom-up, 186–187
 Cannizzaro reaction, 195–196
 cathodic cross-sectional SEM, 193
 cathodic polarization *f*, 192
 chemistry of copper plating bath, 188–189
 copper deposition mechanism and kinetics, 187–188
 copper electrodeposition for trench filling, 186
 copper electroless deposition for trench filling, 194–195
 electroless deposition reactions, 195–196
 formaldehyde (HCHO), 195–196
 Janus Green B (JGB), 188–189
 mechanism of electroless copper deposition, 195–196
 mechanism of void-free filling effect of additives, 193–194
 polyethylene glycol (PEG), 188–189, 196–198
 reaction mechanism: effect of additives, 189–192
 superfilling, 188–189
 superfilling by electroless copper deposition, 196–198
 dual damascene process, 184–186
 electrochemical process for seed layer formation, 198–201
 barrier layer formation/seedless copper filling, electroless deposition, 200–201
 electroless deposition for formation of seed layers, 198–199
 seedless copper electrodeposition on barrier materials, 199–200
 single damascene, 184–186
 single/dual damascene processes, 186
 subtractive etching process/damascene process, 184 *f*, 185
- Electrochemical process integration
 BEOL technology advanced, 257
 CMP, 257
 copper post-CMP cleaning, 257
 Cu metallization PVD barriers, 257
 damascene concept/process, 257
 electrochemical view of copper chemical mechanical polishing, 257
 lithography for Cu damascene fabrication, 257
 low-*k* dielectrics, 257
- Electrochemical view of copper CMP, 257, 359–377
 advantage characteristics of copper, 359
 ammonium hydroxide-base, 361–364
 anodic potentiodynamic curves, 362 *f*
 etching rate of copper, 362–363
 linear polarization of measurement (LPR), 361
 open circuit potential (OCP), 361
 oxidants additions, 361
 polarization curves, 362 *f*
 surface morphology, 363 *f*
- carbonate- and sorbate-base, 372–375
 addition of oxidizer, 373
 anodic polarization of, 375 *f*
 anodic potentiodynamic curves, 374 *f*
 effect of BTA, 373
 evaluation of anodic current transient measurement, 375 *f*
- Electrochemistry, 257
- Electrode/electrolyte interface, 241
- Electrodeposition, 63, 241
 advancement, 63–64
 advantages, 63
 application, 63–64
 changes in process conditions, 64
 copper electrodeposition, 67–68
 dc plating, 66
 mass transport conditions, 65–66
 patterned plating, scales of, 65
 potential distribution, 67
 pulse plating, 66
 pulse reverse plating, 67
 through-hole plating, 67
 types of electroplating in fabrication, 64
- Electroless deposition (ELD), 176
 autocatalytic, 222
 bath components, 227 *t*–228 *t*
 bath constituents used for, 227 *t*
 biological and related templates of, 227 *t*–228 *t*
 on nanoscale object, schematics of, 223 *f*
 structure type of, 227 *t*–228 *t*

- Electroless deposition (ELD)/molecular scale, 221
autocatalytic ELD of metals, 221
fundamentals, 223
Butler–Volmer equation, 224
nanoscale deposition, special of, 225
Nernst equilibrium, 223
steering macroscopic, 224
galvanic plating, contrast, 222
macroscopic, 226
biomolecules as templates, 229
confinement plating, 228
confinement plating in biomolecules, 231–232
sensitization, Pd and Pd/Sn colzoids, 226
nanoscale deposition, 222
scientific communities and, 221
Tollens reaction, 221
- Electrolytic plating/electroplating/plating, 63
see also Electrodeposition
- Electromigration (EM), 265, 281
- Electron beam (EB), 269, 285
- Electron energy loss spectroscopy (EELS), 293
- Electronic technology-based hierarchy, 4*f*
- Electron mean free path, 264
- Electrophoretic deposition (EPD), 73
electrophoresis and, 73–74
process limitations, 73–74
theoretical basis, 74
potential applications, 74–78
conducting lines, 75
embedded passive components, 75–77
fuel cell technology, 75
solid electrolyte capacitors, 77–78
- Electroplating, additives, 65
- Element removal and reactivation technique, 157
- Elmore delay, 48–50
- EM, *see* Electromigration (EM)
- Embedded process, 259
see also Damascene, technique
- “End of roadmap” technology, 176
- Energy-filtered (EF) images, 294
- Epitaxial alignment, NiSi, 127
- Epitaxial lateral overgrowth, 82
- Etching process, 156, 259, 260
- Ethylenediaminetetraacetic acid (EDTA), 195, 415
- Eulerian level set method (LSM), 241, 245, 246
- Eulerian techniques, 241
- F**
- Fabrication process, 269
- FEA, *see* Finite element analysis
- FEM, *see* Finite element method (FEM)
- FEOL, *see* Front-end-of-line (FEOL)
- FEOL/ITRS specifications, 211*t*
- Fick’s laws, 225
- FinFET, 36
structure and transistor, 37*f*
- Finite element analysis, 154, 157*f*
- Finite element method (FEM), 240
- Finite volume method (FVM), 241
- FiPy output, 251*f*
- Flat-band voltage of MOS capacitors, 113*f*
- Fluorine-doped silicon oxide (SiOF), 266, 277
- Fourier transformed infrared spectroscopy (FT-IR), 293
- Front-end-of-line (FEOL), 82
applications, 211–212
dynamic random access memories (DRAM), 211
equivalent oxide thickness (EOT), 211
gate dielectric leakage, 211
metal–insulator–metal (MIM) capacitors, 211–212
metal–insulator–silicon (MIS) capacitors, 212
metal organic precursors/hafnium amido compounds, 211
Moore’s law, 211
physical vapor deposition (PVD), 211
- FT-IR absorption spectra, 269
- “FUSI” (fully silicided gate), 32, 127
- FVM, *see* Finite volume method (FVM)
- G**
- Galvanic deposition, 224
see also “Sensitization”
- Galvanic electrodeposition, 222
- Gas evolution of adsorption material (degas), 148
- Gate delay, 21, 258
versus interconnect delay, 22–23, 23*f*
of logic inverter, 21*f*
- Ge atoms, segregation, 128
- Germanium and III–V channel devices, 35–36
- Graphite layer, 150
formation, 149
- Greenhouse issue, 257
- Grid2D object, 249
- H**
- HAR, *see* High aspect ratio (HAR)
- Heat conduction, 148

High aspect ratio (HAR), 83
 High-density interwafer, 87
 High gas/metal penetration, 284
 High moisture uptake, 284
 High temperature storage (HTS), 290
 HSQ, *see* Hydrogen silsesquioxane (HSQ)
 Hybrid dielectrics, 266
 Hydrogen-free reductants, 222
 Hydrogen silsesquioxane (HSQ), 277
 Hydrostatic stress, 158

I

ILD, *see* Interlayer dielectrics (ILD)
 IMP, *see* Ionized metal plasma (IMP)
 Incubation delay, 209
 "Induction period," 225
 "Input switching threshold," 21
 Insulating silicon dioxide, 34
 Insulator between wiring, change of, 145
 Insulator materials between wiring, change of, 146*t*
 Integrated circuit
 invention of, 3
 metallization, 94*f*
 Integrated metrology (IM), 479
 benefits of, 480
 closed loop control (CLC) process, 486–488
 benefits of, 488
 open-loop control using default polish time, 488*f*
 PID algorithms, 486–487
 real time adjustment, 486*f*
 using default polish time, 489*f*
 before using process control, standard deviation measurement, 489*f*
 criticisms of process equipment
 manufacturers (PEM), 480–481
 end-users *versus* IM implementation, 480
 evolution of, 481
 limitations of, 479–480
 copper CMP, 493
 major components, 484
 measurement accuracy
 film thickness, 482–483
 optical model, 483
 return on investment, qualitative view
 capital investment, 490
 consideration factors, 490–492
 cost saving attributes, 491
 manufacturing advantages, 491–492
 reduction of labor, 490
 before using process control, standard deviation measurement, 489–490

software applications, 494
 technology, 481–486
 dry factory interface, 485*f*
 latest generation IM tool specification, 486*t*
 pre-metal dielectric (PMD) process, 493
 refraction index, Spectrophotometer, 482*f*
 shallow trench isolation, 492–493
 typical optical scheme, spectral reflectometer, 484*f*
 Wet NovaScan 210, 485*f*
 tools installation, 481
 Interconnects
 (dimensions of 32 nm), challenges, 4
 performance issues, 7–8
 process issues, 8–11
 reducing resistance, 7
 Interconnects in ULSI systems
 circuit models of interconnect, 45–52
 area capacitance, 46–47
 capacitive interconnect, 46–47
 cross-capacitance, 46–47
 electromagnetic wave propagation, 50–52
 ideal interconnect, 45
 inductive interconnect, 50–52
 interconnect model types (from top to bottom), 46*f*
 lumped/distributed RC stage, 48*f*
 parallel-plate capacitor expressions, 46–47
 RC tree, 50
 resistive interconnect, 48–50
 design approaches/techniques for interconnect problems, 55–58
 circuit architecture, 58
 layout optimization techniques, 57–58
 metallization stack design, 55
 interconnect metrics, 43–45
 delay, 43–45
 power, 43–45
 reliability, 43–45
 signal integrity, 43–45
 interconnect scaling problem, 52–55
 effective metal resistivity, 54
 on-chip interconnect requirements, 39–43
 blocks, 39–40
 channel routers, 43
 configurable interconnect, 40
 cross section of metallization stack, 42*f*

- floorplan, 40*f*
 - global wires, highest levels, 40
 - local wires, low-level blocks, 40
 - Rent's rule, 41
 - routing tree, 43*f*
 - signal sinks, 43
 - signal source, 43
- power supply interconnect, 58–59
- Interconnect structures, fabrication, 153
- Interface delta function, 247
- Interface engineering targeting, 285
- Interface fracture energy (G_c), 288*f*
- Interface topology, 241
- Interfacial fracture, 165
- Interlayer dielectrics (ILD), 93, 285
- International technology roadmap for semiconductor (ITRS), 25, 121–122, 145, 211, 216
 - challenges for interconnects, 4
 - near-term technology trend targets of, 26
- Intrinsic gate delay, 21–22
- Intrinsic leakage current, 125
- Ion-enhanced ash, 271
- Ionized metal plasma (IMP), 107
- Isolation layer, formation, 150
- ITRS, *see* International Technology Roadmap for Semiconductor (ITRS)

- J**
- Joule's heating (Q), 258
- Junction leakage, 125

- K**
- K_{eff} with respect to air gap, 160, 161*f*
- KGD, *see* Known-good-die (KGD)
- Kinetic regime of diffusion in polycrystalline materials, 100*f*
- KKA, *see* Kramers–Kronig analysis (KKA)
- Known-good-die (KGD), 81
- Kramers–Kronig analysis (KKA), 294

- L**
- Lagrangian approach, two-dimensional, 241
- Langmuir adsorption, 244
- Langmuir kinetics, 170, 173, 178
- Laplace equation, 240
- Large-Grained Cu Interconnects, 133–135
 - Cu thin films/abnormal grain growth, 133–135
 - bimodal grain growth, 133
 - FIB techniques, 135
- Large-scale integration (LSI), 3, 257
- Leakage current/function of time/copper on thermal oxide, 112*f*
- LER, *see* Line-edge-roughness (LER)
- Leveling theory, 239, 240
- Lewis base, 172
- Linear interpolation, 244
- Line-edge-roughness (LER), 260
- Lithography
 - for Cu damascene fabrication, 257
 - misalignment, 281
- Low- k dielectric film, 257
 - basic properties, 327–330
 - cracking and delamination, 329*f*
 - effects of water adsorption, 330*f*
 - mechanical aspects, 328*f*
 - pore size distributions, 328*f*
 - CAP dielectrics, future trends, 337
 - deposition process, 325–327
 - analytical methods, 327*f*
 - technical issues and trends, 326–327, 326*f*
 - TEM micrographs of ULSI interconnect pitches, 326*f*
 - hardening and post-curing techniques, 330–332
 - EB/UV radiation and irradiation process, 331*f*
 - k -value vs. mechanical properties, 332*f*
 - innovation materials and process, 332–337
 - criteria for porous stability, 334
 - durability ratio, 335*f*
 - plasma co-polymerization technology, 334–336, 337*f*
 - technological trends, 334*f*
 - UV curing method, 335*f*
- Low- k materials, 7–8
 - for CVD, 147*t*
 - development, 145
 - change of insulator between wiring, 145
 - conditions for practical usage, 146
 - issues of porous low- k materials, 148
 - porous low- k material, 148
 - for SOG, 147*t*
 - variety, 277*f*
- Low mechanical strength, 284
- Low plasma resistance, 284
- LSI, *see* Large-scale integration (LSI)
- LSI implementation, 257

- M**
- Macroscopic ELD
 - biomolecules as templates, 229
 - “enhancement,” 229
 - “enzyme metallography,” 229

- Macroscopic (*cont.*)
 hydroquinone , standard reductant, 229
 confinement plating, 228
 popular substrates, 229
 confinement plating in biomolecules,
 231–232
 Ohmic behavior, 231
 Reches' silver, 231
 fundamentals, 224–225
 sensitization, Pd and Pd/Sn colzoids
 “self-sensitizing,” 226
- Material design engineering, 285
- Maze routers, 43
see also Area routers
- Mean free path (MFP), 278
- Mean time to failure (MTF), 283
- Mechanical friction, low-*k* film, 265
- Medium-scale integration (MSI), 3
- Melting point of Cu, 258
- MEMS, *see* Microelectromechanical systems (MEMS)
- Metallization patterning process, 68
see also Dual damascene process, plating
- Metallorganic condensation, 171
- Metallorganic thermal decomposition, 171
- Metal–metal bond formation, 225
- Metal-oxide-semiconductor field-effect transistor (MOSFET), 15, 16*f*, 121, 127
 characteristics, 19
 “long-channel characteristics,” 18
 novel devices, 36–37
 source–drain current, 18
- Metal-oxide-semiconductor (MOS) transistor, 93
- Metal penetration, 270
- Methyl silsesquioxane (MSQ), 277, 285
- Microelectromechanical systems (MEMS), 63, 87
- Microporous non-conductor, 73
- Micro-processing units (MPU), 258
- Middle-of-Line (MOL) applications, 212–214
 ALD W nucleation layers, 214
 chemical vapor deposition (CVD), 212
 tetrakis(dimethylamido)titanium (TDMAT), 212
- Mini-electron beam, 148
- “Mixed potential,” 223
- MnP-type structure (orthorhombic), 127
- Modified edge liftoff test (m-ELT), 28
- Modular assembly, 77
- Moletronics, nanoscale interconnects
 technology
 carbon nanotubes (CNTs)
 electronic structure, 514–515
 geometric structure, 514–515
 interconnect applications of CNTs, 516
 tube-tube junctions, 516–518
 mechanical properties of CNTs, 515
 thermal properties of CNTs, 515
 tube–metal contacts, 518–519
- “Moore’s clock,” 23, 25*f*
 pendulum, phases, 24
- Moore’s law, 23–25, 64
 scaling trend of DRAM cell area, 24*f*
- MOS capacitor model, charge density, 16
- MOS capacitors with CoPW diffusion barriers,
 114*f*
- MOS device and interconnects scaling physics
 current regimes, 18–19
 linear region, 17–18
 saturated region, 18
 subthreshold region, 19
- digital signal propagation
 gate delay, 21–22
 gate delay *versus* interconnect delay,
 22–23
 trends in CMOS miniaturization, 23–32
- mobility and carrier velocity, 20–21
- MOSFET transistor
 basic device physics, 15–17
 technology, 17
- new device structures and materials
 germanium and III–V channel devices,
 35–36
 novel MOSFET devices, 36–37
 silicon-on-insulator (SOI), 34
 strained silicon and SOI, 34–35
 strained-silicon MOSFET, 32–34
- MOSFET, *see* Metal-oxide-semiconductor field-effect transistor (MOSFET)
- MOS transistor, *see* Metal-oxide-semiconductor (MOS) transistor
- MPU, *See* micro-processing units (MPU)
- MSQ, *see* Methyl silsesquioxane (MSQ);
 Porous methylsilsesquioxane (MSQ)
- Multilayer photomask structure, 260
- Multilayer tape sandwich, 76
- Multi-via level air-bridge structure, for stress
 calculation, 159*t*
- Multi-via level model structures, 155*f*
- N**
- Nanoclustering method, 268
- Nanometer-level pores, 266

- Nanopowder, 78
- Nanoscale deposition, 225
- Nanoscale interconnect technology
- alternative molecular system
 - charge transport mechanisms, 519–520
 - self assembly techniques, 520–522
 - architectures, 507–508
 - die-to-die integration, 509–510
 - hyper-integration, 508–509
 - moletronics, 511
 - carbon nanotubes (CNTs), 512–514
 - silicon wafers with BCB
 - bonds.(infrared image), 512*f*
 - wafer-to-wafer integration, 510–511
- Nanoscale objects, 222
- “Nanotechnology,” 226
- National Technology Roadmap for
- Semiconductors, *see* International Technology Roadmap for Semiconductor (ITRS)
- Nernst equilibrium, 223
- NiAs-type structure (hexagonal), 127
- Non-aqueous dispersion media, 74
- Non-volatile memory (NVM), 82, 83
- N-type MOSFET, 15
- charge regimes of MOS capacitor in, 16*f*
- Nucleation mode, C54-phase, 124
- NVM, *see* Non-volatile memory (NVM)
- O**
- Ohmic metal/semiconductor contact, 122
- Oxidation–reduction potential (ORP), 436, 440
- Oxide-to-oxide bonding, 85
- P**
- PAALD, *see* Plasma-Assisted Atomic Layer Deposition (PAALD)
- Palladium (II) hexafluoroacetylacetonate, 170
- structure, 172*f*
- Parasitic capacitance, 263
- Patterned plating, scales of, 65
- PCB, *see* Printed circuit board (PCB)
- PECVD, *see* Plasma-enhanced CVD (PECVD)
- PFM, *see* Phase field method (PFM)
- Phase field method (PFM), 246
- Physical vapor deposition (PVD), 186, 277
- barriers, Cu metallization deposition
 - technique, 316–317
 - alternative methods, 317–318
 - self-formation, 317
 - sputter deposition, 316–317
 - diffusion barrier layer necessities, 311–312
 - driving force, types, 317–320
 - classification of metal, coefficient activity, 319*t*
 - Ellingham diagram, 318*f*
 - solute concentration , coefficient activity, 319*f*
 - metallurgical aspects, 312–316
 - bias thermal stressing (BTS) test, 314
 - conventional criteria, material selection, 312
 - diffusion barrier parameters, 313*t*
 - influence of contact angle, 315
 - influence of substrate surface condition, 316–317
 - resistivity and heat of formation of carbides, 315*t*
 - resistivity and heat of formation of nitrides, 314*t*
 - role of kinetics, 320
- Pixel-by-pixel processing, 87
- Planarization, advanced techniques, 459
- conventional methods (copper), 460–461
 - electrochemical polishing, 460
 - limitations, 459–460
 - mechanical depositions, 462–463
 - mechanism of ECMD, 463–469
 - mechanism of ECMP, 469–472
 - copper removal rate, 471*f*
 - planarization of a topographic copper layer, 470*f*
 - polarization curves of copper surface, 470*f*
 - novel methods (copper), 462
- Plan-view/cross-sectional SIM images/100-nm thick sputtered Cu, 135*f*
- Plan-view TEM images of 100-nm thick sputtered Cu films, 134*f*
- Plasma-assisted atomic layer deposition (PAALD), 217
- plasma-enhanced ALD (PEALD), 217
- Plasma-enhanced CVD (PECVD), 6, 266
- Plasma process, 279
- Plating and electroless plating, ALD seed layers, 169
- Cu on PA-ALD Pd, electroless deposition, 176–178
 - “end of roadmap” technology, 176
 - FE-SEM images, Cu film on TaNX, 177*f*
 - FE-SEM images, Cu on aspect ratio trench, 177*f*
 - robust native oxide, 176
 - metal ALD process, 170*f*
 - palladium on noble metal, 173–174

- Plating and electroless (*cont.*)
 hydrogen/argon purge, 173
 parasitic CVD, 173
 Pd ALD films, sequential growth, 174*f*
 palladium on tetrasulfide silane, 174–176
 higher fluorine level, 174
 lack of catalytic activity, 174
 lack of texture, 175
 quality of film, 174
 RHEED spectra, Pd ALD films, 175*f*
 thermal/plasma-enhanced ALD, 171–173
 Cu precursor thermal decomposition, 173*f*
 inert hydrogen, 172
 lack of conformality, 172
 remote plasma source, 172
- PLC, *see* Programmable logic controllers (PLC)
- P-MOS** transistors, 15
- Poisson's ratio, 288
- Polishing pad, 269
- Poly-arylene-ether (PAE), 278
- Polymer-to-polymer via-last schematic cross section, 86
- Pore-sealing technology, 270, 270*f*
- Porogen, 266
- Porous low-*k* materials, issues, 148
- Porous materials, 258
- Porous methylsilsequioxane (MSQ), 155, 266, 286
- Post-CMP cleaning, 379
 chemical defects, 380
 electro-chemical behavior of copper (acid), 383
 anodic potentiodynamic curves, 383*f*, 384*f*
 energy dispersive spectroscopy (EDS), 384
 etching in HNO₃ solution, 381, 382
 etching process, 382–383
 exposure in cleaning solutions
 SEM micrograph, 384*f*
 interlayer dielectric (ILD) surface, 379
 mechanical defects, 379–380
 particle contamination of wafer surface, 379
 process parameters, 380–382
 Triton B, 381
 using distilled water, 381
- Pre-bottom wafer singulation 3D integration, 80
- Pressure cooker test (PCT), 289
- Printed circuit board (PCB), 79
- Pristine elemental surface, 176
- Process optimization/improvement, 285
- Programmable logic controllers (PLC), 218
- Proposed model of air gap, 150*f*
- Prototype air-bridge structures, 153
- Prototype low-profile, high-performance capacitors, 77*f*
- Pseudo-one-dimensional leveling theory model, 240
- Pseudo-wafer 3D integration, 82*f*
- Pulsed cyclic galvanostatic analysis (PGCA), 437, 439
- Pulse plating, 66
- PVD, *see* Physical vapor deposition (PVD)
- Python programming language, 249
- R**
- Raman spectroscopy, 293
- RC delays, 7
 time, 93
- Reactant diffusion and partial reactions on nanoscale surface, 225*f*
- Reactive ion etching (RIE), 98, 183–186, 276
- Recrystallization of polycrystalline, 82
- “Red Brick Wall,” 275
- Reflection high energy electron diffraction (RHEED), 174
- Reliability parameters, interconnect, 265
- Residual stresses, 153
- Resist ash, 271
- Resistivity changes of 300-nm thick Cu, 139*f*
- Resistivity of Cu lines of various widths, effective, 216*f*
- RHEED, *see* Reflection high energy electron diffraction (RHEED)
- RIE, *see* Reactive ion etching (RIE)
- “Roadmap acceleration,” 25
- Robust process development, 291–293
 SiV stress test results, 292*f*
 surrounding pattern effect, mechanism, 292*f*
- S**
- SAM, *see* Self-assembled molecular (SAM)
- SBH, *see* Schottky barrier height (SBH)
- Scalar variable, 246
- Scaling and power dissipation, 29–32
 direct gate tunneling current density vs. effective oxide thickness, 30*f*
 guidelines for selecting alternative gate dielectric, 31
 overview of high-*k* dielectrics, 31*t*
- Scaling theory, 27–29
- Scanning TEM (STEM), 293
- Schottky barrier height (SBH), 122, 128

- Schottky diodes, 110
 reverse-biased, 110
- Scribing, 148
- “Sea of Kelvin,” 291
- Self-assembled molecular (SAM), 105
- “Self-limiting” behavior, 173
- “Self-sensitizing,” 226
- “Sensitization,” 222
 methods of ELD, 227*t*–228*t*
 of nonconductive surfaces, 222
- Shadowing effect, 259, 260
- Short-channel effects, 28
- Signal propagation, 258
- Silane-coupling treatment, 148
- Silicides, 5, 121
 bulk MPU/ASIC, in ITRS 2005, 123 *f*
 CoSi₂, 125
 contact resistivities, 123 *f*
 intermetallic compound, 121
 NiSi, 125–127
 low consumption of Si, 125
 low contact resistivity, 126
 low formation temperature, 125–126
 low resistivity, 125
 silicide formation in MOSFET, 122 *f*
 self-align silicide (salicide) process, 121
 SiGe incorporation, 127–128
 energy bandgap, controllability, 127
 heteroepitaxial growth of Si_{1-x}Ge_x, 127
 mono-germanosilicide phase, 128
 realizing higher doping concentrations, 127
 TiSi₂, 124–125
 ULSI application, 121
- Silicide/Si interface, 124
- Silicon-based integrated circuits (ICs), 3
- Silicon-on-insulator (SOI), 34
- Simple EPD cell *vs.* deposition on porous membrane, 74 *f*
- SIMS depth profile of Cu, 109 *f*
- Single-via level model structure, 154 *f*
- Sintering process, 73
- SiOC, *see* Carbon-doped silicon oxide (SiOC)
- SiOC/SiCN films, characteristics, 281*t*
- SiOF, *see* Fluorine-doped silicon oxide (SiOF)
- Si–O ring structures, 269
- SiP, *see* System in a package (SiP)
- SIV, *see* Stress-induced voiding (SiV)
- Small-angle x-ray scattering (SAXS)
 spectrum, 500–502, 502 *f*
- Small-scale integration (SSI), 3
- S-MAP, *see* Stacked mask process (S-MAP)
- SoC, *see* System-on-chip (SOC) device
- SOD, *see* Spin on dielectric (SOD)
- SOG, *see* Spin on glass (SOG)
- Solution domain and its boundary, 243 *f*
- Source/drain (S/D) contact, 121
- Spin on dielectric (SOD), 145, 266, 285
- Spin on glass (SOG), 145
- Spintronics, nanoscale interconnects
 technology, 522–524
 electroplating, 524–526
- Sputtering, 149, 259, 260
- Stacked mask process (S-MAP), 282
- Strained silicon and SOI, 33, 34–35
 straining silicon channel, 33
- Strained-silicon MOSFETs, 32–34
- Stress-induced voiding (SiV), 265, 279, 291
- Superconformal electrodeposition, modeling
 adsorption rate, 239
 Butler–Volmer equation, 240
 deposition rate, 239, 240
 Eulerian technique, 241
 FiPy, 239, 249–252
 governing equations, 242–245
 Langmuir adsorption, 244
 Laplace equation, 240
 level set equations, 245–246
 numerical discretization, 247–249
- Superfilling additives, 68
- Surfactants, 65
- Switching Net, 43–45
 interconnect power, 43–45
- System in a package (SiP), 79
 three-dimensional integration, 257
- System-on-chip (SOC) device, 257, 275
- T**
- Tafel equation, 240
- Tantalum, plasma clean, 171
- TCAD-Raphael, 156
- TDDB, *see* Time-dependent dielectric
 breakdown (TDDB)
- “Technology generation”, 93
- TEM, *see* Transmission electron microscopy
 (TEM)
- TEM/EELS measurements, 294 *f*
- Temperature cycle test (TCT), 289
- Temperature humidity bias (THB), 289
- Tetramethylheptanedionate (tmhd), 171
- Theoretical resistivities/MS model, 132 *f*
- Thermal loading, 153
- Thermal stability, 275
- Thermal stresses, 153
- Thermo-mechanical properties, 153, 164
- Three-dimensional non-volatile memory, 83 *f*

Through-hole plating, 67
 Time-dependent dielectric breakdown (TDDB), 265, 293
 Tobacco mosaic virions, 230*f*
 Tollens reaction, 221
 Tomography three-dimensional, 266
 “Top-down” manufacturing, 4
 Transfer-printing onto tape, 75
 Transistors, 28, 40, 211
 see also specific transistors
 Transmission electron microscopy (TEM), 293
 Trench air gap, 156
 TVS measurement of capacitor, 115*f*

U

ULSI, *see* Ultra large-scale integration (ULSI) technology
 ULSI metallization/materials/electrical properties, 131–141
 fabrication technique, 133
 high-speed ULSI devices/ 70-nm-wide Cu interconnects, 133
 Mayadas and Shatzkes (MS) model, 131
 RC delay, 131
 “self-formation of barrier layer,” 133
 theoretical resistivity, 132
 Ultra large-scale integration (ULSI) technology, 3–4, 121, 131, 183–186
 challenges, ICs, 3–5
 material issues in Cu interconnects, 5–6
 performance issues, 7–8
 process issues, 8–11
 copper metallization/diffusion barriers, 93–115
 materials used in manufacturing, interconnects, 6*t*
 classification, 5
 performance variables characterize, 7
 Ultra-low-power consumption, 257
 “Ultra-shallow junctions,” 17
 Ultrasonic vibration, 178
 Ultra violet (UV), 269, 285
 Unlimited stability, EPD, 74
 Unsintered Ag–Pd conduction line, 75*f*
 UV, *see* Ultra violet (UV)

V

Valence electron energy loss spectroscopy (V-EELS), 293

Valence ELS, 294*f*
 Very large-scale integration (VLSI), 3
 Void formation, 259
 Volume-averaged Cu in multi-via level structures
 trench, 164*f*
 trench + via air-gap structure, 164*f*
 trench + via r-gap structure, 164*f*
 Volume-averaged stresses
 effective elastic moduli, 165
 in single-via level structure
 Cu line stresses, 162*f*
 Cu via stresses, 162*f*
 stresses in multi-level structure, 163
 stresses in single-via structure, 162–163
 Von Mises stress, 158

W

Wafer bonding techniques, 84
 Wafer-level packaging (WLP), 86
 Wafer process, 157
 Wafer processing, 257
 Wagner number, 66
 Wet chemistry, 177
 Wide/narrow Cu interconnects/diffusion barrier layer, 132*f*
 Wiring process, formation of, 149
 WLP, *see* Wafer-level packaging (WLP)

X

XPS, *see* X-ray photoelectron spectroscopy (XPS)
 X-ray fluorescence (XRF), 497–498
 energy dispersive, 498*f*
 high-luminosity EDXRF, 498*f*
 X-ray photoelectron spectroscopy (XPS), 171
 X-ray reflectometry (XRR), 499–500
 example of spectrum, 499*f*
 fast XRR devices, 500
 simplified scheme, 500*f*
 X7R capacitor powder, 76*f*

Y

Young’s modulus, 269, 275

Z

“Zeta-potential,” 74