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List of Acronyms

ADRES	Architecture for dynamically reconfigurable embedded systems
ALAP	As late as possible
ALU	Arithmetic-logic unit
AOP	Aspect oriented programming
API	Application programming interface
ASAP	As soon as possible
ASIC	Application-specific integrated circuit
ASIP	Application-specific instruction processor
AST	Abstract syntax tree
CCM	Custom computing machine
CDFG	Control/data flow graph
CDG	Control dependence graph
CFG	Control-flow graph
CISC	Complex instruction-set computer
CLB	Configurable logic block
CPLD	Complex programmable logic Devices
CPU	Central processing unit
CSD	Common signed digit
CSP	Communicating sequential processes
DAG	Directed acyclic graph
DDG	Data dependence graph
DFG	Data flow graph
DIL	Dataflow intermediate language
DISC	Dynamic instruction set computer
DRESC	Dynamically reconfigurable embedded system compiler
DRLE	Dynamically reconfigurable logic engine
DSE	Design space exploration
DSL	Domain specific language
DSP	Digital signal processor
EDIF	Electronic design interchange format
EPIC	Explicitly parallel instruction computing

FCCM	Field-custom computing machine
FDCT	Fast discrete cosine transform
FFT	Fast Fourier transform
FIFO	First in first out
FPAA	Field-programmable ALU arrays
FPGA	Field-programmable gate arrays
FSM	Finite-state machine
FSMD	Finite-state machine with data-path
FU	Functional unit
GPP	General purpose processor
HDL	Hardware description language
HLS	High-level synthesis
HPDG	Hierarchical program dependence graph
HTG	Hierarchical task graphs
IEEE	Institute of electrical and electronic engineers
ILP	Instruction level parallelism
IP	Intellectual property
IR	Intermediate representation
ISA	Instruction set architecture
I/O	Input/output
JIT	Just in time
JVM	Java virtual machine
LSB	Least significant bit/byte
LARA	LAnguage for Reconfigurable Architectures
LUT	Look-up table
MARGE	Malleable architecture generator
MSB	Most significant bit/byte
P&R	Placement and routing
PE	Processing element
PLD	Programmable logic device
PRISC	Programmable reduced instruction set computers
RAM	Random-access memory
ROM	Read-only memory
rDPA	re-configurable data-path architecture
REMARC	Reconfigurable multimedia array coprocessor
RFU	Reconfigurable functional unit
RISC	Reduced instruction-set computer
RPU	Reconfigurable processing unit
RTL	Register transfer level
SIMD	Single instruction multiple data
SRAM	Static random-access memory
SSA	Static single assignment
STG	State transition graph

TDF	Task description format
VHDL	VHSIC (very high speed integrated circuit) hardware description language
VLIW	Very-long instruction width
VLSI	Very large scale integration

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