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Nanocrystal-Embedded-Insulator (NEI) Ferroelectric FETs for Negative Capacitance Device and Non-Volatile Memory Applications

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Abstract

We report a novel nanocrystal-embedded-insulator (NEI) ferroelectric field-effect transistor (FeFET) with very thin unified-ferroelectric/dielectric (FE/DE) insulating layer, which is promising for low-voltage logic and non-volatile memory (NVM) applications. The ferroelectric nature of the NEI layers comprising orthorhombic ZrO_2 nanocrystals embedded in amorphous Al_2O_3 is proved by polarization voltage measurements, piezoresponse force microscopy, and electrical measurements. The temperature dependent performance and endurance behavior of a NEI negative capacitance FET (NCFET) are investigated. A FeFET with 3.6 nm thick FE/DE achieves a memory window larger than 1 V, paving a pathway for ultimate scaling of FE thickness to enable three-dimensional FeFETs with very small fin pitch.

Keywords: NEI, Ferroelectric, NC, Memory, Germanium, FeFET

Background

Field-effect transistors with a ferroelectric gate insulator layer (FeFETs) have attracted considerable interest for a variety of integrated circuit applications. Due to its inherent negative capacitance (NC) properties, a FeFET can achieve steeper switching behavior than a conventional MOSFET, enabling lower voltage operation [1]. Various channel structures [2–4] and materials [5–7] have obtained sub-60 mV/decade subthreshold swing (SS). Also, hysteresis in the current-voltage (*I-V*) characteristic due to remnant polarization (P_r) can be used for non-volatile memory (NVM) application [8]. Material development for FeFETs recently has focused on polycrystalline-doped HfO_2 due to its better thickness scalability [9] and CMOS process compatibility [2]. However, there still exists a fundamental limit for HfO_2 thickness scaling to avoid undesired gate leakage current; this in turn limits the FinFET [2]. Inspired by the nanocrystal MOS and memory device concept [10, 11], an insulating dielectric (DE) layer with embedded ferroelectric (FE) nanocrystals is introduced in this work. The resulting new device design illustrated in Fig. 1 is called the "Nanocrystal-Embedded-Insulator" (NEI) FeFET. The main advantage of this design is a thinner unified-FE/DE layer that meets the low-gate-leakage requirement.

In this work, NEI FeFETs are reported. Physical properties and ferroelectricity of the NEI layers with different physical thicknesses are characterized. Electrical performance of NEI FeFETs is investigated for low-voltage logic and NVM applications.

Methods

Key process steps for NEI FeFETs fabrication are shown in Fig. 1a. Four-inch n-type Ge(001) wafers with a resistivity of 0.088–0.14 Ω cm were used as the starting substrates. After pregate cleaning using diluted HF, Ge(001) wafers were loaded into an atomic layer deposition (ALD) chamber for the deposition of the NEI layer comprising ZrO_2 nanocrystals embedded in amorphous Al_2O_3 matrix. NEI layers with the various thicknesses were utilized in this work. TaN metal gate was deposited on the NEI FeFETs using the reactive sputtering. After the gate patterning and etching, BF_2^+ ions were implanted

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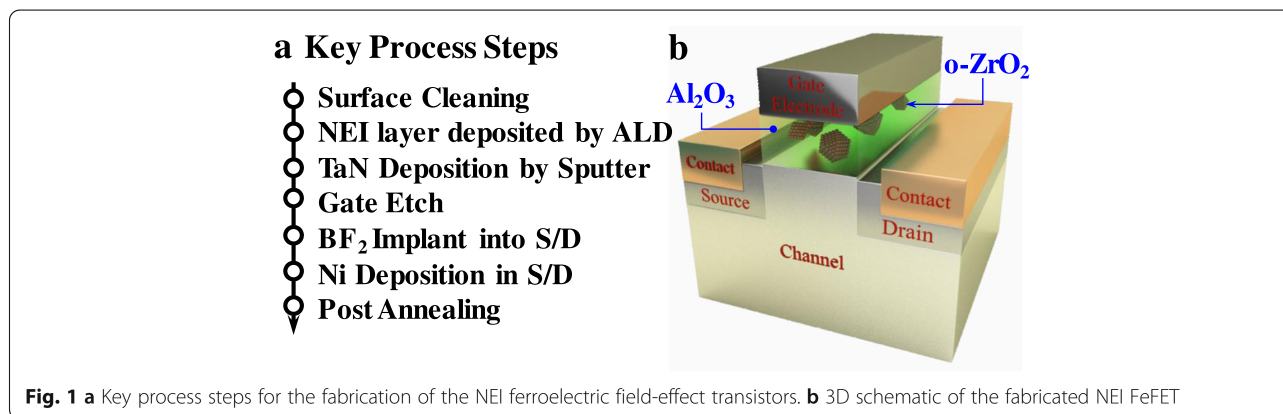

Fig. 1 **a** Key process steps for the fabrication of the NEI ferroelectric field-effect transistors. **b** 3D schematic of the fabricated NEI FeFET

into the source/drain regions at an energy of 20 keV and a dose of 1 × 15 cm^{-2}. Thirty-nanometer nickel (Ni) was deposited in source/drain regions using the lift-off process. Finally, device fabrication was completed with rapid thermal annealing (RTA). Control metal-oxide-semiconductor field-effect transistors (MOSFETs) with a purely dielectric Al_2O_3 gate insulating layer also were fabricated.

Figure 1b shows the 3D schematic of the fabricated NEI FeFET, which comprises FE nanocrystals embedded in an amorphous DE gate insulating layer. Although the volume of FE material is small, it is sufficient for NCFET and NVM applications. The insulating DE material is key to achieving low gate leakage and low operating voltage; it should have both a large bandgap energy and high dielectric permittivity (κ). It also should provide for a high coercive field (E_c) of the embedded FE nanocrystals.

The cross-sectional transmission electron microscope (XTEM) image in Fig. 2a shows the source/drain, channel, and gate edge regions of a fabricated FeFET. Figures 2b and c indicate the thicknesses of the NEI layers studied in this work to be 3.6 and 2.1 nm, respectively. Note that an interfacial layer of GeO_x exists between the NEI layer and Ge, although it cannot be seen.

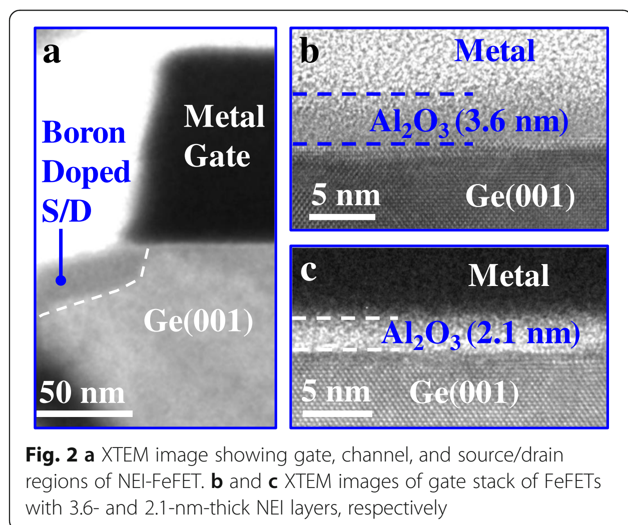

Fig. 2 **a** XTEM image showing gate, channel, and source/drain regions of NEI-FeFET. **b** and **c** XTEM images of gate stack of FeFETs with 3.6- and 2.1-nm-thick NEI layers, respectively

High-resolution TEM (HRTEM) images in Fig. 3 demonstrate the ZrO_2 nanocrystals embedded in amorphous Al_2O_3 on Ge(001) in the NEI samples with thicknesses of 3.6 and 6 nm. In our previous work, we have shown that the atomic percentage of Zr in the NEI layer is less than 0.5% [12]. Based on the diffraction patterns, the interplanar spacing d within the nanocrystals is calculated to be 0.173 nm, which corresponds to (111)-oriented orthorhombic ZrO_2 phase [13].

Polarization vs. voltage (P-V) and piezoresponse force microscopy (PFM) measurements were carried out on the NEI samples with the different thicknesses. To characterize the ferroelectricity of the NEI layer, P-V curves of TaN/NEI (3.6 nm)/Ge, TaN/NEI (6 nm)/$Si_{0.7}Ge_{0.3}$, and TaN/NEI (10 nm)/TaN capacitors are shown in Fig. 4a, b, and c, respectively. The NEI layer exhibits a lower P than the reported values of $HfZrO_2$ (HZO) [14], which is due to the fact that the volume ratio of ZrO_2 nanocrystal in Al_2O_3 matrix is quite low. It is seen that the remnant polarization P_r of the NEI film increases with the increasing of film thickness. P-V curves in Fig. 4c indicate that the ferroelectricity of the NEI layer degenerates while the annealing temperature increases from 450 to 550 °C. It is noted that the reason for the unclosed P-V loops is because a leakage indeed exists. It was reported that the resultant offset at zero electric field diminishes as the voltage sweeping range is reduced [3, 15, 16]. The amplitude (upper) and phase (lower) images of 3.6 nm, 6 nm, and 10 nm NEI were measured, as shown in Fig. 5a, b, and c, respectively. As shown in Fig. 6, patterns indicating the opposite polarity written onto the surface of NEI on TaN exhibit the clearer contrast with the increasing of film thickness.

Results and Discussion

NEI NCFET

Figure 7a shows measured I_{DS}-V_{GS} curves of the NEI NCFETs with a NEI thickness of 3.6 nm annealed at 450

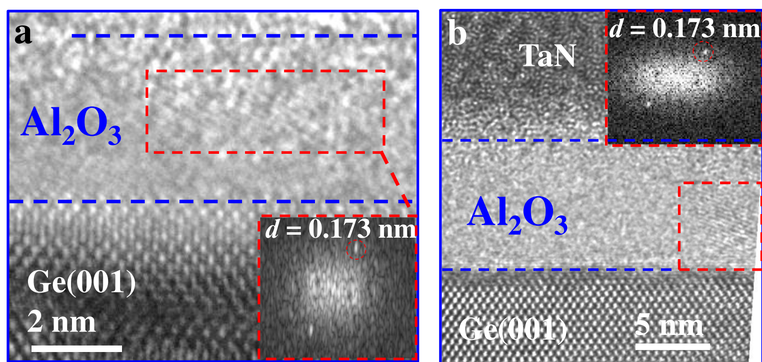

Fig. 3 HRTEM images showing nanocrystals embedded in amorphous Al_2O_3 for the samples with thicknesses of **a** 3.6 nm and **b** 6 nm. Insets show that the interplanar spacing *d* in the nanocrystal is 0.173 nm, corresponding to o-ZrO_2(111) phase

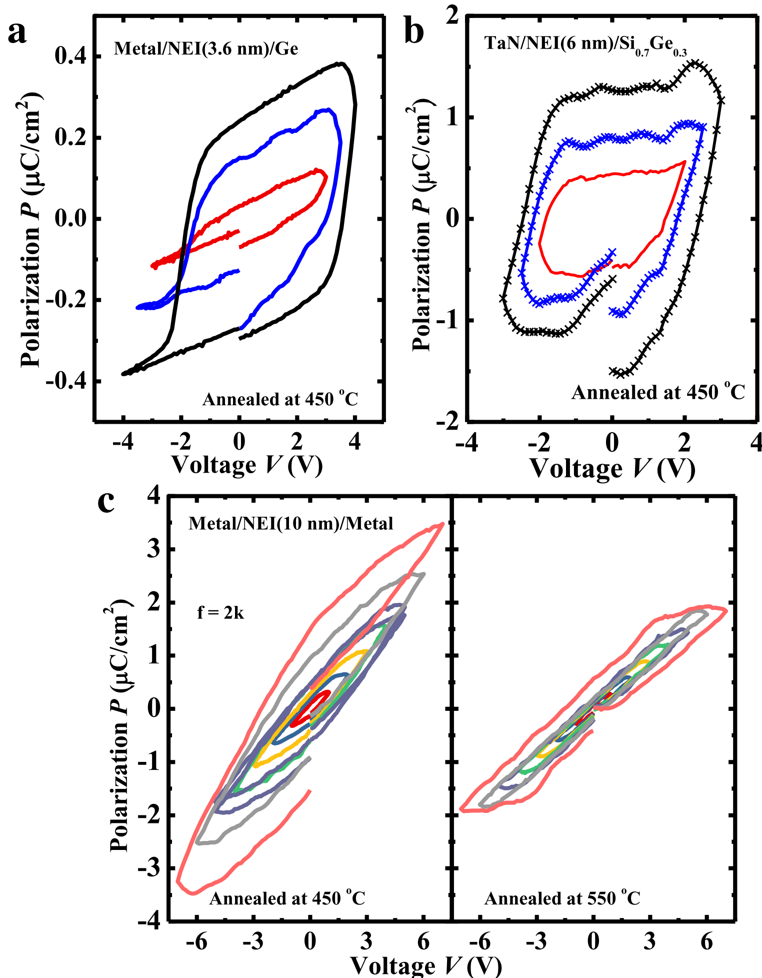

Fig. 4 a–**c** Measured *P-V* curves of TaN/NEI (3.6 nm)/Ge, TaN/NEI (6 nm)/$Si_{0.7}Ge_{0.3}$, and TaN/NEI (10 nm)/TaN, respectively

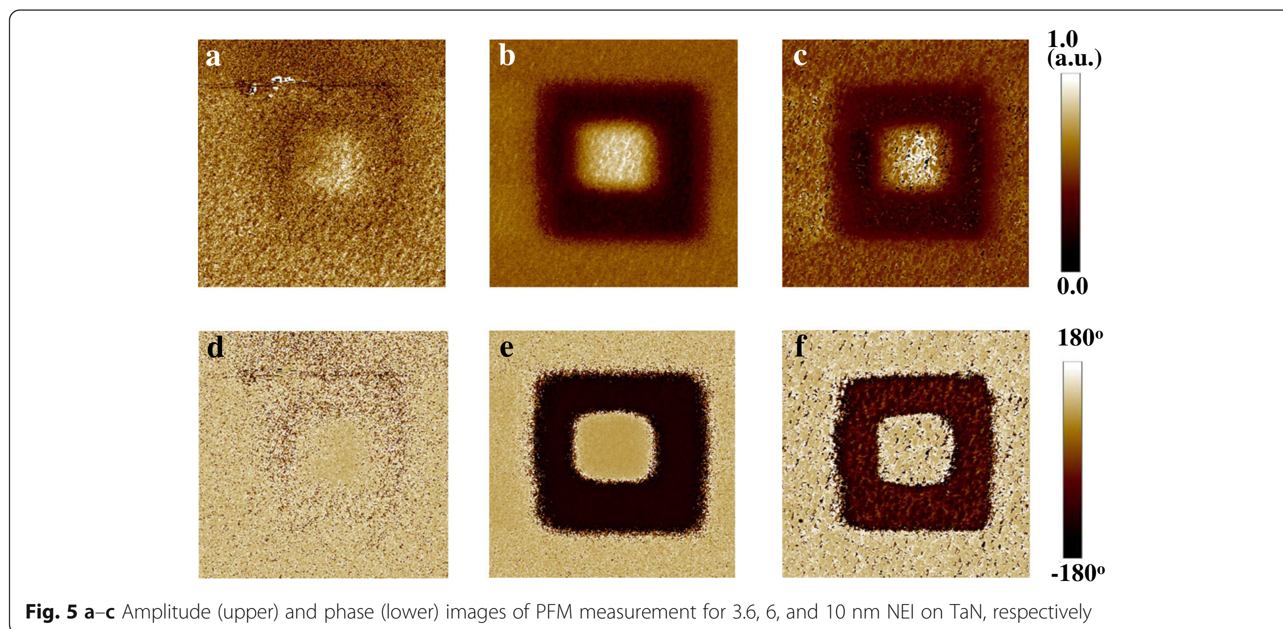

Fig. 5 a–c Amplitude (upper) and phase (lower) images of PFM measurement for 3.6, 6, and 10 nm NEI on TaN, respectively

°C and 500 °C. The NCFETs exhibit little hysteresis indicating the good matching between the ferroelectric capacitance and the MOS capacitance in the transistors. The NCFETs show the NC effect induced clockwise *I-V* loops, which is in contrast to the counterclockwise ones by charge trapping/detrapping [17]. The gate leakage I_G as a function of V_{GS} of the same pair of devices demonstrates that the formation of nanocrystals in Al_2O_3 does not increase the gate leakage. Figure 7b shows that the NCFETs achieve the sub-60 mV/decade steep SS points for the forward and reverse sweepings. The SS fluctuations in the NEI NCFET, also observed in NC FinFETs [2, 18], might be due to the polarization switching by the different ferroelectric nanocrystals or domains. The measured I_{DS}-V_{DS} curves for the same pair of devices in Fig. 7c show that at $|V_{GS} - V_{TH}| = |V_{DS}| = 1.0$ V, the NCFET with RTA at 500 °C achieves 29% larger I_{DS} in comparison with the transistor annealed at 450 °C. This is attributed to the fact that the carrier mobility in channel and contact resistance characteristics can be improved with the increasing of annealing temperature [19]. The typical characteristic induced by the ferroelectric layer, negative differential resistance (NDR), is observed in the I_{DS}-V_{DS} curves for the NCFETs annealed at the different temperatures.

Figure 8a shows measured I_{DS}-V_{GS} curves of a NEI NCFET and a control MOSFET with the same insulator thickness of 2.1 nm. Devices have a L_G of 6 μm. The

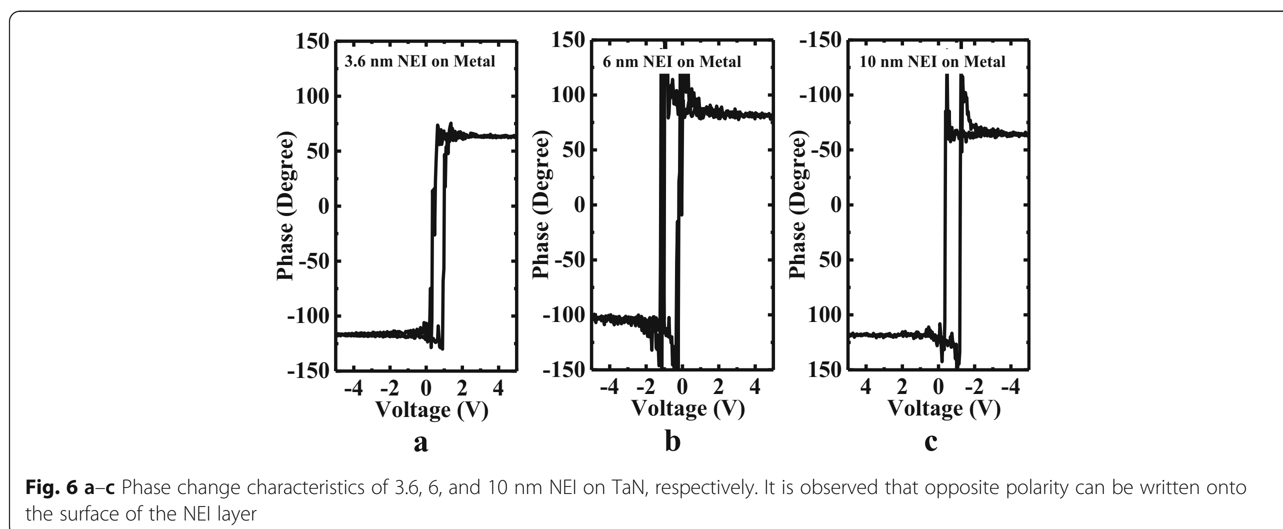

Fig. 6 a–c Phase change characteristics of 3.6, 6, and 10 nm NEI on TaN, respectively. It is observed that opposite polarity can be written onto the surface of the NEI layer

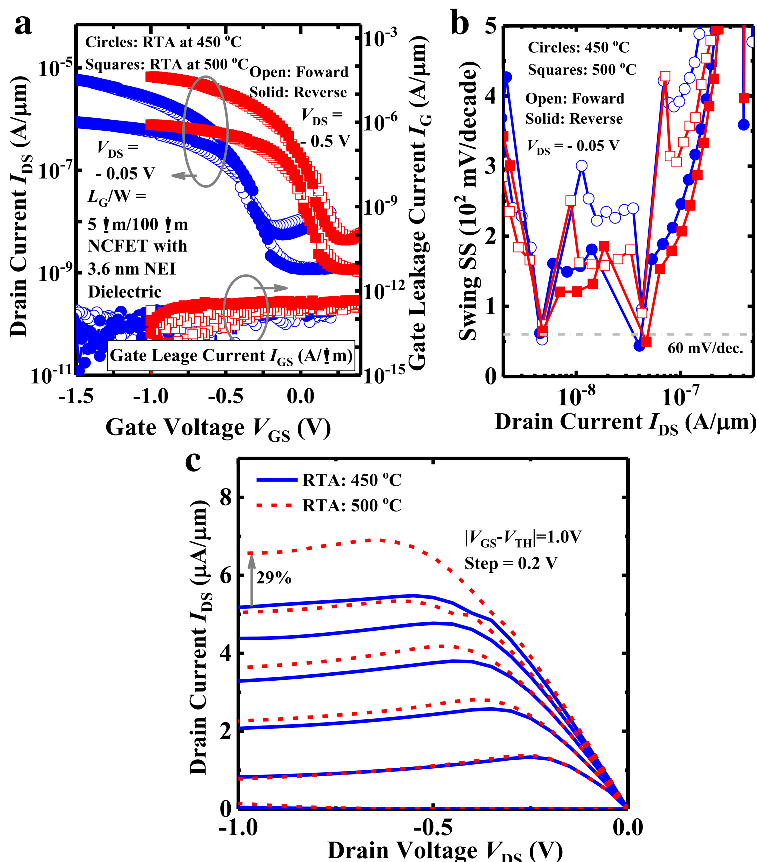

Fig. 7 a Measured I_{DS}-V_{GS} and I_G-V_{GS} curves of NCFETs with 3.6-nm NEI annealed at 450 °C and 500 °C. **b** NEI NCFETs has the sub-60 mV/decade points for a V_{DS} value of − 0.05 V. **c** I_{DS}-V_{DS} curves for the NEI NCFETs showing the obvious NDR phenomena. NC transistor annealed at 500 °C achieves a 29% I_{DS} improvement compared to the device with RTA at 450 °C at a supply voltage of 1.0 V

NCFET exhibits the hysteresis-free characteristics. The inset shows the point SS vs. I_{DS} curves for the devices, demonstrating that improved SS is achieved in the NCFET compared to the control device, up to the threshold voltage. Figure 8b shows the I_{DS}-V_{DS} curves of the NEI NCFET and the control MOSFET. NCFET exhibits the NDR phenomenon for the low V_{GS}. The NDR effect corresponds to the improved drain-induced barrier lowering (DIBL) characteristics in NCFET compared to the control MOSFET, as shown in Fig. 8a. At $|V_{GS} - V_{TH}| = |V_{DS}| = 1.0$ V, a 16% I_{DS} enhancement is obtained in NCFET in comparison with the control device. NCFET with 2.1 nm NEI has the less significant NDR compared to the transistor with 3.6 nm NEI, which is consistent with the conclusion in [20].

The temperature dependence of the NCFET with 3.6-nm-thick NEI is investigated herein. Figure 9a shows I_{DS}-V_{GS} curves measured at 10 °C and 30 °C. Inset indicates that the SS performance of the transistor does not degrade at the elevated temperatures. As the temperature increases, the *I*-*V* curve shifts to more negative V_{GS} due to the dominant effect of ferroelectricity, which is opposite to the trend for a conventional MOSFET. Figure 9b summarizes the shifts in hysteresis voltage and forward switching threshold voltage with temperature. Forward V_{GS} shifts to more negative values as temperature increases, which might be due to increased E_c of the NEI.

NEI FeFET for Non-Volatile Memory Application

By increasing the range of V_{GS} sweeping, the hysteresis voltage of a NEI FeFET can be increased to achieve a large and stable memory window (MW) for read and write operations. As shown in Fig. 10, a FeFET with 3.6-nm NEI demonstrates that the MW increases from 0.2 to 1.14 V as V_{GS} sweeping range varies from (0.1 V, − 0.1 V) to (1 V, − 2 V). DC sweep endurance of another FeFET memory device is shown in Fig. 11a, Fig. 11b illustrates the hysteresis characteristics as a function of number of DC sweeping cycles. Stable *I*-*V* hysteresis window of ~ 0.65 V is seen.

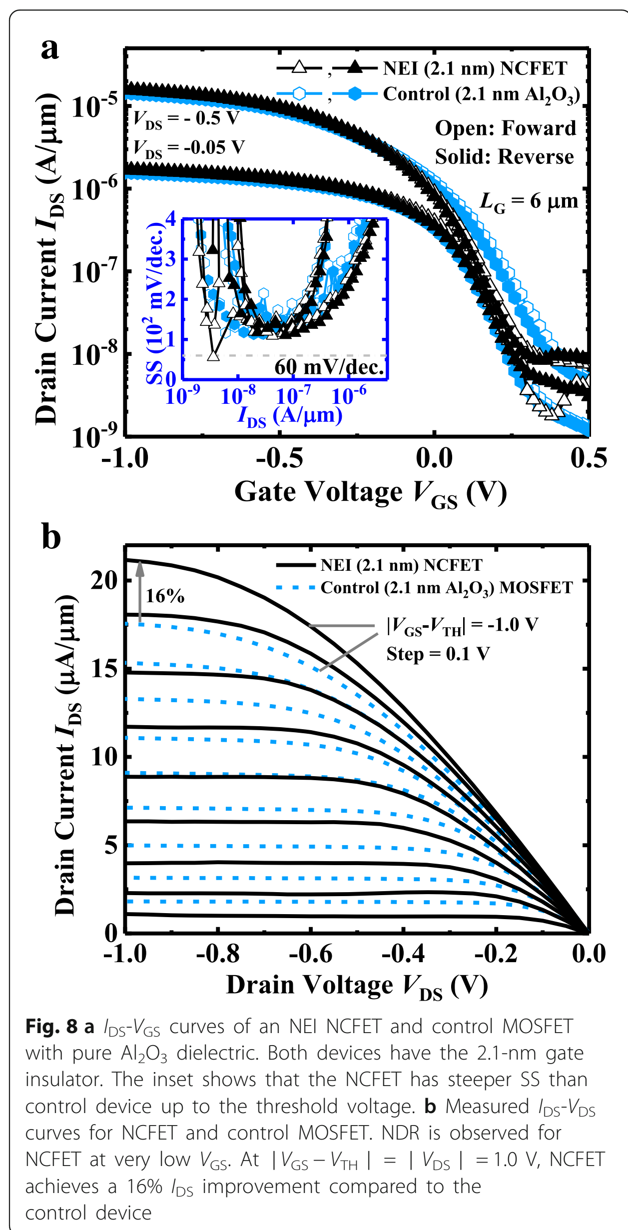

Fig. 8 **a** I_{DS}-V_{GS} curves of an NEI NCFET and control MOSFET with pure Al_2O_3 dielectric. Both devices have the 2.1-nm gate insulator. The inset shows that the NCFET has steeper SS than control device up to the threshold voltage. **b** Measured I_{DS}-V_{DS} curves for NCFET and control MOSFET. NDR is observed for NCFET at very low V_{GS}. At $|V_{GS} - V_{TH}| = |V_{DS}| = 1.0$ V, NCFET achieves a 16% I_{DS} improvement compared to the control device

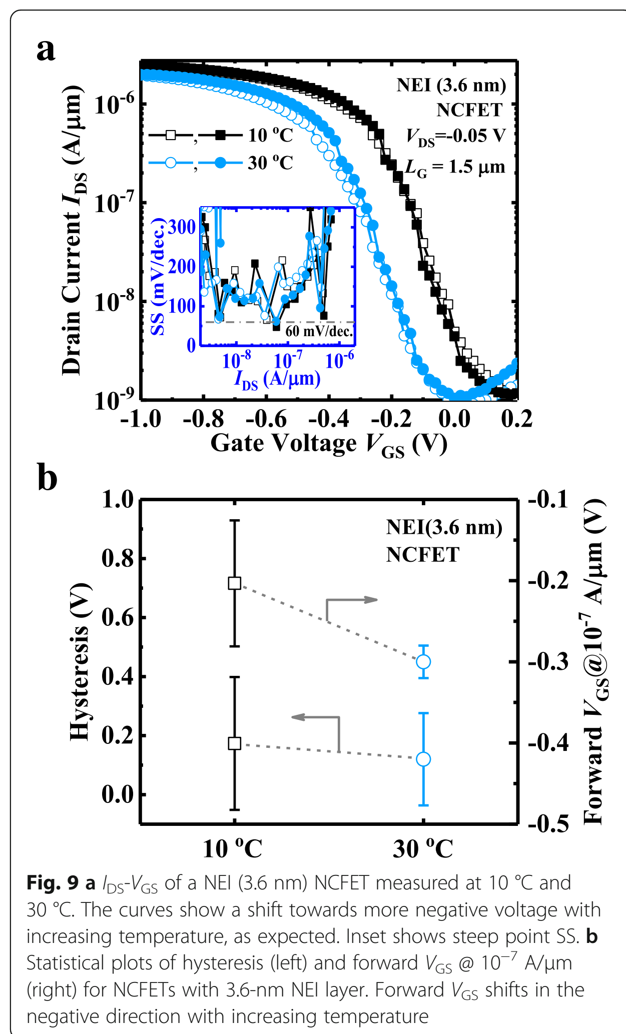

Fig. 9 **a** I_{DS}-V_{GS} of a NEI (3.6 nm) NCFET measured at 10 °C and 30 °C. The curves show a shift towards more negative voltage with increasing temperature, as expected. Inset shows steep point SS. **b** Statistical plots of hysteresis (left) and forward V_{GS} @ 10^{-7} A/μm (right) for NCFETs with 3.6-nm NEI layer. Forward V_{GS} shifts in the negative direction with increasing temperature

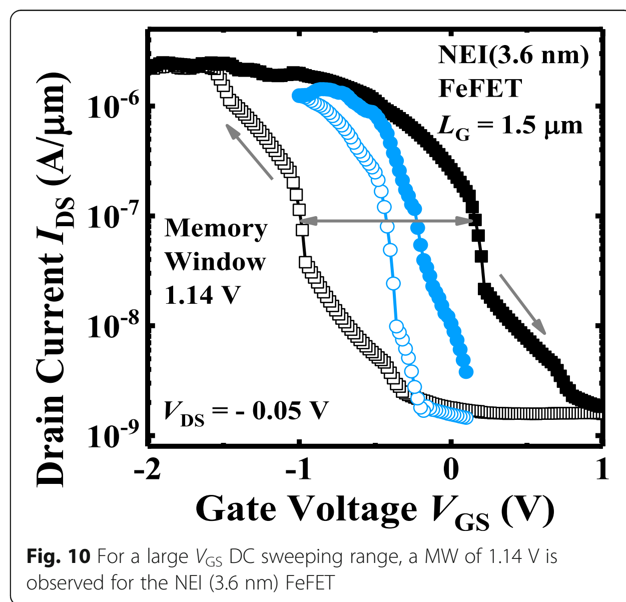

Fig. 10 For a large V_{GS} DC sweeping range, a MW of 1.14 V is observed for the NEI (3.6 nm) FeFET

Figure 12 benchmarks the NEI FeFET memory device against reported FeFETs, with regard to MW and FE layer thickness [8, 21–24]. It should be noted that the NEI FeFET device in this work achieves a sizable (> 1 V) MW with the thinnest reported FE thickness of 3.6 nm. We speculate that it is easier to achieve the stable FE phase in NEI with a smaller thickness, as compared to the doped HfO_2 [28–30].

Finally, the advantages of the NEI FeFET provided by ZrO_2 nanocrystals embedded in amorphous gate insulator are discussed. Figure 13 benchmarks the NEI layer against reported doped HfO_2 films [2, 3, 21, 25–27], with regard to E_c and P_r. NEI can achieve a much lower P_r compared to doped HfO_2 for similar

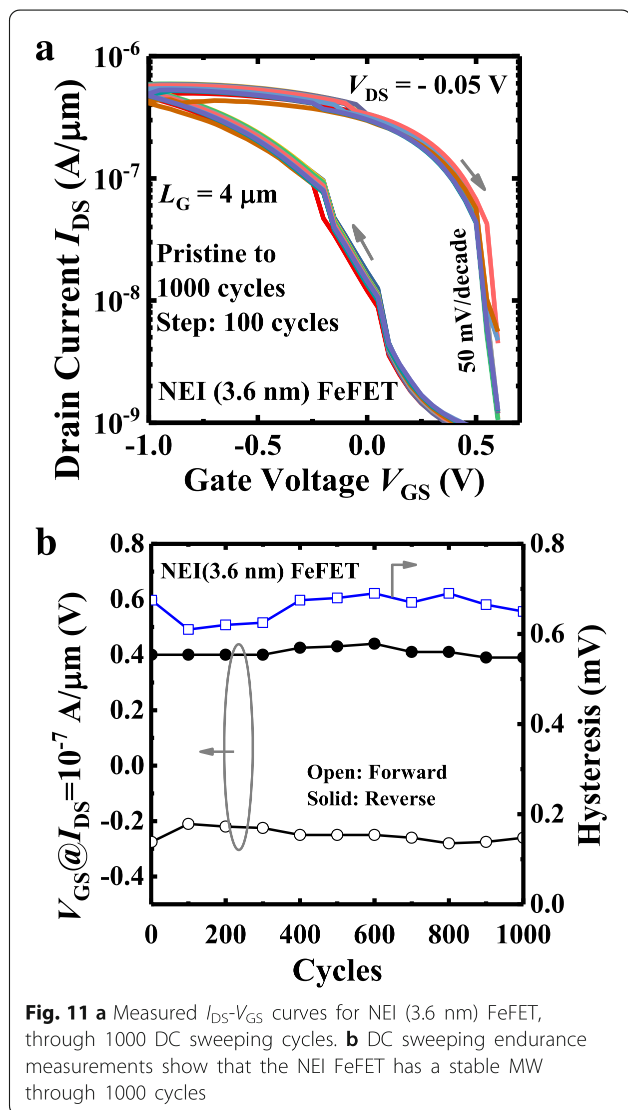

Fig. 11 **a** Measured I_{DS}-V_{GS} curves for NEI (3.6 nm) FeFET, through 1000 DC sweeping cycles. **b** DC sweeping endurance measurements show that the NEI FeFET has a stable MW through 1000 cycles

E_c. Our experiments have demonstrated that a P_r below 1 μC/cm^2 can provide the required MW in the FeFETs. Excessive polarization could lead to greater depolarization, resulting in worse retention characteristics, which was reported in [25]. Furthermore, the FE and DE properties of the NEI layer can be adjusted separately: P_r is enhanced/reduced by increasing/decreasing the volume of FE nanocrystals, and κ is increased by incorporating other elements in the amorphous matrix (e.g., $LaAlO_3$), to optimize FeFET performance.

Conclusions

Novel FeFETs with ZrO_2 nanocrystals embedded in an amorphous Al_2O_3 gate insulating layer are reported. Physical analyses indicate that less than 0.5% Zr in Al_2O_3 produces sufficient ferroelectricity for

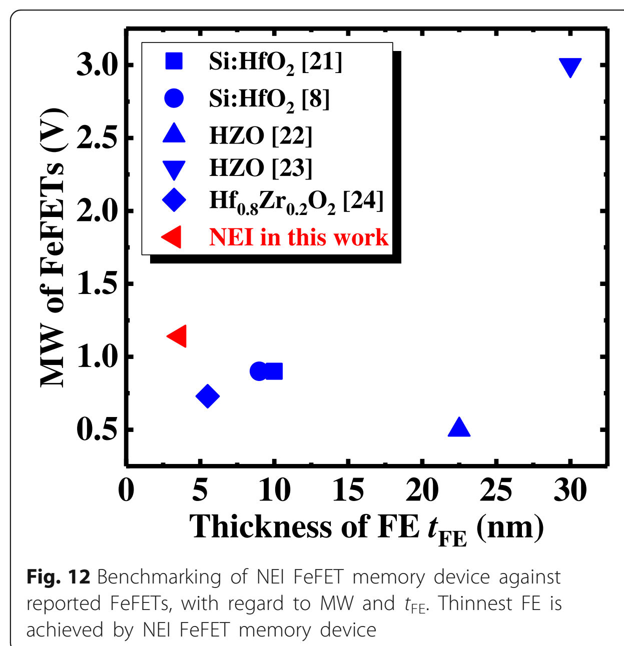

Fig. 12 Benchmarking of NEI FeFET memory device against reported FeFETs, with regard to MW and t_{FE}. Thinnest FE is achieved by NEI FeFET memory device

NCFET and NVM applications. Stable NC effect is observed at different measurement temperatures. Stable FeFET memory operation with record thin (3.6-nm total thickness) gate insulator is demonstrated. Stable MW is achieved over 1000 DC endurance cycles. The proposed NEI FeFET design provides a pathway for scaling down the thickness of the FE/DE gate insulator layer to be compatible with FinFETs with very small fin pitches.

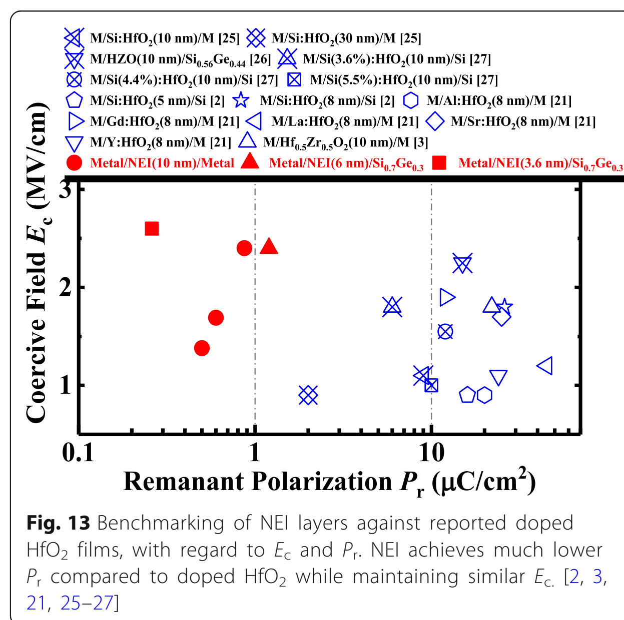

Fig. 13 Benchmarking of NEI layers against reported doped HfO_2 films, with regard to E_c and P_r. NEI achieves much lower P_r compared to doped HfO_2 while maintaining similar E_c. [2, 3, 21, 25–27]

Abbreviations

Al_2O_3: Aluminum oxide; ALD: Atomic layer deposition; BF_2^+: Boron fluoride ion; DC: Direct current; Ec: Coercive field; FeFET: Ferroelectric field-effect transistor; Ge: Germanium; GeO_x: Germanium oxide; HF: Hydrofluoric acid; HRTEM: High-resolution transmission electron microscope; I_{DS}: Drain current; MOSFETs: Metal-oxide-semiconductor field-effect transistors; MW: Memory window; NC: Negative capacitance; NDR: Negative differential resistance; NEI: Nanocrystal-embedded-insulator; Ni: Nickel; Pr: Remnant polarization; RTA: Rapid thermal annealing; SS: Subthreshold swing; TaN: Tantalum nitride; V_{GS}: Gate voltage; V_{TH}: Threshold voltage; ZrO_2: Zirconium dioxide

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Availability of Data and Materials

The datasets supporting the conclusions of this article are included within the article.

Authors' contributions

YP carried out the experiments and drafted the manuscript. GQH, YP, and WWX designed the experiments. JBW helped to measure the device. GQH and YL helped to revise the manuscript. JCZ and YH supported the study. All the authors read and approved the final manuscript.

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Competing interests

The authors declare that they have no competing interests.

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