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Ultra-Low Specific On-resistance Lateral Double-Diffused Metal-Oxide-Semiconductor Transistor with Enhanced Dual-Gate and Partial P-buried Layer

Zhuo Wang, Zhangyi'an Yuan, Xin Zhou*, Ming Qiao, Zhaoji Li and Bo Zhang

Abstract

An ultra-low specific on-resistance ($R_{on,sp}$) lateral double-diffused metal-oxide-semiconductor transistor (LDMOS) with enhanced dual-gate and partial P-buried layer is proposed and investigated in this paper. On-resistance analytical model for the proposed LDMOS is built to provide an in-depth insight into the relationship between the drift region resistance and the channel region resistance. N-buried layer is introduced under P-well to provide a low-resistance conduction path and reduce the resistance of the channel region significantly. Enhanced dual-gate structure is formed by N-buried layer while avoiding the vertical punch-through breakdown in off-state. Partial P-buried layer with optimized length is adopted under the N-drift region to extend vertical depletion region and relax the electric field peak in off-state, which enhances breakdown voltage (BV) with low drift region resistance. For the LDMOS with enhanced dual-gate and partial P-buried layer, the result shows that $R_{on,sp}$ is 8.5 mΩ·mm^2 while BV is 43 V.

Keywords: Enhanced dual-gate, Lateral double-diffused metal-oxide-semiconductor transistor (LDMOS), Partial buried layer, Specific on-resistance

Background

With the increase of demand for more complex and faster logic function in analog power IC, it is significant to improve the performance of the lateral double-diffused metal-oxide-semiconductor transistor (LDMOS), specially minimizing specific on-resistance ($R_{on,sp}$) and maximizing off-state breakdown voltage (BV) [1–9]. Most developed technologies focus on the drift region optimizing to improve the trade-off of $R_{on,sp}$ vs. BV for LDMOS devices [10–20]. In our previous work, the LDMOS with ultra-shallow trench isolation (USTI) was proposed [21]. The depth and corner angel of USTI were optimized to achieve best-in-class performance. However, for the low voltage LDMOS, the drift region is losing domination in $R_{on,sp}$ and the contribution of the channel region cannot be ignored.

Method

In this work, a novel ultra-low specific on-resistance LDMOS with enhanced dual-gate and partial P-buried layer is investigated. The physical models IMPACT.I, BGN, CONMOB, FLDMOB, SRH, and SRFMOB are used in numerical simulation. On-resistance analytical model is proposed to provide an in-depth insight into the relationship between the drift region resistance and the channel region resistance. Based on the model, N-buried layer and partial P-buried layer are optimized to achieve low $R_{on,sp}$ and high BV.

Results and Discussion

Figure 1a shows the schematic cross-section of ultra-low specific on-resistance LDMOS with enhanced dual-gate and partial P-buried layer. The LDMOS features the dual-gate with N-buried layer and the partial P-buried layer which contributes to reduce $R_{on,sp}$ and enhance BV, respectively. In the channel region, the enhanced dual-gate is formed by trench gate and highly doped

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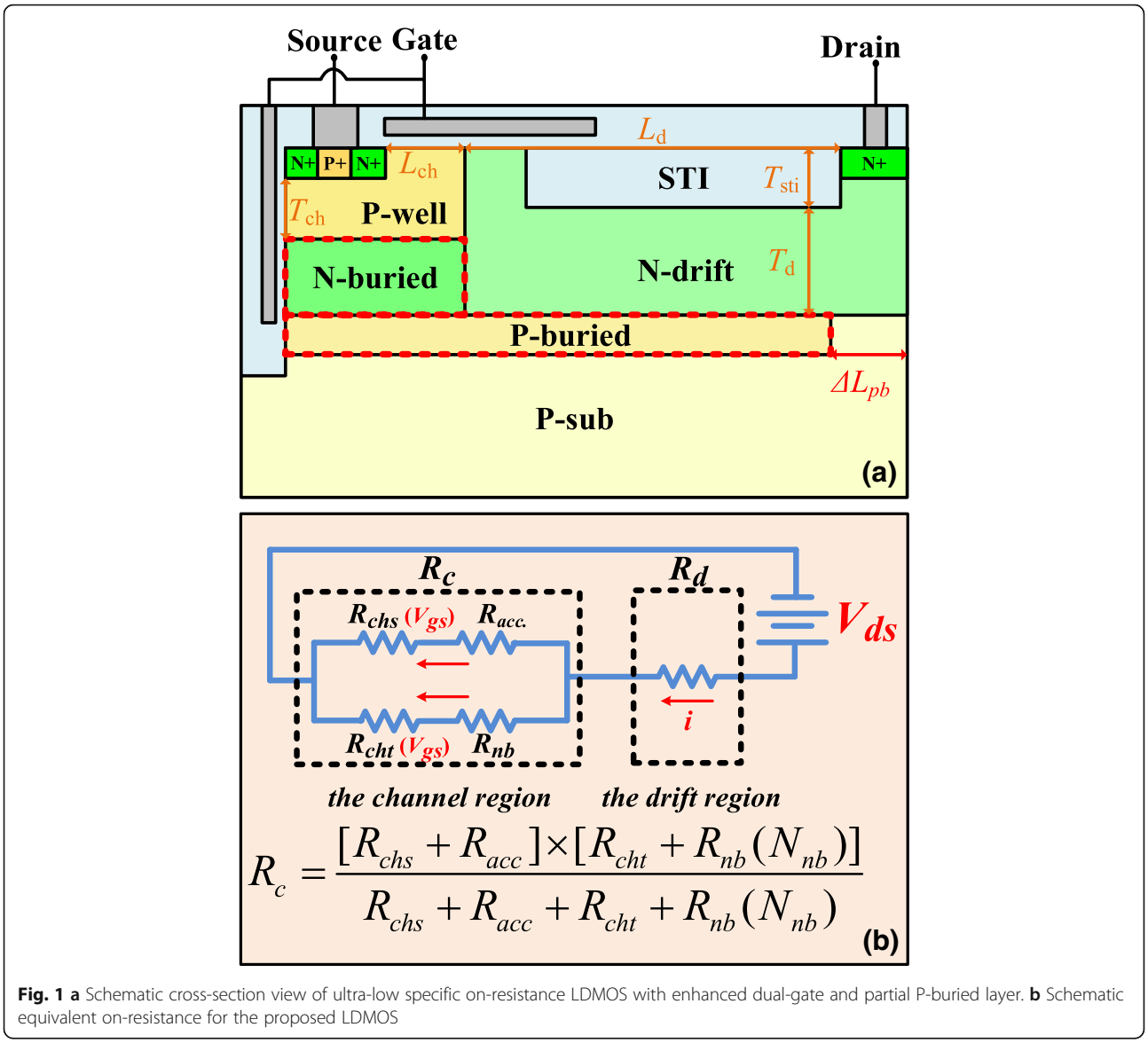

Fig. 1 **a** Schematic cross-section view of ultra-low specific on-resistance LDMOS with enhanced dual-gate and partial P-buried layer. **b** Schematic equivalent on-resistance for the proposed LDMOS

N-buried layer. Compare to conventional dual-gate structure, N-buried layer significantly reduce the resistance of the channel region by provide a low on-resistance conduction path under P-well in the on-state. In the drift region, the partial P-buried layer with high doping concentration is introduced under the N-drift region to enhance BV while maintaining low $R_{on,sp}$. The partial P-buried layer helps to reduce the vertical electric field in the off-state without breaking charge balance in the drift region. The key size of the novel device is listed in Table 1.

Figure 1b shows the schematic equivalent on-resistance model for the proposed LDMOS. The total on-resistance is considered as the resistance of the drift region (R_d) and the resistance of the channel region (R_c) in series. In the channel region, surface channel conduction path parallels the trench channel conduction path. Thus, R_c is equal to $(R_{chs} + R_{acc})//(R_{cht} + R_{nb})$, where R_{chs}, R_{acc}, R_{cht}, and R_{nb} are the resistances of the surface-gate channel, the accumulation region, the trench gate channel, and the N-buried layer, respectively. Based on the proposed on-resistance model, the reduction of R_c would achieve by decreasing R_{nb} without affecting the other performances, because the other resistances are mainly determinate by

Table 1 The key size of the novel device

L_d	1.6 μm
L_{ch}	0.3 μm
T_{ch}	0.2 μm
T_{sti}	0.3 μm
T_d	0.7 μm

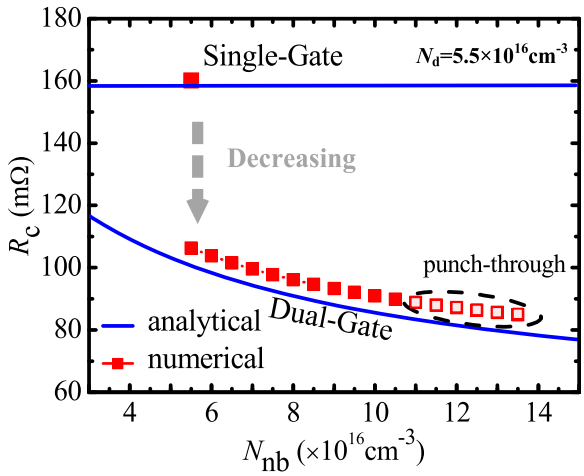

Fig. 2 Numerical and analytical R_c as a function of N_{nb} with single-gate and dual-gate ($Z = 1$ cm). N_d is the doping concentration of the N-drift region

the process technology, operation voltage, and threshold voltage. The R_d has been reduced by introducing P-buried layer under N-drift region to enhance the Reduce Surface-field (RESURF) effect in our previous work. In this work, the partial P-buried layer is adopted to improve the BV while maintaining the low R_d.

Aiming at the reduction of R_c, the N-buried layer with high doping concentration is introduced under P-well. Figure 2 shows numerical and analytical R_c as functions of the doping concentration of the N-buried layer (N_{nb}) with single-gate and dual-gate. It is indicated that the dual-gate structure helps to reduce R_c compared with the single-gate. When $N_{nb} = N_d = 5.5 \times 10^{16}$ cm^{-3}, R_c is 110 mΩ. According to the on-resistance model, R_{nb} is the main contributor to R_c. And then, the R_{nb} is desired to decrease with the aim of smaller R_c. As shown in Fig. 2a, R_c is reduced with N_{nb} increasing. When $N_{nb} = 1.35 \times 10^{17}$ cm^{-3}, R_c is reduced to 85 mΩ. However, Fig. 2 also shows that N_{nb} would be limited by punch-through breakdown. Because of adding trench gate, R_c is decreased firstly by 34% with $N_{nb} = N_d = 5.5 \times 10^{16}$ cm^{-3}. As N_{nb} increases, R_c continuously decreases. With optimized $N_{nb} = 1.05 \times 10^{17}$ cm^{-3}, R_c is decreased by 45% at last. When $N_{nb} > 1.05 \times 10^{17}$ cm^{-3}, punch-through breakdown will happen in P-well. The analytical result of $R_{on,sp}$ shown in Fig. 2 indicates that the proposed model provides a good fitting with numerical simulation results. Therefore, the model is believable to guide the optimization design.

Figure 3a shows numerical BV as a function of N_{nb} with different doping concentration of P-well (N_{pwell}). N_{nb} has an effect on not only the R_c, but also the BV. For a given N_{pwell}, BV keeps unchanged at small N_{nb}, and then decreases with N_{nb} increasing. When N_{nb} increases to 1.2×10^{17} cm^{-3}, BV starts to drop with $N_{pwell} = 2 \times 10^{17}$ cm^{-3}. The drop of BV is ascribed to punch-through breakdown in the P-well region as shown in Fig. 3b. As drain voltage increases, the depletion region in P-well extends to the source. When the depletion region attacks the N+/P-well junction, the punch-through breakdown occurs. For a large N_{pwell}, the depletion mainly extends to the drift region, and the punch-through

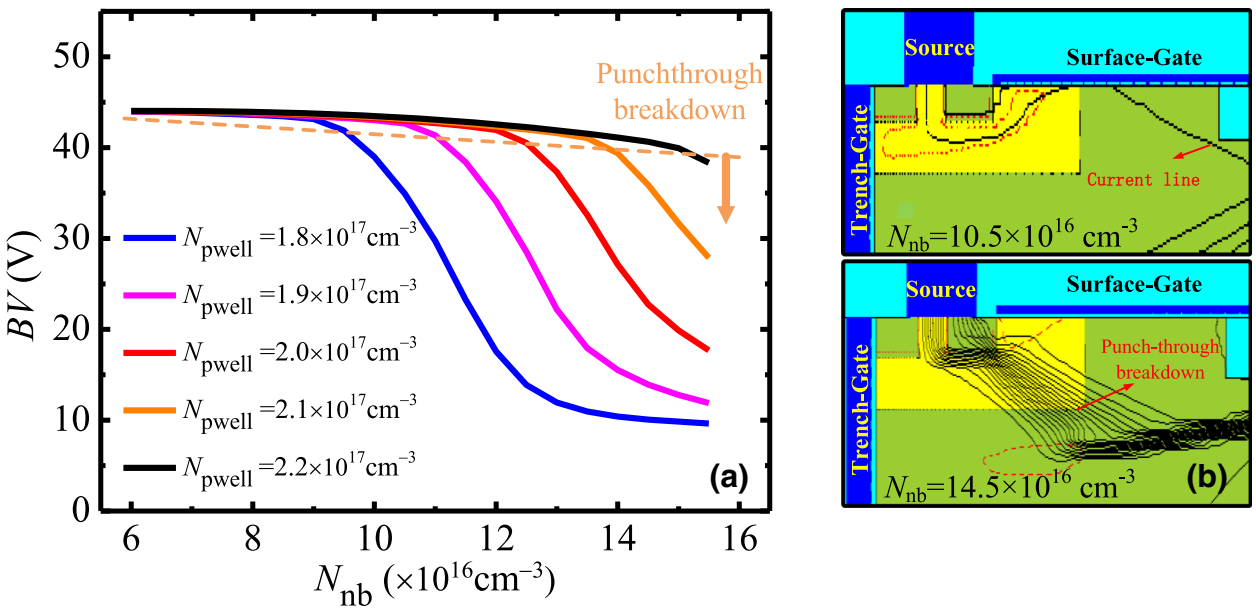

Fig. 3 a Numerical BV as a function of N_{nb} with different N_{pwell}. **b** Current density profile for $N_{nb} = 10.5 \times 10^{16}$ cm^{-3} and 14.5×10^{16} cm^{-3} while $N_{pwell} = 2 \times 10^{17}$ cm^{-3} at breakdown

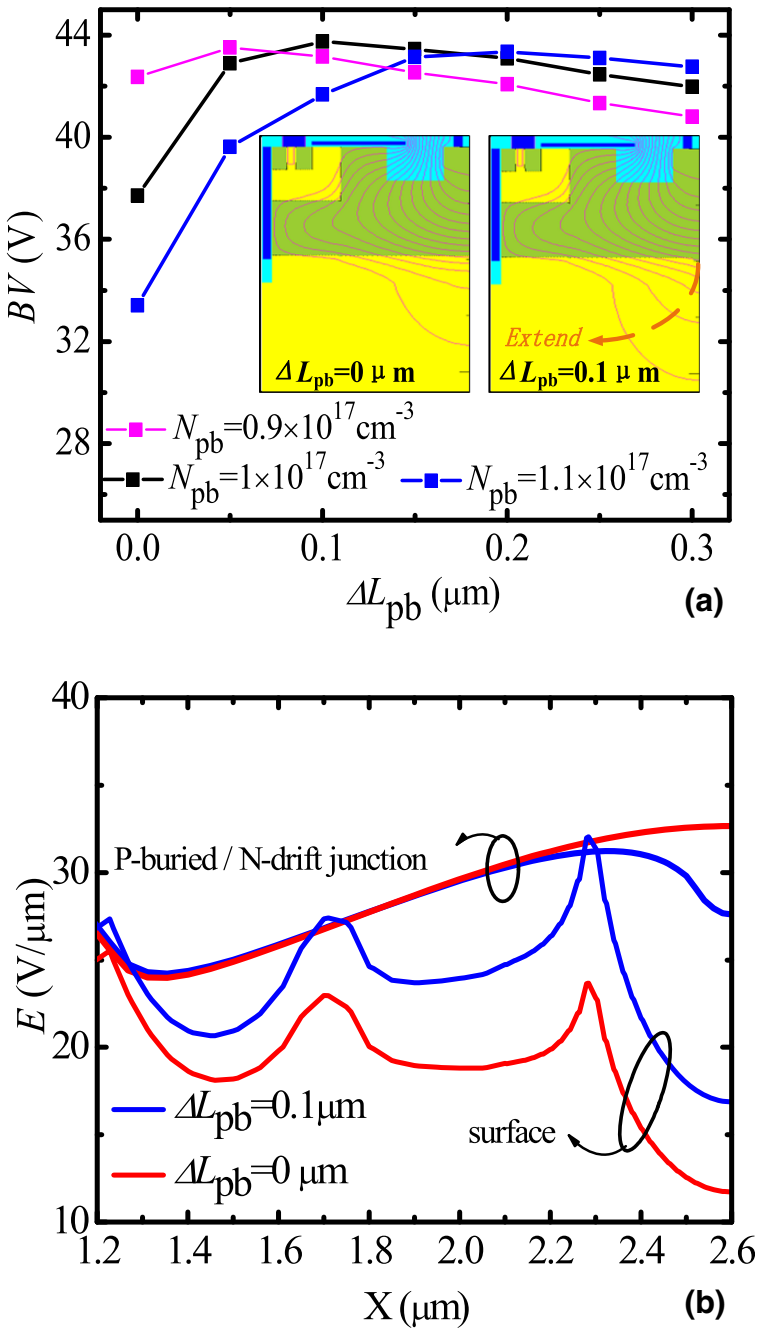

Fig. 4 **a** BV as a function of ΔL_{pb} with different N_{pb}. The insert is the equipotential contour profile with $N_{pb} = 1 \times 10^{17}$ cm^{-3}. **b** Electric field distribution at the surface and the P-buried/N-drift junction interface

breakdown is avoided without degrading the BV. Although P-well with high doping concentration benefits to avoid the punch-through breakdown, it would enhance the threshold voltage. Thus, N_{pwell} of 2×10^{17} cm^{-3} is chosen with consideration to threshold voltage and the trade-off between the BV and $R_{on,sp}$.

In order to achieve low R_d and high BV, partial P-buried layer is introduced under the N-drift region. Figure 4a shows BV as a function of ΔL_{pb} with different N_{pb}. For a given N_{pb}, as ΔL_{pb} increases, BV increases and then decreases slightly. When $\Delta L_{pb} = 0.1$ μm, $N_{pb} = 1 \times 10^{17}$ cm^{-3}, BV reaches the maximum value 43 V. The insert shows the equipotential contour profile with $N_{pb} = 1 \times 10^{17}$ cm^{-3}. It is indicated that the equipotential contour in the partial P-buried layer structure extends more to substrate with comparison to full P-buried layer.

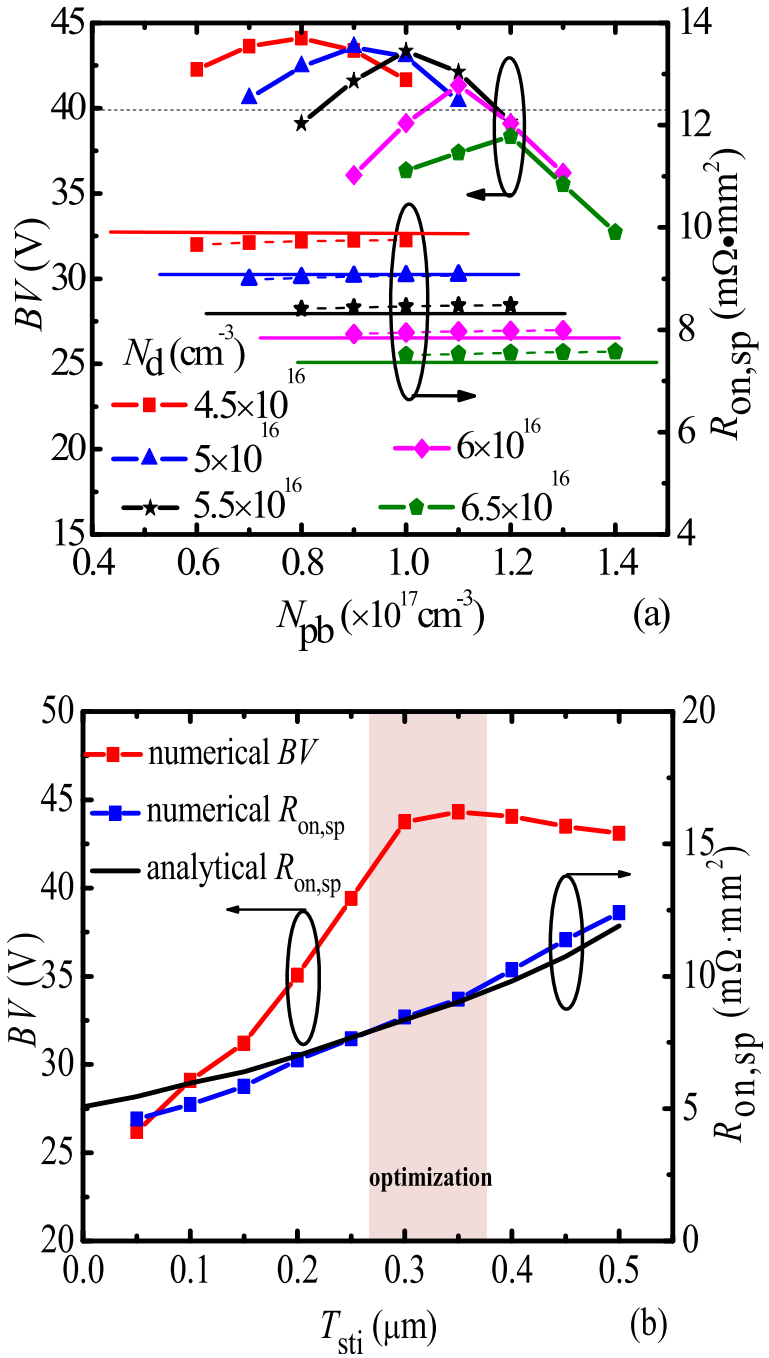

Fig. 5 **a** Numerical (dotted line) and analytical (solid line) BV and $R_{on,sp}$ as functions of N_{pb} for different N_d. **b** Numerical (dotted line) and analytical (solid line) BV and $R_{on,sp}$ as functions of T_{sti}

Figure 4b shows electric field distribution at the surface and the P-buried/N-drift junction interface. For optimized conventional LDMOS, the breakdown occurs usually at the N-drift/P-buried interface. For the proposed LDMOS, the junction of N-drift/P-sub replaces the junction of N-drift/P-buried to relax the vertical electric field and extend depletion region, which results in a higher BV while maintaining low R_d.

Charge balance between N-drift and partial P-buried layer is required to achieve high BV. Figure 5a shows that numerical and analytical BV and $R_{on,sp}$ as functions of the doping concentration of the P-buried (N_{pb}) for different N_d. For a given N_d, BV has a maximum value with varied N_{pb}, and the maximum of BV increases with the decrease of N_d. However, $R_{on,sp}$ can be increased as the N_d decreasing. Due to BV required higher than 40 V,

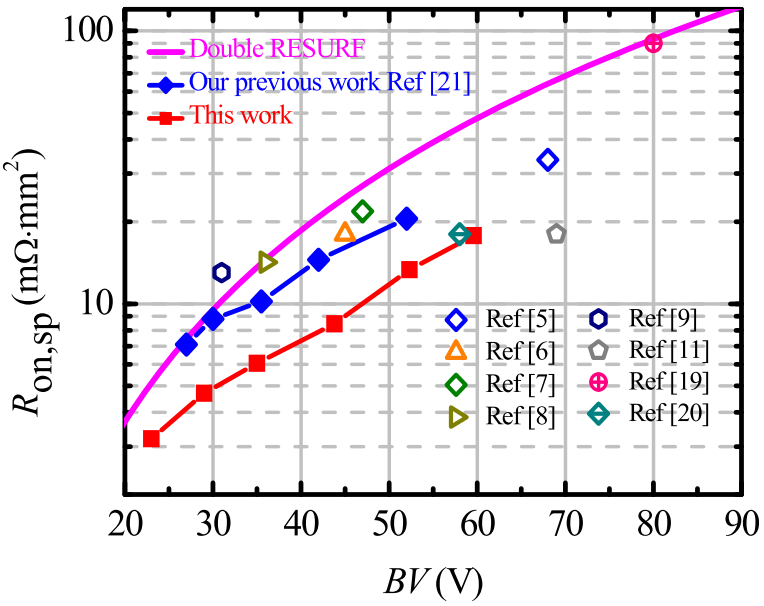

Fig. 6 The benchmark of existing BCD technologies and the proposed LDMOS

the $N_d = 5.5 \times 10^{16}\,cm^{-3}$ and $N_{pb} = 1 \times 10^{17}\,cm^{-3}$ are chosen. Figure 5b shows numerical and analytical BV and $R_{on,sp}$ as functions of the thickness of the STI layer (T_{sti}). T_{sti} has strong impact on BV and $R_{on,sp}$, and it should be designed and optimized carefully as well as our previous work [21]. For $T_{sti} < 0.3$ μm, the breakdown point under the edge of poly field plate has a high electric field peak. As T_{sti} increases, the electric field peak is relaxed, and then BV increases. For $T_{sti} = 0.3$ μm, BV of 43 V is obtained. For $T_{sti} \geq 0.3$ μm, the electric field peak under the edge of poly field plate is enough low, as a result, the breakdown point transfers to P/N junction under the drain side. As T_{sti} increases, BV increases and then saturates.

Figure 6 shows the benchmark of existing Bipolar-CMOS-DMOS (BCD) technologies and the proposed LDMOS. Apparently, the process technology for proposed LDMOS is compatible with our developed BCD technology which achieved the best-in-class performance of LDMOS. In the fabrication process for the proposed LDMOS, N-buried layer could share the same mask with P-well. For the proposed LDMOS, $R_{on,sp}$ is 8.5 mΩ·mm^2 while BV = 43 V, which is reduced by about 37% compared with our previous work.

Conclusion

A novel ultra-low specific on-resistance LDMOS with enhanced dual-gate and partial P-buried layer is proposed and investigated by numerical simulation in this paper. N-buried layer with high doping concentration is utilized to achieve enhanced dual-gate with reducing R_c. Partial P-buried layer is introduced under the N-drift region to enhance BV with keeping charge balance. The fabrication process of the LDMOS in this work is compatible with the existing BCD technology reported in our previous work. The result shows that the $R_{on,sp}$ of the proposed LDMOS is reduced by 37% at BV of 43 V compared with previous work. With the semiconductor processing technology going to nanometer level, the $R_{on,sp}$ can reduce further with channel length decrease.

Abbreviations

BCD: Bipolar-CMOS-DMOS; BV: Breakdown voltage; LDMOS: Lateral double-diffused metal-oxide-semiconductor transistor; RESURF: Reduce surface-field; $R_{on,sp}$: Specific on-resistance; USTI: Ultra-shallow trench isolation

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Availability of Data and Materials

All data generated or analyzed during this study are included in this published article.

Authors' Contributions

ZW proposed the novel structure and was a major contributor in writing the manuscript. ZY built, deduced, and calculated the analytical model. XZ verified the analytical model by simulation software. Other authors offered comments and revised the manuscript. All authors read and approved the final manuscript.

Competing Interests

The authors declare that they have no competing interests.

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