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Editorial

Transforming Signal Processing Applications into Parallel Implementations

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Improving silicon technology has offered the possibility of heterogeneous platforms involving multiple multiprocessors, DSP processors, and FPGAs, but the key issue is the creation of the methodologies and tools that allow designers to quick and efficient map complex DSP systems onto such platforms. Typically, these design processes will involve application modeling and development of transformations for mapping these application models onto hardware architecture models against some key performance criteria such as timing, area, or power consumption.

The purpose of this special issue is to highlight work which addresses the limitations in mapping from the application model onto the architecture model for complex DSP systems. These are not addressed in current design tool offerings to any great extent and issues include automatic translation of features in application specific models such as tokens and actors into "architecture model" specific expressions; exploration of algorithmic parallelism in such a way to make it match hardware platforms and development of transformations to reduce energy consumption and area against a throughput budget.

The papers addresses a number of topics ranging from model of computation (MoC) representations through to tools to explore realizations from SystemC descriptions.

In "SPRINT: a tool to generate concurrent transaction level models from sequential code," J. Cockx et al. describe a tool to generate a concurrent SystemC transaction level model from sequential code. Using this tool, different parallelization alternatives were evaluated during the design of an MPEG-4 simple profile encoder and an embedded zero tree coder. With their approach, generation was carried out in minutes thereby allowing extensive exploration of the design space.

In "Self-timed scheduling analysis for real-time applications," O. M. Moreira and M. J. G. Bekooij describe an approach that uses multirate dataflow graphs (MRDFs) to schedule the tasks of a hard real-time streaming application onto a multiprocessor system-on-chip. They extended the temporal analysis of self-time scheduling (STS) for MRDF graphs to model not only the average throughput but latency as well. This allows the maximum latency to be determined for jobs with periodic, sporadic, and bursty sources. The approach is demonstrated for a simplified channel equalizer and a wireless LAN receiver.

In "Development and evaluation of high-performance image decorrelation algorithms for the nonalternating 3D wavelet transform," E. Moyano-Ávila et al. show that by exploiting the inherent features of the application and the computing platforms they can achieve speedups in performance. They describe the implementation of a standard three-dimensional wavelet transform on an SGI Origin 38000, shared memory supercomputer and show that by partitioning the video sequences into groups and by implementing parallel versions of the algorithms, a workload distribution strategy can be deployed efficiently to distribute the workload across several processors.

In "Exploiting the expressiveness of cyclo-static dataflow to model multimedia implementations," K. Denolf et al. look at the design of complex multimedia systems using MoC descriptions. They show how cyclo-static dataflow (CSDF) makes a suitable MoC and show how "implementation specific" aspects can be expressed using CSDF. In particular, they

look at buffer requirements and demonstrate their approach for an MPEG-4 video encoder.

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Ed F. Deprettre was born in Roeselare, Belgium, on August 10, 1944. He is Fellow of the IEEE. He recieved the M.S. degree from the University of Ghent, Ghent, Belgium, in 1968, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 1981. 1980–1999, he was a Professor at the Department of Electrical Engineering, Circuits and Systems section, Signal Processing Group. From January 1st, 2000, he is Professor at the Leiden Institute of Advances Computer Sciences, Leiden University, Leiden, The Netherlands, where he is Head of the Leiden Embedded Research Center. His current research interests are in system level design of embedded systems, in particular for signal, image, and video processing applications, including wireless communications and multimedia. He is editor and coeditor of 4 books and several special issues of international journals. He is on the editorial board of 3 journals.

Roger Woods is a Professor at Queen's University Belfast and leads the Programmable Systems Laboratory. He received his BS.c. in electrical and electronic engineering and his Ph.D. from the same university in 1985 and 1990, respectively. His current research interests include system-level design flows and applications of programmable systems. He was General Chair of the FPL 2001 and the IEE's FPGA Developer's Forum in 2003 and 2005 and technical program committee cochair of 2005 IEEE IWVDVT workshop and 2008 Applied Reconfigurable Conference (ARC). He is on the program committee of conferences including SIPS, FCCM, FPL, FPT, ARC, and VLSIDAT. He has published over 130 scientific papers and holds a number of patents in the real-time implementation of digital filters. He is a Fellow of the IET and a Senior Member of IEEE.

Ingrid Verbauwhede 's interests include circuits, processor architectures, and design methodologies for real-time embedded systems in security, cryptography, digital signal processing, and wireless communications. This includes the influence of new technologies and new circuit solutions on the design of next generation systems-on-chip. She received her Electrical Engineering degree and Ph.D. degree from the K. U. Leuven in Belgium. She is currently a Professor there and an Adjunct Professor at UCLA. At K. U. Leuven, she is Codirector of the COSIC (Computer Security and Industrial Cryptography) lab. She was the Program Chair in 2002 and the General Chair in 2003 for the ACM/IEEE ISLPED conference, is the Program Chair for 2007 CHES conference, and was on the executive committee of the 42nd and 43rd DAC as the Design Community Chair. She is a Senior Member of IEEE and Member of the IEEE Signal Processing Society technical committee on Design and Implementation of Signal Processing Systems.

Erwin de Kock is a Principal Engineer at NXP Semiconductors in the area of system design methodology. He has 12 years experience in this area while being employed by Philips Research and NXP Semiconductors. He has worked amongst others on scheduling of real-time video signal processing systems, multiprocessor programming, programming models, program transformation, and multiprocessor system integration. Currently, Erwin is an Architect for the ESL IP integration environment within NXP Semiconductors. He also represents the company in the ESL Working Group of The SPIRIT Consortium. Erwin holds M.S. and Ph.D. degrees in computer science. He has published over 25 papers and he has served in technical program committees of several conferences including DATE and CODES+ISSS.