Research Article

Design and simulation of a high-performance Cd-free Cu_2SnSe_3 solar cells with SnS electron-blocking hole transport layer and TiO_2 electron transport layer by SCAPS-1D

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Abstract
This article presents numerical investigations of the novel (Ni/SnS/Cu_2SnSe_3/TiO_2/ITO/Al) heterostructure of Cu_2SnSe_3 based solar cell using SCAPS-1D simulator. Purpose of this research is to explore the influence of SnS hole transport layer (HTL) and TiO_2 electron transport layer (ETL) on the performance of the proposed cell. Based on the proposed device architecture, effects of thickness and carrier concentration of absorber layer, SnS HTL, TiO_2 ETL, absorber layer defect density, operating temperature and back-contact metal work function (BMWF) are studied to improve the cell performance. Our initial simulation results show that if SnS HTL is not introduced, the efficiency of standard Cu_2SnSe_3 cell is 1.66%, which is well agreed with the reported experimental results in literature. However, by using SnS and TiO_2 as HTL and ETL, respectively and optimizing the cell parameters, a simulated efficiency of up to 27% can be achieved. For Cu_2SnSe_3 absorber layer, 5×10^{17} cm^{-3} and 1500 nm are the optimal values of carrier concentration and thickness, respectively. On the other hand, the BMWF is estimated to be greater than 5.2 eV for optimum cell performance. Results of this contribution can provide constructive research avenues for thin-films photovoltaic industry to fabricate cost-effective, high-efficiency and cadmium-free Cu_2SnSe_3-based solar cells.

Keywords Cu_2SnSe_3 (CTSe) thin-film solar cells · SnS HTL · TiO_2 ETL · Cadmium-free solar cells · High-performance solar cells · SCAPS-1D

1 Introduction

Due to the serious global warming phenomenon caused by the use of fossil fuels, as an alternative energy resource and for sustainable development, it is demanding to improve the power conversion efficiency (PCE) and reduce the overall production cost of solar photovoltaic (PV) modules. Although the PCE of crystalline silicon-based solar cells is the highest, reaching 26.7% (single-cell) and 24.4% (module) among wafer-based technologies [1], thin-film solar cells (TFSCs) technology has a greater advantage in reducing raw material consumption, excluding energy-intensive manufacturing processes and higher performance stability at actual operating temperatures. Single-junction cuprous sulfide- cadmium sulfide (Cu_2S/CdS) solar cells are the first reported TFSCs and their PCE is about 9.1%, but the long-term performance is deteriorated due to the diffusion of copper into the CdS matrix and the doping of the CdS layer, for which further research activities on Cu_2S/CdS solar cells were turned down [2, 3]. Due to low-cost, material availability, non-toxicity, low processing temperature and cost-effective processing technologies, amorphous silicon (a-Si)-based solar cells among the TFSCs are preferable to the researcher. The PCE of TFSCs based on a-Si can reach up to 13.6% [4]. Current researches based on chalcogenide-based solar cells have

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made great contributions to the development of low-cost and earth-abundant TFSCs. In particular, cadmium telluride (CdTe) and copper-indium-gallium selenide (CIGS) based solar cells are two of the leading second generation TFSCs with the highest PCE of 22.1% and 22.6%, respectively [1]. However, Cd of CdTe-based TFSCs is recognized as a carcinogenic element and environmentally hazardous materials and Te is toxic as well as rare earth material [5]. Moreover, playing a key role in meeting current and future global energy demands in tera-watt scale, there are several shortcomings in terms of the overall sustainability of CIGS technology, due to the use scarce (*Ga, In*) elements [6–8] and the high material costs resulting from the large demand of *In* from the display industry [9]. Therefore, in the last decade, a negative impact on the viable potential of CdTe and CIGS-based technologies has been observed due to resource constraints as well as ecological issues. In this context, p-type kesterite based semiconductors with copper, zinc, tin and sulfur/or selenium (CZTS or CZTSe) as components, are considered to be an alternative absorber material due to their low-cost, non-toxicity and earth-abundancy [10–12] and shows high-efficiency potential for the near future [13]. Besides, the current production capacity of raw materials of CZTS allows sufficient solar cells to be produced to provide electricity on a Tera-Watt scale [14]. Consequently, in the last few years, CZTS and its related compounds, mainly, CZTSe and CZTSSe have received extensive attention as an absorber material for TFSCs. It was first identified as suitable absorber materials for solar cells in 1988 [10] and according to reports, the record efficiency of CZTS/CZTSe based TFSCs has increased from 0.66% in 1997 [12] to 12.6% in 2013 [15, 16]. Maximum efficiency of 17.59% and V_{OC} of 940 mV were observed for a silver mixed CZTS (ACZTS) cell with a (CdS/ ACZTS/CZTS/ITO) structure, as indicated by optoelectronic simulations [17]. Currently, this highly promising CZTS/ CZTSe material has not yet reached an efficiency equivalent to that of CIGS and CdTe-based solar cells. CZTS/CZTSe is a defect-prone system and consists of various types of defects like acceptor and donor vacancies (V_{Cu}, V_{Zn}, V_{Sn} and V_S), anti-sites defects (Cu_{Zn}, Zn_{Cu}, Cu_{Sn} and Sn_{Cu}), defect complexes such as ($Cu_{Zn}+Zn_{Cu}$), ($Cu_{Sn}+Sn_{Cu}$) etc. and interstitials defects, that result in shallow donor and acceptor energy levels, as well as mid-gap and deep trap states in the band gaps. Deep levels in the band gap make it easier to capture both minority and majority carriers. The larger potential fluctuations and higher defects density is identified as the massive V_{OC} deficit in CZTS/ CZTSe devices. Moreover, the stoichiometric deviation, due to more elements in the quaternary CZTS/CZTSe system, affects the crystal structure. In addition, too many elements in the absorber could increase the production cost of the solar cells. Therefore, finding a new and alternative absorber material, which must be less-defective, economical, ecological, abundantly available on Earth and easily controllable stoichiometry, is highly expected accordingly.

Therefore, the potentially attractive copper tin based ternary chalcogenide material Cu_2SnSe_3 (CTSe), which has not been well studied, could be a good alternative to the CISe, CIGSe and CZTSSe technology. In particular, CTSe is based on earth-abundant and nonhazardous elements, that has a simple cubic sphalerite like phase or monoclinic structure with a sphalerite superstructure [18, 19]. It is a p-type semiconductor, with a tunable direct band gap of 0.8 to 1.7 eV, a wide light absorption band and a high light absorption coefficient (10^4–10^5 cm^{-1}) and low electron and hole mobility [20–23]. More importantly, there is no zinc (Zn) in the CTSe material system, which can completely avoid the unfavorable [$Cu_{Zn}+Zn_{Cu}$] defect complexes [24] and eliminate the Zn-related secondary phases. However, the substitution of Sn into Cu sites is not energetically favored owing to the large difference in the effective ionic radii between Sn^{4+} (0.69 Å) and Cu^{1+} (0.77 Å) [25]. Therefore, Sn_{Cu} defects are unlikely to be produced in CTSe system as well.

Generally, in the manufacturing process of a multicomponent material system, with the number of components in the material system, the difficulty in the controlling of composition, phase and growth parameters increases. Complex quaternary material systems, such as CIGS, CZTS and CZTSe, require precise control of growth conditions. Therefore, the simpler ternary material system CTSe is highly attractive and is very suitable for manufacturing low-cost TFSCs due to its solution processibility and very suitable optoelectronic properties as mentioned earlier. In addition, it has been found that the phase stability zone of quaternary compounds (such as CIGS, CZTS and CZTSe) is much smaller than that of ternary compounds (such as CISe and CTSe), as a large number of competitive secondary phases are formed for the former compared to the latter. Moreover, CTSe-based quantum dot sensitized solar cells (QDSCs) showed much better catalytic activity as compared to devices made with CZTSe/CZTS as a counter electrode [26, 27].

In 2015, Tang Zeguo et al. first studied the feasibility of CTSe-based solar cells using (SLG/Mo/CTSe/CdS/ ZnO/ AZO/Al) device structures with PCE of 0.079% [28]. The low PCE of the devices was attributed to the presence of secondary phases like SnSe and $SnSe_2$ within the absorber films. In the same year, Ge-doped CTSe (CTGSe)-based solar cell was fabricated by Kang Min Kim et al. with the cell configuration of (glass/Mo/CTGSe/CdS/i-ZnO/ ZnO:Al/Al) and obtained the PCE of 0.045% for undoped CTSe and 3.02% for CTGSe [29]. Similarly, solar cells of (glass/ITO/CdS/CTSe/Ag) structure, with the highest PCE of 1.17%, fabricated through a combination of chemical

bath deposition and Doctor Blade technique, is reported by Basak et al. [30]. It has been proposed that the J_{SC} can be increased by optimizing the interface between the CTSe/CdS layer, thereby improving the PV performance. Recently, Dwivedi et al. reported an inverted hybrid TFSCs using CTSe-nanocrystals in the form of (glass/ITO/ZnO/P3HT:PCBM:CTSe-nanocrystal/Ag) and showed a maximum of 1.35% PCE [31]. Besides, Liu et al. reported for the first time TFSCs based on quantum dot sensitized (QDSC) CTSe with a device structure of (glass/FTO/CTSe/CdSe-QD-sensitized porous TiO_2) [32]. The device showed a record PCE of 4.93%. Therefore, given the poor efficiency reported by CTSe solar cells, it becomes evident that PV performance is still far from fully optimized and the PCE of CTSe solar cells is mainly limited by the quality of the CTSe absorber layer and the formation of poor p–n junction at interfaces (absorber/buffer). In particular, the high minority carrier recombination at the back contact (Mo)/absorber (CTSe) interface limits the V_{OC}, while improper band alignment at the CTSe/CdS interface causes the J_{SC} of the CTSe solar cells to decrease. Therefore, more studies are needed to further improve the device efficiency of CTSe-based solar cells. Use of TiO_2 and doped-TiO_2 to enhance the carrier transport in organic solar cells were reported in Ref. [33–35]. In this regard, we propose to use an n-type TiO_2 layer as an alternative to the CdS buffer layer for CTSe TFSCs. It can be a promising electron transport layer (ETL) for the CTSe-based solar cells due to its suitable band alignment with CTSe. In addition, a layer of p-type SnS thin films was added to the absorber layer as a back-surface passivation layer to reduce the minority carrier recombination at the back-electrode/CTSe interface, thereby enhancing the PV performance of the device.

Many researchers in this field have been presenting solar cells with improved PV performance over a period of time, even though the entire process is not only quite complex but also costly and time-consuming [36]. Nowadays, scientists are considering to use simulator to find out design optimizations of solar cells and predict certain factors to ensure the best results for their device. As a result, manufacturing complexity, cost and time are significantly reduced. In this work, the SCAPS-1D simulator is used to simulate the specific (Ni/SnS/CTSe/TiO_2/ITO/Al) structure of the solar cell to study and optimize the various PV performance parameters of the proposed device. In this study, *Ni* with the metal work function of 5.35 eV [37, 38] is used as back contact materials, as *Ni* is known to form a nearly ohmic contact with very low contact resistance with SnS [39], while, Al is used as front contact materials. The PV performance parameters are studied by tuning the back-contact metal work function, working temperatures and the thickness, carrier concentration, defect density of different layers to obtain an optimum cell performance.

2 Numerical modeling and simulation parameters

In this work, CTSe-based TFSC structure of (Ni/SnS/CTSe/TiO_2/ITO/Al) was implemented in the Solar Cell Capacitance Simulator (SCAPS-1D) environment. SCAPS-1D is a one-dimensional software based on solving three basic semiconductor device equations; Poisson's equation, the continuity equation for free holes and free electrons, under steady-state conditions [40]. It is a computer program that allows modeling of physical and electronic structures of TFSCs based on heterojunction, homojunction, multi-junction and even Schottky barriers and can be used by specifying the electrical and optical parameters of each defined layer as the input parameters of the simulation. CTSe material parameters, that are inputted in the simulator, ultimately determine the relative accuracy of simulated results. Therefore, the material parameters of the CTSe absorber layer are selected precisely from authentic literature, theory and in some cases reasonable assumptions to reflect the possible result under practical experimental conditions. Table 1 lists the baseline parameters for different layers of the device and their values used to perform the calculations. We have introduced one type of single deep-level defects in each semiconductor layer. Considering the recombination at two interfaces (CTSe/TiO_2 and SnS/CTSe), reasonable neutral interface defects are also used. Table 2 summarizes the interfacial defect parameters used in the simulation. The front and back contacts are characterized by the work function, reflectivity and surface recombination velocity. The reflection was assumed to be 90% at the back contact and 10% at the front contact [41]. Parameters for the front contact, back contact and working temperatures are attached in Table 3. For the simulation, the experimental absorption coefficient data of the SnS, CTSe, TiO_2, CdS and ITO were used from the literature [42–46]. The device was illuminated from the window layer (ITO) side and all calculations were performed under the standard AM1.5G solar spectrum (100 mW/cm^2) illumination [47]. The shunt resistance and series resistance were fixed at 1000 Ω cm^{-2} and 2.5 Ω cm^{-2}, respectively.

Table 1 Material parameters, used for simulating (Al/ITO/TiO_2/CTSe/SnS/Ni) solar cell [48–51]

Parameters	ITO	TiO_2 (ETL)	CTSe (Absorber)	SnS (HTL)	CdS
Thickness (nm)	50	20–60	1000–5000	100–500	50
Bandgap E_g (eV)	3.5	3.26 [44]	1.34 [52]	1.6 [42]	2.42
Electron Affinity, χ (eV)	4.6	4.20	4.41	4.1	4.3
Relative permittivity, ε_r	8.9	10.0	10.0	13.0	10.0
Effective CB density of states N_C (cm^{-3})	2.2×10^{18}	2.0×10^{17}	2.2×10^{18}	1.18×10^{18}	2.2×10^{18}
Effective VB density of states N_V (cm^{-3})	1.8×10^{19}	6.0×10^{17}	1.8×10^{19}	4.46×10^{18}	9.1×10^{18}
Electron Thermal Velocity (cms^{-1})	1.0×10^{7}	1.0×10^{7}	1.0×10^{7}	1.0×10^{7}	1.0×10^{7}
Hole Thermal Velocity (cms^{-1})	1.0×10^{7}	1.0×10^{7}	1.0×10^{7}	1.0×10^{7}	1.0×10^{7}
Electron mobility, μ_n ($cm^2V^{-1}\,s^{-1}$)	10	100	100	15	100
Hole mobility, μ_p ($cm^2V^{-1}\,s^{-1}$)	10	25	25	100	25
Donor concentration, N_D (cm^{-3})	1.0×10^{21}	$10^{16}-10^{20}$	0.0	0.0	1.1×10^{16}
Acceptor concentration, N_A (cm^{-3})	0.0	0.0	10^{14}—10^{18}	$10^{16}-10^{19}$	0.0
Defect density, N_t (cm^{-3})	1.0×10^{16}	1.0×10^{16}	$10^{16}-10^{19}$	1.0×10^{16}	1.0×10^{16}
Capture cross-section of electrons (cm^2)	1.0×10^{-17}	1.0×10^{-16}	1.0×10^{-15}	1.0×10^{-17}	1.0×10^{-17}
Capture cross-section of holes (cm^2)	1.0×10^{-15}	1.0×10^{-14}	1.0×10^{-15}	1.0×10^{-15}	1.0×10^{-15}

Table 2 Parameters used for defects at interfaces of solar cells

Parameters	SnS/CZTS	CZTS/TiO_2
Defect type	Neutral	Neutral
Capture cross-section of electrons (cm^2)	1.0×10^{-19}	1.0×10^{-19}
Capture cross-section of holes (cm^2)	1.0×10^{-19}	1.0×10^{-19}
Energetic distribution	Single	Single
Total defect density (cm^{-2})	1.0×10^{16}	1.0×10^{16}

Table 3 Front and back contact parameters used in simulation

Parameters	Back contact electrical properties	Front contact electrical properties
Surface recombination velocity of electrons (cms^{-1})	10^5	10^7
Surface recombination velocity of holes (cms^{-1})	10^7	10^5
Work function (eV)	5.35 *Ni* (111)	4.26 *(Al)*
Working Temperature (K)	290–390	

3 Results and discussions

3.1 Enhanced open circuit voltage (Voc) with SnS electron-blocking HTL and TiO_2 ETL

As we mentioned earlier, so far, CTSe-based TFSCs has not been studied well. Very few reports are found in literature in which the CdS layer and the CTSe absorber form a p–n junction [28–32]. Researchers use mostly Ag or Mo as the back-metal electrode, Al as the front electrode and ITO as the window layer. In this work, initially, a standard CTSe-based solar cell with the (Ag/CTSe/CdS/ITO/Al) structure has been adopted using the SCAPS-1D simulator. The J-V characteristics of the cell is shown in Fig. 1a. Analysis of J-V characteristics of the standard device revealed the poor PV performance in terms of $V_{OC}=0.449$ V, $J_{SC}=11.53$ mA/cm^2, FF = 32% and PCE = 1.66%. The results are consistent with those reported in the references [30]. The poor PV performance of the *Basic Cell* is due to the high series resistance offered by the device [30], which in turn reduces the FF and leads to inferior PV performance. In addition, the high minority carrier surface recombination rate at the absorber/back-electrode interface increases the dark current/minority carrier recombination current, thereby reducing V_{OC}. Hence, passivation of the surface of the absorber layer to reduce the surface recombination of minority carriers at the absorber/electrode interface is very important for improving V_{OC} and PV performance. Such a passivation layer at the absorber/back-electrode interface can be realized by incorporating a suitable p-type semiconducting layer with a relatively higher carrier concentration than the absorber layer between the absorber and back electrode. Therefore, the voltage generated at the p^+-p junction (passivation layer-absorber junction) creates a barrier to electron current at the rear contact, which results in higher V_{OC} and less recombination at junction and bulk as well. In this context, we propose to insert a p-type SnS layer as a passivation layer or electron-blocking hole transport layer (HTL) between the CTSe absorber layer and back-electrode. SnS is selected as the HTL because it has a similar material composition

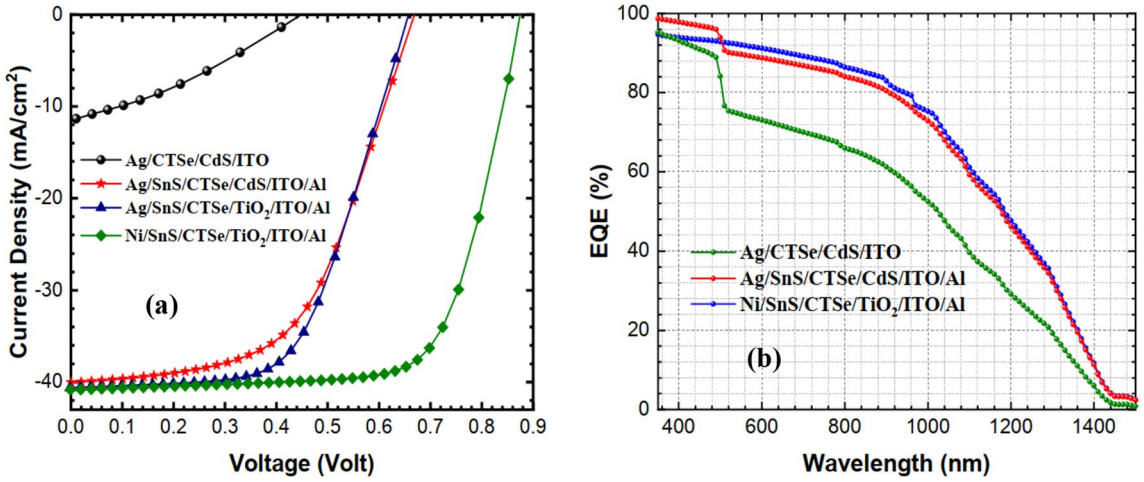

Fig. 1 (**a**) J-V characteristics of *Basic* CTSe-based solar cell, *C-1*, *C-2* and *C-3* cell with the device structure of (Ag/CTSe/CdS/ITO), (Ag/SnS/CTSe/CdS/ITO/Al), (Ag/SnS/CTSe/TiO_2/ITO/Al) and (Ni/SnS/CTSe/TiO_2/ITO/Al) respectively, (**b**) External quantum efficiency (EQE) spectra of CTSe-based solar cells with different cell configuration as indicated on the graph.

as CTSe, suitable p-type properties and is easy to synthesize by various methods [53]. At present, CTSe thin films are directly fabricated on the Mo-coated substrates, where Mo/CTSe interface suffers from poor stability, the formation of MoS_2 layer and voids. A comparative study reported by Chen et al. [54] concluded that inserting the SnS buffer layer instead of ZnS and CuS can show less interfacial defects, no secondary phase and improved crystal quality of CZTS films. The added SnS layer reacts with secondary phases such as CuS that may be formed during the CZTS film fabrication process, which greatly inhibits the formation of these secondary phases in the CZTS absorber layer [55]. Since CZTS and CTSe are very similar material systems, we assume that SnS may also be a suitable HTL for CTSe-based solar cells. The J-V characteristics of the modified cell (*C-1* cell) with the configuration of (Ag/SnS/CTSe/CdS/ITO/Al) is presented in Fig. 1a and the values of PV performance parameters are listed in Table 4. The difference in PV performance parameters between the standard cell and the modified cell (*C-1* Cell) is striking (see Fig. 1a). The average PCE of the standard cell is 1.66%, while *C-1* cell showed the PCE of 14.67%. The significant increase in efficiency is due to the increase in V_{OC} from 449 to 669 mV, FF from 32% to 54.8% and J_{SC} from 11.53 to 40 mA/cm^2. Therefore, the J-V analysis shows that it is beneficial to insert SnS into the standard cell structure as HTL and can produce devices with better PV performance in terms of V_{OC}, FF and J_{SC}. After the insertion of SnS HTL as a passivation layer, due to the lower interface recombination, the increase in the V_{OC} value in the device is expected and well known [56, 57]. In particular, this increase in V_{OC} may be attributed due to the suitable band offset between SnS and CTSe absorber and generation of built-in potential at both ends of the absorber layer and hence reduces minority carrier recombination at the SnS/CTSe interface. The improvement of the J_{SC} of the *C-1* cell is attributed to the existence of the direct electric field induced by the SnS layer, which allows the charge to flow in the absorption layer.

Interface defects and cliff conduction band offset (CBO) in CTSe/CdS interface [58] as well as large spike CBO can adversely affect device performance. Moreover, due to the toxicity of Cd in CdS and light absorption at near 520 nm, which leads to the optical loss, alternative ETL with $E_g > 2.42$ eV should be investigated [59]. Therefore, as we proposed earlier that n-type TiO_2 with $E_g = 3.26$ eV could be a promising ETL for the CTSe-based solar cells due to its suitable band alignment with CTSe. Figure 1(a) shows the J-V curve of the *C-2* cell of the device configuration of (Ag/

Table 4 PV performance parameters for different cell configurations

Cell Configuration	V_{OC} (Volt)	J_{SC} (mA/cm^2)	FF (%)	PEC (%)	Device ID
Ag/CTSe/CdS/ITO	0.449	11.53	31.99	1.66	*Basic Cell*
Ag/SnS/CTSe/CdS/ITO/Al	0.669	40.01	54.81	14.67	***C-1***
Ag/SnS/CTSe/TiO_2/ITO/Al	0.660	40.61	58.84	15.71	***C-2***
Ni/SnS/CTSe/TiO_2/ITO/Al	0.876	40.84	70.93	25.39	***C-3***

SnS/CTSe/TiO_2/ITO/Al), where the CdS layer in *C-1* cell is replaced by the TiO_2 ETL layer. The solar cell (*C-2* cell) with TiO_2 as ETL exhibited slightly enhanced PV performances as shown in Table 4. As shown in Table 4, the *C-2* solar cell using TiO_2 as the ETL showed a slightly enhanced PCE of 15.71%. The V_{OC} of *C-1* and *C-2* cells are the same. Regarding the FF and J_{SC} values, the 7% difference in FF and the 0.60 mA/cm^2 difference in J_{SC} between the *C-1* and *C-2* cells can undoubtedly be attributed to the effect caused by replacing the CdS layer with a TiO_2 layer. The increase of FF signifies the decrease of the series resistance of the cell with this replacement. Therefore, replacing CdS with TiO_2 ETL in the structure can significantly improve the PV performance of solar cells.

3.2 Effect of back contact metal work function on PV performance of CTSe-based solar cells.

The back-contact material has a great influence on the performance of the solar cell. Molybdenum (*Mo*) is a metal back contact, suitable for CIGS solar cells, but not for Kesterite, because the chemical stability of the *Mo*/Kesterite interface is not stable as shown by thermodynamic analysis [60]. Therefore, in spite of the fact that *Mo* has been broadly utilized as the standard back contact material in kesterite devices, it ought to be re-examined. To investigate systemically the influence of the electron work function of the metal on the rear contact, its value was changed in the range from 4.9 to 5.4 eV in the simulation and the normalized PV performance parameters are illustrated in Fig. 2. As shown in the figure, by increasing the back contact metal work function from 4.9 eV to 5.2 eV, an amazing improvement in solar cell parameters was found. All PV

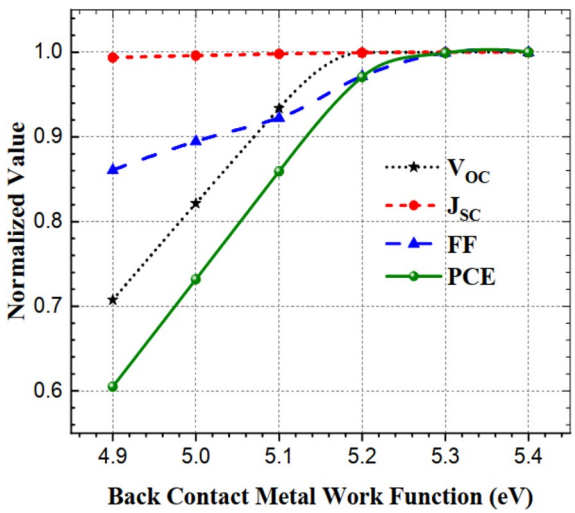

Fig. 2 Variation of normalized PV performance parameters of CTSe-based solar cells as a function of back contact metal work function.

performance parameters except J_{SC} (J_{SC} is almost constant) show similar trends, initially increasing with the increase of the metal work function and above the critical metal work function (5.2 eV), these parameters indicate saturation behavior. This is due to the fact that as the metal work function increases, the barrier height for majority charge carriers (holes) at the back contact interface decreases, which reduces the interfacial recombination of charge carriers. As a result, V_{OC} improves, while the J_{SC} remains almost unchanged, thereby improving the performance of the device. These results suggest that back contact metal work function of above 5.2 eV is required for better performance of CTSe-based solar cell. Therefore, metals with high work functions (such as Au, Ir, Ni and W) could be used as back contact material to obtain the highest PCE from CTSe solar cells. In this regard, we recommend to use Ni (111) with the work function of 5.35 eV as back contact materials for the high performance CTSe-based solar cells. Finally, we propose a high performance CTSe-based solar cell (*C-3*), where the back contact materials of *C-2* cell is replaced by Ni (111). The J-V characteristics of the final solar cell is shown in Fig. 1(a). Figure 1(b) shows the EQE spectra of CTSe-based solar cells with different device structure. For the *Basic cell*, EQE below 520 nm is quite high, which is due to higher absorption of photon by CdS layer (Eg = 2.42 eV), whereas the poor EQE is observed at the longer wavelength region. The impact of SnS electron blocking transport holes layer on the EQE spectra is clearly observed; EQE in the longer wavelength region is significantly enhanced. The proposed cell (*C-3* cell) exhibits improved EQE among the other cells. The *C-3* cell exhibited very good PV performance of V_{OC} = 0.88 V, J_{SC} = 40.8 mA/cm^2, FF = 71% and PCE of 25.4%, as listed in Table 4. Figure 3(a) shows the planar device structure of the proposed final solar cell. Here, substrate type device structure is used and the selection of the stacked structure of the heterojunction device is mainly determined by proven technological feasibility and successes in CIGSSe and CZTSSe solar cells. CTSe, TiO_2 and SnS, which are the absorber, ETL and HTL, respectively, formed the heterojunction and constitute the key parts of the device.

When the potential of the conduction band minimum (CBM) of the buffer ETL is lower in potential than that of the absorber layer, the potential difference that may occur between the quasi-Fermi level of the p-type absorber layer and the n-type ETL under illumination is reduced. This brings down the V_{OC} that can be generated. This band alignment also results in an energy barrier to the electron flow under forward bias, thereby increasing the recombination rate at the absorber/ETL interface. Such a band alignment at the p–n junction is called a *cliff CBO*, which reduces R_{sh} and FF. The band alignment which is convenient to the V_{OC} is the spike CBO, in which the CBM

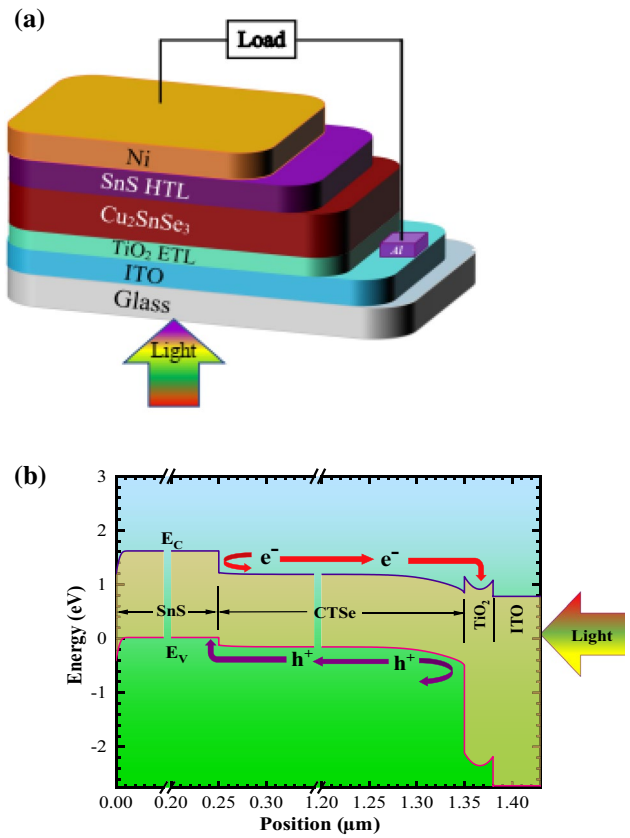

Fig. 3 (**a**) schematic diagram and (**b**) energy band diagram of the (Al/ITO/TiO_2/CTSe/SnS/Ni) heterojunction solar cell.

of the ETL is a little higher in potential than that of the absorber layer. Theoretical analysis shows that with the increase of spike CBO, the change of V_{OC} is small [61]. It has also been calculated that the optimum spike CBO between the absorber and buffer layer is between 0 to 0.4 eV [61], beyond this level, higher barriers can reduce current flow and hence efficiency. The simulated energy band diagram of the proposed *C-3* cell with novel structure of (Ni/SnS/CTSe/TiO_2/ITO/Al) heterojunction solar cells is shown in Fig. 3b. It can be seen from the figure that the conduction band of the CTSe absorber layer is lower in potential than that of TiO_2 ETL and the small spike CBO between them is + 0.2 eV, which makes it easy for photo-electrons to transport through the ETL and into the collection electrode. Photo-generated holes cannot enter the TiO_2 ETL as it is observed that the energy of the valence band of the TiO_2 ETL is much lower in potential that that of the CTSe absorber. Therefore, n-type TiO_2 establishes a suitable junction with CTSe absorber layer to transport photo-generated electrons to ITO through TiO_2, whereas holes are blocked at TiO_2 layer. An effective hole transport layer (HTL) should have the properties as opposite to that of ETL. The valence band maximum (VBM) energy should closely match with the valence band of the absorption layer. It is seen from Fig. 3b that the VBM energy of the SnS HTL is slightly higher than that of the CTSe absorber, so the photo-generated holes from the CTSe layer can be effectively transferred to the back electrode through the SnS HTL. The conduction band energy of the SnS HTL is suitably larger than that of the CTSe absorption layer (spike CBO = + 0.34 eV), so the photo-generated electrons are blocked from the CTSe to the back electrode by this barrier at SnS HTL. Therefore, SnS and CTSe form a suitable junction to transport holes to the back electrode through the SnS HTL and it prevents electrons from reaching the back electrode.

3.3 Effect of absorber layer thickness and carrier concentration on the cell PV performance

The challenge in the field of TFSCs is to produce ecof-riendly, cost-effective solar cells with high PCE with very thin absorber layers. The absorber layer thickness and carrier concentration are the key choices for structuring the TFSCs, as it is generally influencing the photo-generated excitons and charge carrier extraction. Therefore, the optimization of the carrier concentration and thickness of the absorber layer is crucial in achieving optimum cell performance. The simultaneous effect of absorber layer carrier concentration and thickness on the PV performance of the novel (Ni/SnS/CTSe/TiO_2/ITO/Al) heterojunction solar cells was investigated, as shown in Fig. 4. The initial values of thicknesses, defect density and carrier concentration of the TiO_2 ETL were set to 30 nm and 10^{16} cm^{-3} and 10^{18} cm^{-3}, respectively. While the same parameters for the SnS HTL were set to 200 nm and 10^{16} cm^{-3} and 10^{19} cm^{-3}, respectively. To rationalize the simulation, the CTSe thickness and carrier concentration were varied from 500 to 3000 nm and 10^{14} to 10^{18} cm^{-3}, respectively. As observed in Fig. 4, for lower carrier concentration (< 10^{15} cm^{-3}) of the absorber, an increase in the CTSe absorber layer thickness yields a systematic effect of reducing V_{OC}. On the other hand, the increase in the carrier concentration of CTSe layer from 10^{14} to 10^{17} cm^{-3} resulted in a significant increase in V_{OC}. This is due to the decrease in reverse saturation current as the carrier concentration increases, thereby increasing V_{OC}. Beyond this carrier concentration of the absorber, V_{OC} starts to decrease again. It can be seen from Fig. 4 that the contour area of the highest J_{SC} extends in the region with the highest thickness and lowest acceptor concentration of the absorption layer (bottom-right). The device can produce high J_{SC} with acceptor carrier concentration as low as 10^{15} cm^{-3} and a minimum absorber layer thickness of 2000 nm. The increase of J_{SC} as the thickness of CTSe increases is attributed to the increase in the absorption of long wavelength photons in this layer. As the acceptor

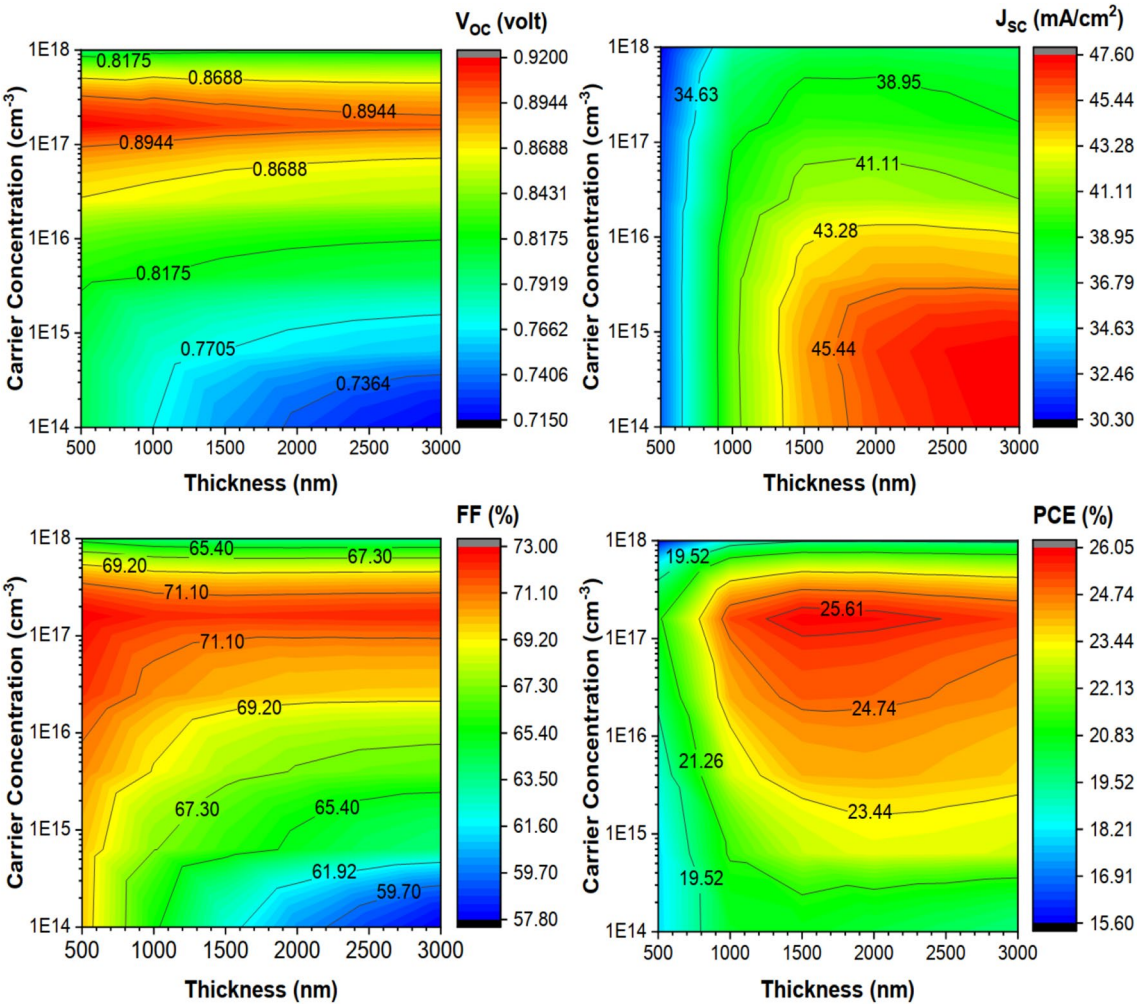

Fig. 4 Concurrent effect of thickness and carrier concentration of absorber layer on the PV performance of CTSe-based solar cell

carrier concentration increases, the lifetime of photogenerated electrons is shortened, reducing the carrier collection at interface, so J_{SC} decreases. Moreover, at carrier concentrations higher than 10^{15} cm^{-3}, the J_{SC} collection should be reduced due to the smaller width of the depletion layer. At lower acceptor concentration, the FF slightly decreased with CTSe layer thickness, which is due to the increase of series resistance of the device. The height contour area of FF is found at the relatively lower thickness and acceptor carrier concentration of about 10^{17} cm^{-3}. It was observed in Fig. 4 that the device is capable of producing high PCE of > 25% at a carrier concentration ranging from 5×10^{16} to 5×10^{17} cm^{-3} and at a thickness > 1500 nm. From this study, a maximum PCE of 26% was found at the carrier concentration of 5×10^{17} cm^{-3} with a CTSe-absorber layer thickness of 1500 nm. High CTSe layer carrier concentration ($>5\times10^{17}$ cm^{-3}) induces a detrimental effect on the overall performance of the device, which might be due to the increase of Auger recombination. Interestingly, an

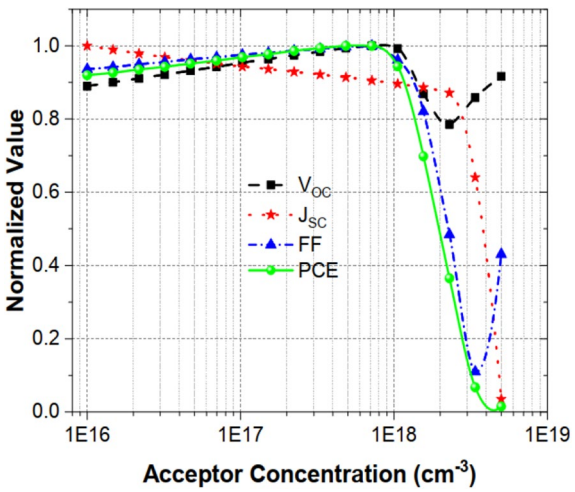

Fig. 5 Normalized values of all the PV performance parameters as a function of acceptor concentration of CTSe layer

abrupt transition of all the PV performance parameters is observed at the onset of a carrier concentration of 5×10^{17} cm^{-3}, shown in Fig. 5. Normalized values of all PV performance parameters of the novel solar cell as a function of the acceptor concentration of the CTSe layer are depicted in Fig. 5. According to semiconductor theory, as the carrier concentration of semiconductor increases, the semiconducting properties deteriorate, which is one of the main problem that limits the higher value of carrier concentration in semiconductor. According to the "Mott transition" theory [62], the observed sharp transition of all photovoltaic performance parameters from higher to lower values can be well explained. After a certain doping level, the semiconductor enters into the metallic conductive state by losing its semiconductor characteristics. However, the carrier concentration of the absorber layer has the most noticeable influence on the electric field at the interfaces, as shown in Fig. 6, which is the key parameter for separating and collecting photogenerated carriers. The most observable impact of absorber carrier concentration on the electric filed of the CTSe/TiO_2 interface is the reduction of the width of the space charge region, while at the SnS/CTSe interface both the electric field intensity and the width of space charge region reduces abruptly above the concentration of 5×10^{17} cm^{-3}. The reduction in the width of the space charge region at both interfaces and the field strength at the SnS/CTSe interface should degrade photogenerated carrier separation and collection significantly. Moreover, a higher value of acceptor concentration corresponds to an increase in the carrier recombination in the bulk region, thereby also reducing J_{SC}.

3.4 Effect of CTSe absorber layer defects on cell performance

The optoelectrical properties of materials can change due to defects present in the material system. Therefore, it is important to study the influence of defect density of the absorber layer in various absorber layer thickness, as defects at the absorber layer of solar cells are unfavorable for its performance. In this simulation, we introduced only single deep-level donor like defects state in the CTSe layer due to the fact that the formation energy acceptor defects are lower than donor ones [24]. Figure 7 presents the concurrent effect of defects density and thickness of absorber layer on the solar cell performances. The effect of defect density from 10^{16} to 10^{19} cm^{-3} and thickness from 500 to 2000 nm are analyzed to assess the performance of the device. It is observed from Fig. 7 that the V_{OC} of the novel (Ni/SnS/CTSe/TiO_2/ITO/Al) heterojunction solar cells does not change with the thickness of the CTSe layer, but the defect density of the CTSe layer has the adverse effect of reducing V_{OC} from 0.93 V to 0.57 V as the defect density changes from 10^{16} to 10^{19} cm^{-3}. The FF follows the same behavior as the V_{OC}. In contrast, J_{SC} shows a maximum value of > 38 mA/cm^2 at thicknesses and defect densities of, > 1500 nm and < 10^{16} cm^{-3}, respectively. Decreasing the thickness from 2000 to 500 nm causes the J_{SC} to drop by 8.0 mA/cm^2 and a decrease in J_{SC} can also be observed at defects > 10^{17} cm^{-3}. Conclusively, when the thickness is > 1500 nm and the defect density is < 1.2×10^{16} cm^{-3}, the highest observed PCE is > 26%. All the above findings suggest that the defect density of the absorber layer has an adverse effect on the performance of CTSe solar cells. We found that increasing the thickness of the absorber layer can partially alleviate this problem.

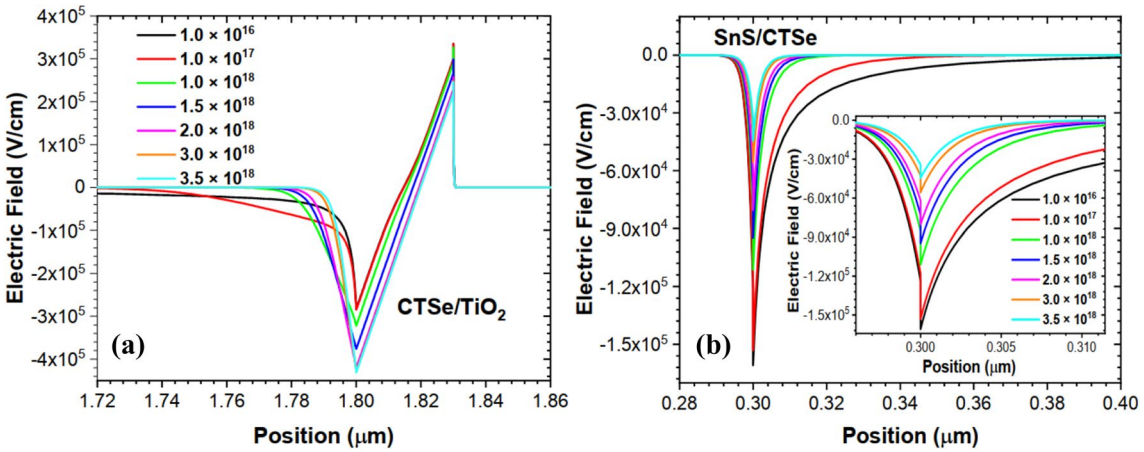

Fig. 6 Effect of acceptor concentration of the absorber layer on the electric field (**a**) at the CTSe/TiO_2 interface and (**b**) SnS/CTSe interface.

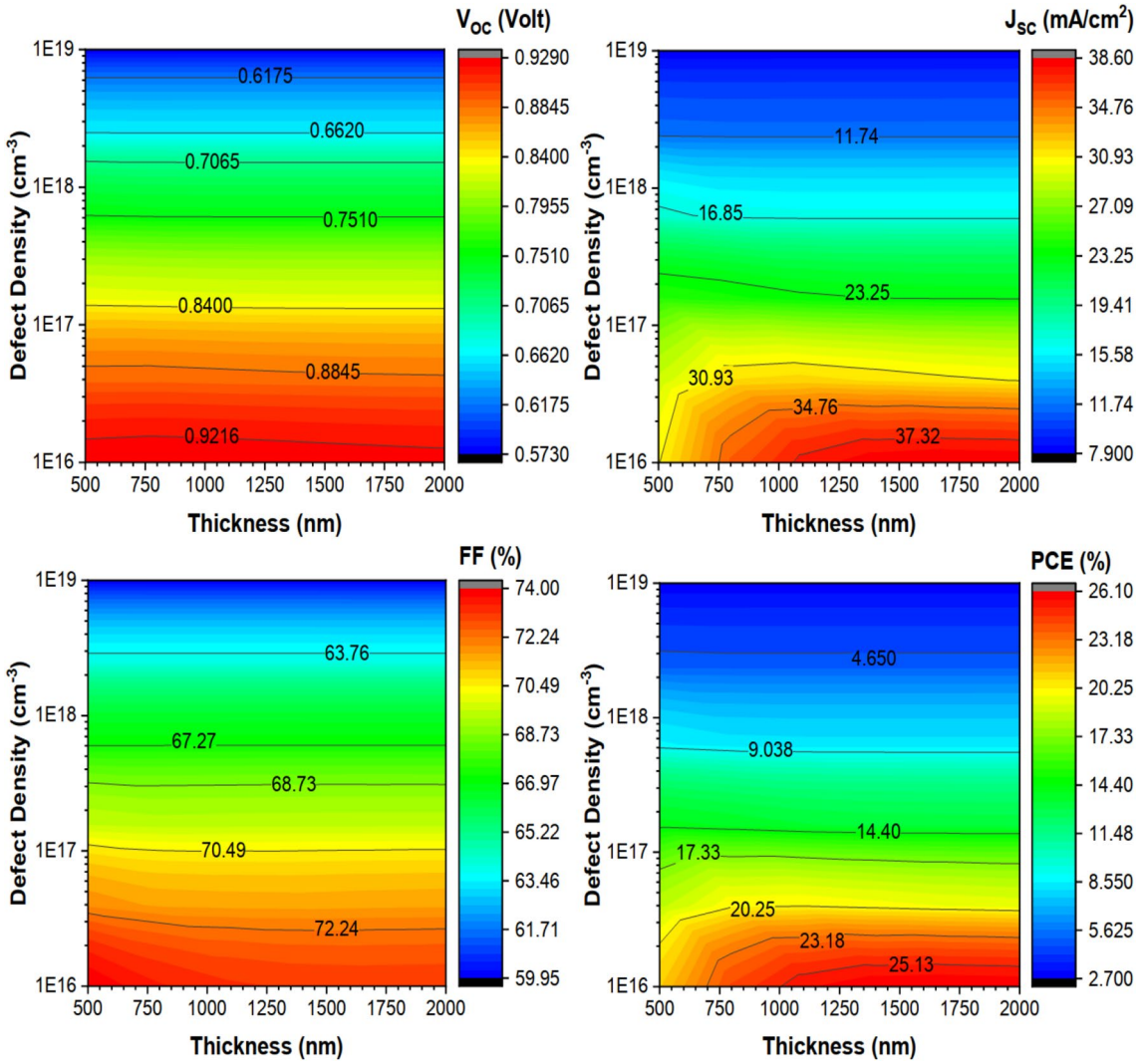

Fig. 7 Variation of PV performance parameters with defect density and thickness of the absorber layer in CTSe solar cells.

3.5 Effect of SnS HTL thickness and carrier concentration on the cell performance

In order to study the simultaneous influence of SnS HTL thickness and carrier concentration, the structure shown in Fig. 3a was simulated. The thickness and carrier concentration of the SnS layer were varied from 100 to 600 nm and 10^{16} to 10^{20} cm^{-3}, respectively. A fixed CTSe layer thickness of 1500 nm is used for the first step of the simulation. A single deep-level donor type defects states with a defect density of 10^{16} cm^{-3} was introduced in the SnS layer [63]. Figure 8 shows the changes in solar cell PV performance parameters due to SnS layer thickness and carrier concentration. As it can be seen from Fig. 8 that the PV parameters such as V_{OC}, J_{SC} and PCE exhibit similar behavior with SnS layer thickness and carrier concentration. The aforesaid parameters were hardly changed with the thickness of the SnS layer, but increased with the increase of the SnS layer carrier concentration. In particular, V_{OC} increased with the carrier concentration of SnS HTL, indicating a decrease in photo-generated charge carrier recombination. It is found that J_{SC} and therefore PCE increase with the increase of carrier concentration but independent of thickness. At SnS HTL carrier concentrations > 10^{19} cm^{-3}, the maximum PCE was found to be > 27%. On the contrary, the contour area for the highest FF is found at lower carrier concentration and thickness of SnS HTL (bottom-left). FF decreases with the decrease of carrier concentration and thickness, indicating that the series resistance of the cell increases with the increase of SnS HTL carrier concentration and thickness.

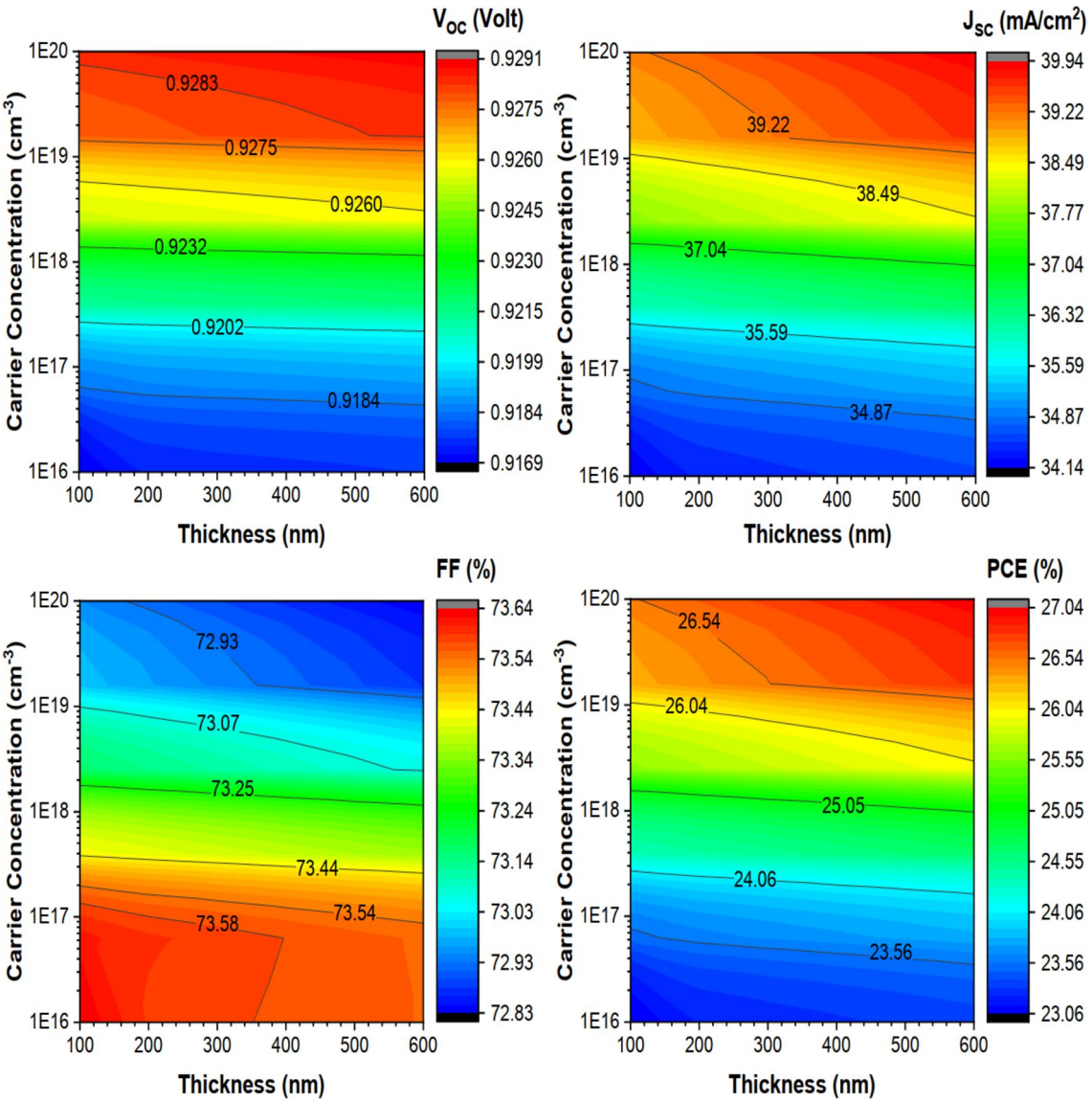

Fig. 8 Variation of PV performance parameters of CTSe solar cells due to SnS layer thickness and carrier concentration

3.6 Effect of TiO_2 ETL thickness and carrier concentration on the cell performance

In TFSCs, an appropriate ETL is required to obtain high V_{OC}. The resistive nature of the ETL may limit the amount of current that flows into a smaller localized area and drives the filament or shunt formation process, thereby improving PV performance. Moreover, in order to obtain a higher V_{OC} value as stable as thicker cells, TFSCs with a lower carrier mobility absorber need more buffering [64]. The concurrent effect of TiO_2 ETL thickness and carrier concentration on cell performance was investigated, as it is important in terms of stability and performance of the device and presented in Fig. 9. The thickness of ETL was considered to be thinner than the other layers, whereas, the ETL with relatively high carrier concentration was adopted for this study. The carrier concentration and thickness of the TiO_2 ETL was varied from 10^{16} to 10^{20} cm^{-3} and 20 to 60 nm, respectively. The thickness and carrier concentration of CTSe absorber and SnS HTL were fixed at 1500 nm, 300 nm and 5×10^{17} cm^{-3}, 10^{19} cm^{-3}. A single deep-level acceptor-type defects states with a defect density of 10^{16} cm^{-3} was also introduced in the TiO_2 layer. It can be clearly seen from Fig. 9 that at a lower TiO_2 carrier concentration ($<10^{18}$ cm^{-3}), the cell performance is very poor and all PV parameters of the device behave in the same way, rapidly decreasing with increasing TiO_2 thickness. However, the PV performance of the device remained unchanged and independent of thickness when the TiO_2 carrier concentration was $>10^{18}$ cm^{-3}. This improvement of the PV performance

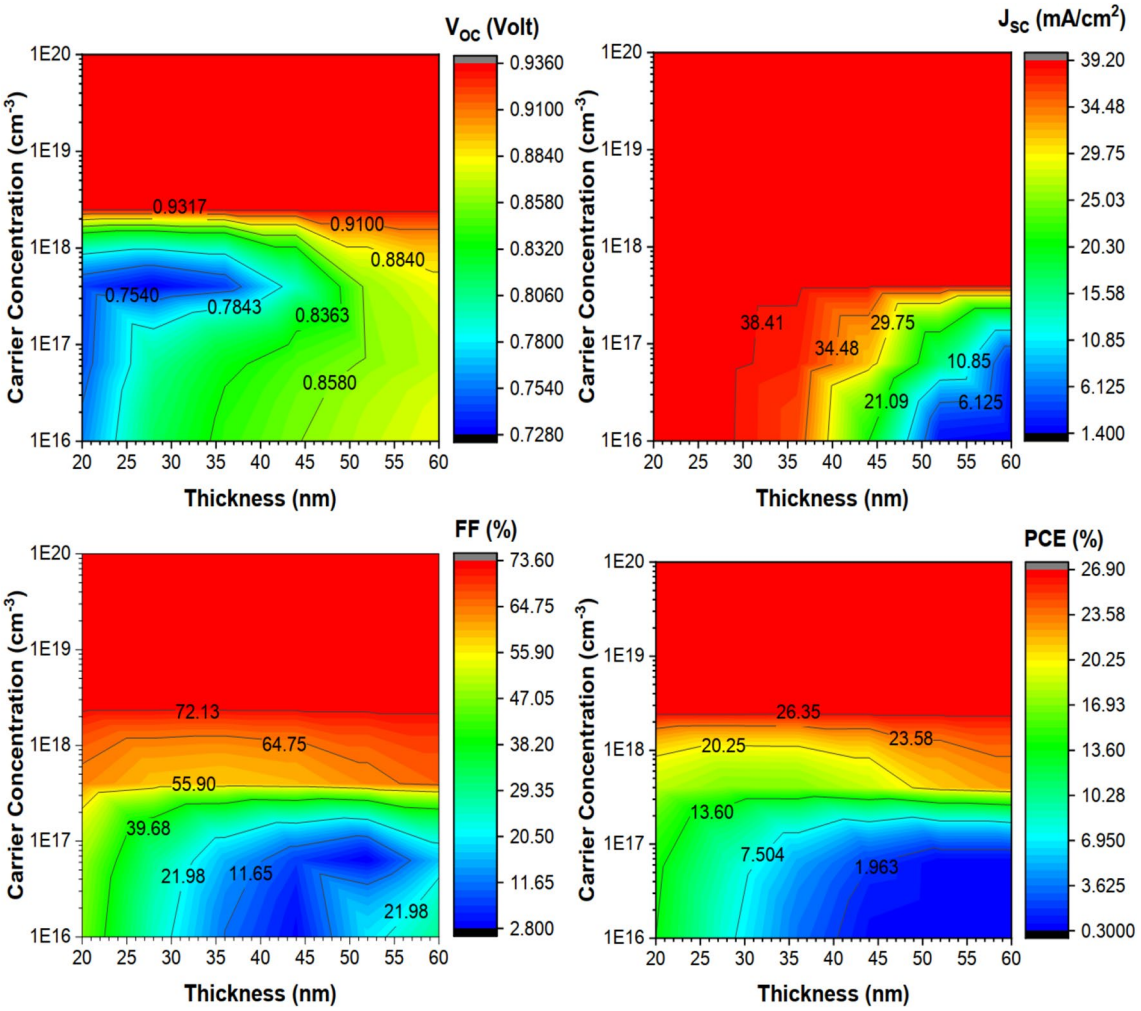

Fig. 9 Variation of PV performance parameters of CTSe solar cells due to TiO_2 layer thickness and carrier concentration.

of the device can be ascribed to the decrease of recombination of the minority charge carrier and series resistance with the increase of TiO_2 carrier concentration. In the study, maximum PCE was observed at a very thin layer of TiO_2 and carrier concentration of $> 10^{18}$ cm^{-3}. However, it is too hard to deposit a very thin ETL layer but it is practicable to achieve a thickness of 30 nm which will work better.

3.7 Effect of temperature on the cell performance

The important role of operating temperature with respect to the electrical efficiency of PV devices has been fully established and documented, as it has received much attention from the scientific community. Therefore, it is very important to study the temperature behavior (T) of solar cells, as in applications they are usually exposed to a temperature range of 288 K to 323 K [65] and even higher temperatures in the desert during the summer period [66], in space and concentrator systems [67]. In this section,

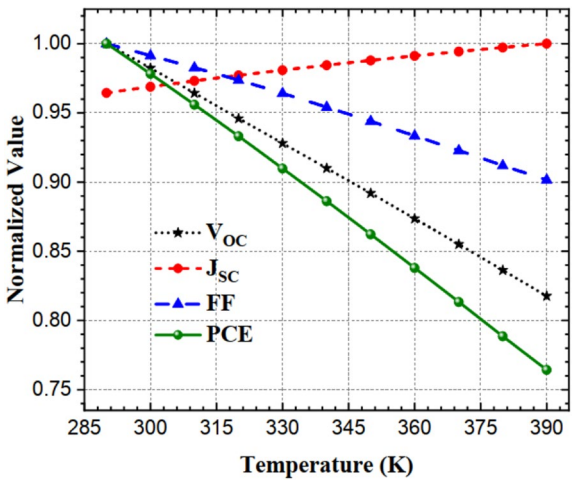

Fig. 10 Normalized values of all the PV performance parameters of CTSe-based solar cells as a function of working temperature

PV performances of our proposed solar cells have been achieved in the temperatures ranged between 290 and 390 K and the results are shown in Fig. 10. In this simulation process, all the variable parameters of CTSe solar cells are taken as the optimized value obtained previously. In Fig. 10, the normalized values of all the PV performance parameters of CTSe-based solar cells as a function of working temperature are presented. There was a significant linear decrement of V_{OC}, FF and PCE, accompanied by a slight increment in J_{SC} value, see in Fig. 10. As the operating temperature increases, the reverse saturation current increases due to increased internal carrier recombination rates caused by increased carrier concentrations, ultimately reducing V_{OC} [68, 69]. At the same time, the small increase in J_{SC} is due to the decrease of the band gap with increasing temperature. Also, the increase of the working temperature of the cells affects the material conductivity by increasing the scattering of charge carriers with thermally activated phonons, which in turn decrease the PV performance of the solar cells. As a result, a linear decay of PCE is observed as the temperature increases from 290 to 390 K. Under standard test conditions (STC-298 K), the temperature coefficient C_T (%K^{-1}) of PCE is defined as [70]

$$C_T = \left(\frac{1}{\eta_{STC}} \frac{d\eta_T}{dT} \times 100\% \right) \quad (1)$$

where, η_{STC} is the cell efficiency at STC and η_T is the efficiency at any temperature T. Using the equation (1), it is found that the C_T of PCE of the cell is − 0.237%K^{-1}, indicating the thermal stability of the solar cell is good enough for outdoor installation.

4 Conclusions

Suitable optoelectrical properties of CTSe firmly indicate that it can replace the scarce elements of CIGS absorbers and highly complicated stoichiometric elements based CZTS in solar cell. In this study, the PV performance of CTSe-based multi-junction solar cells with the (Ni/SnS/CTSe/TiO_2/ITO/Al) device structure was studied from the perspective of numerical simulation. The simulation revealed that the highest efficiency of single junction CTSe/CdS (excluding SnS-HTL) solar cell reached to 1.66%, which is comparable to the reported experimental data in literature. By introducing an SnS layer between the absorber and the back electrode as an electron-blocking HTL, the efficiency of the solar cell is increased to 14.67%. This study also showed that the replacement of CdS buffer layer, which is toxic and causes optical loss in visible range, with TiO_2 ETL to the heterostructure further improved the PCE to 15.71% of the CTSe based solar cells. The back contact metal work function plays a vital role in CTSe-based solar cells. After studying the effect of the back-contact work function on the cell performance, it is found that in order for the device to work at maximum performance range, at least the back-contact materials with a work function of 5.2 eV is required. By optimizing the appropriate absorber layer, ETL and HTL thickness, carrier concentration and replacing back contact metal (*Mo*) with *Ni* (111), it is found that the efficiency of CTSe based thin film devices could further be enhanced to 27%, which exceeds the commercial benchmark level. Based on optimized data, the optimum PV performance of the solar cell is achieved for CTSe, SnS HTL and TiO_2 ETL layer thicknesses of 1500, 300 and 30 nm with the carrier concentrations of 5×10^{17}, 1×10^{19} and 1.2×10^{18} cm^{-3}, respectively, at a temperature of 300 K. Also, the effect of the operating temperature on the performance of the CTSe solar cell structure was investigated from 290 to 390 K. The proposed novel structure showed very good PV performance stability on elevated temperature with the temperature coefficient of PCE is − 0.237%K^{-1}. The findings of this contribution accentuate the prospect of the cadmium-free CTSe-based heterojunction solar cells in thin film PV industry as the next generation thin film PV device.

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Compliance with ethical standards

Conflict of interest The author declares no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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