Research Article

# Temperature impact on reliability of power RF devices under S-band pulsed-RF test

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**Abstract**
This paper presents an innovative reliability bench of aging life tests designed to high power RF applications for device lifetime under pulse conditions. The temperature effect on the parameters of power RF LDMOS (Radio Frequency Laterally Diffused-Metal–Oxide–Semiconductor) devices is highlighted. Indeed, the acceleration of the degradation mechanisms is related, directly or indirectly, to the temperature variation. The tests carried out on the power amplifier will be "Life-test RF" type (accelerated aging under constant constraints) over a period of 1500 h to quantify the drifts of the parameters measured (mainly $P_{OUT}$ and $I_{DSS}$) under reliability bench life-test at different temperatures. The parameters of devices have been characterized i.e. static, dynamic and RF before and after testing. This allows us to quantify the degradation, of the shift, of a certain number of electrical quantities ($V_{TH}$, $G_M$, $R_{DSON}$, $C_{RSS}$, etc.). The analysis of the physical results has been presented (simulator 2D ATLAS-SILVACO) to explain and observe the physical review of temperature impacts on power RF LDMOS performance. Finally, initial impacts analysis have been discussed.

**Keywords** Reliability · Power RF transistor · Temperature effects · Hot carrier

## 1 Introduction

The huge demand for high performance costs and high effective gives LDMOSFET devices an important place [1]. They have good performances than bipolar and GaAs transistors [1, 2]. Currently, the power RF LDMOS are used in several areas especially on base stations, TV broadcast and in radar systems with high capabilities particularly in terms of output power and Power Added Efficiency (PAE) [3, 4]. Metal Oxide Field Effect Transistors (MOSFETs) are the smost used devices in higher power RF field [3]. They are distinguished many advantages relative to bipolar devices, such as in particular [4, 5]; better linearity, with intermodulation products of smaller amplitude, and these are devices that are better from thermal runaway [1, 6]. The cost of MOSFETs represents a clear advantage over III–V technologies for application rates up to around 4 GHz.

Recently, the characterization, optimization, and reliability of LDMOS devices have drawn much attention [2, 4]. For this purpose, we designed and implemented an innovative reliability bench able to keep monitoring of RF powers, voltages and device basic temperatures where the values correspond to the constraint operating conditions [5, 7, 8]. The duty cycle and pulse length have steadily increased to improve radar performance, from the accession of solid-state power modules in radar system [5]. These important needs for operation have increased the amount of constraint applied to devices and have a direct impact on their lifetime. A study knowledge of temperature impact is important for an improved estimation of modules reliability and of the transistors that compose it

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[4, 7]. The reliability index was formulated on the assumption basis for reliability calculation [9]. For these reasons, a thorough has initiated to improve new methods for investigating the reliability of RF power devices in pulsed radar operating conditions.

This paper discusses the relationship between the shift of electrical parameters and the subsequently-degraded zone in structure in order to improve the performance at the manufacturer. It also describes how to calculate the device MTTF (Mean Time To Failure) and how to intervene before failure especially in critical applications such as radars or planes.

A full electrical characterization (I–V, C–V and RF) has been performed. Therefore, a full review of these critical electrical parameters is exposed and analyzed.

This manuscript is consisting respectively as follows: reliability pulsed life aging bench; power RF LDMOS structure and simulation; experimental study; results and discussion. At the end, the conclusion and the prospects.

## 2 Reliability RF pulsed life test bench

This work presents the temperature impact on the reliability of a RF power device submitted to "Life-test RF" on an innovative reliability bench (Figs. 1, 2) dedicated specifically for this purpose. An RF LDMOS device has chosen dedicated to accelerated life tests. All performance degradation of device electrical parameters after accelerated RF pulsed life test at various temperatures are studied and discussed. From the results analysis, we can see that in lower temperature, the drift is greater of significant electrical parameters.

The reliability bench diagram has been implemented is shows in Fig. 1, which will achieve the objective, namely the estimation of the lifetime of the transistors under operational radar conditions [5]. It contains eight "branches" of

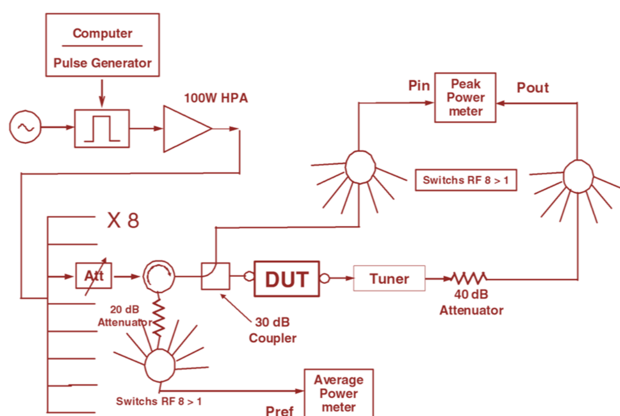



**Fig. 1** Synoptic of a RF power reliability bench in pulsed mode

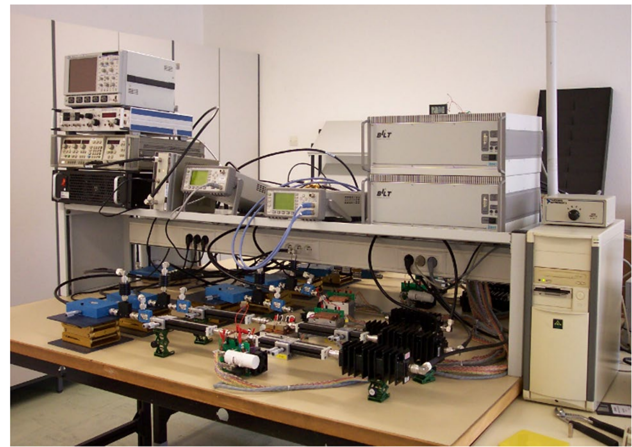


**Fig. 2** Photography of the RF power reliability bench in pulsed mode

tests. This choice of eight transistors to be tested results from a compromise between the complication of bench implementation and the samples necessary number for the measurements representativeness.

This bench is able to keep track of many parameters like voltages, currents, base-plate temperature, and peak power. Eight samples is the bench capacity max to test simultaneously. The Fig. 2 represents the devise under test placed on its test fixture, supplied by DC power and connected to RF connector (type N).

The bench is composed of three interdependent subsets:

- a microwave part,
- a control/command part piloted by PC,
- thermal module for each devices.

The DC, RF and thermal conditions applied to the power RF LDMOS device are the following:

- DC: $V_{DS} = 44$ V, $V_{GS} = 3.79$ V, with $I_{DQ} \approx 3$ mA at 25 °C.
- RF: Pulse Width / Cyclic Ratio = 500 µs/50%. Frequency = 2.9 GHz. $P_{IN} = 30.5$ dBm, $P_{OUT} = 43$-$44$ dBm.
- Thermal: Sole temperature of Peltier effect module equal at 25 °C and 150 °C.

The application allows to save temperature, currents and voltages of gate and drain, the reflective values, the input and output powers. After pulsed RF aging, the device behavior shift under test has been characterized at $T_{am}$ (ambient temperature) and then a parameter set is extracted. The electrical characterization authorize to determine the feedback RF life-tests to any significant parameter shift and better understand the degradation phenomena. The DC conditions correspond to a class B

amplification because the source gate voltage is slightly lower than the threshold voltage of the power RF LDMOS (≈ 4–5 V). The amplifier is aged under pulsed CW operation in radar S band, which results in RF conditions. The frequency of 2.9 GHz is the limit value of the civil radar for S band between 2.7 and 2.9 GHz and is in the middle of the military radar (2.7–3.1 GHz). The both conditions of thermal aging that were chosen to accelerate up the tests are provided and regulated by the thermal modules (Peltier effect). The selection of some temperature stress is founded on an industrial property and others come from the experience acquired over the tests course.

## 3 Simulation and structure of power RF-LDMOS

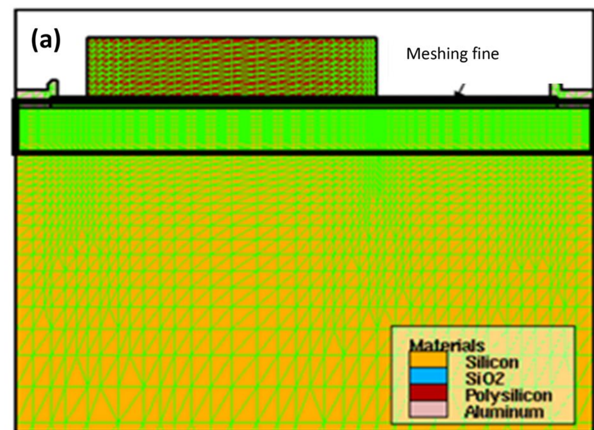
The physical simulations are investigated by ATLAS-SILVACO [10] for locating and confirming the physical phenomena inside the structure. The physics model Monte Carlo [11] has been used to evaluation the hot electrons and the impact ionization. Through this simulation, can it possible to analyse the static and dynamic characteristics. The physical model based on a precise geometric data, doping, carrier equations and material characteristics.

The ATLAS module of SILVACO [10] used to implant and simulate, a modified device structure of a RF N-channel LDMOS which was analysed by Raman et al. [11]. The recapitulation of technological and geometric data used for simulations, are cited in Table 1. The mesh choice is very important of different regions and it is a primary criterion in a numerical model. This choice is a compromise between accuracy and efficiency of the simulation. The mesh used for the simulation presented in Fig. 3a. Critical zones are situated under the gate (channel region and access) and the Dbody diode [12, 13].

The net doping profile along silicon surface presented in Fig. 3b, with all the cited values are "max" values, or high concentration due to the profiles that are implanted. They are all Gaussian type, except on the epitaxial layer concentration which is uniform (Fig. 3b).

Table 1 Device dimensions

| Parameter | Value (µm) |
|---|---|
| Source length | 1.1 |
| Source-gate spacing | 1 |
| Gate length | 0.8 |
| Gate-drain spacing | 3 |
| Drain length | 1.1 |
| Gate oxide thickness | 0.065 |



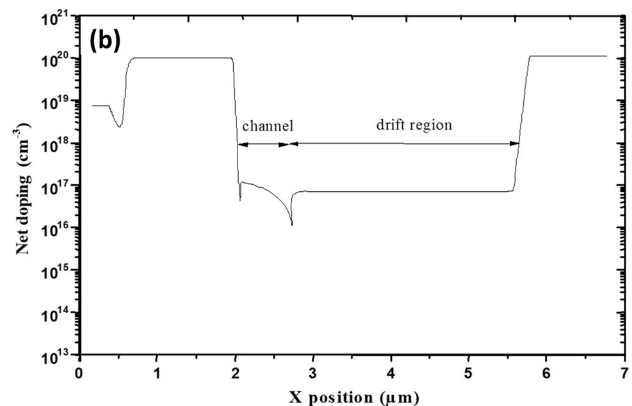




Fig. 3 N-LDMOSFET device implemented in Silvaco-Atlas: Fine mesh visualization (**a**), with net doping profile along silicon surface (**b**)

## 4 Experimental study

This result is founded on the comparison between two components before and after 1500 h of RF aging. Device 1 is aged at room temperature (25 °C) and device 2 at 150 °C. For extract a set of critical electrical parameters, the two transistors have been characterized in static and dynamic area. This work should allow correlating the RF aging for the two different temperatures thanks to the electrical parameter drift. The I–V and C–V measurements were performed at room temperature, respectively by a DC E5270 analyzer and an impedance meter HP 4194, which are driven by Agilent's ICCAP software [14].

### 4.1 DC measurement

In Fig. 4, present the evolution of the threshold voltage after aging test. The source drain current has been reduced at low source drain voltage level (10 mV) is greater at 25 °C than at 150 °C. This influence is often attributed to charge of mobility and trapping at the oxide / semiconductor

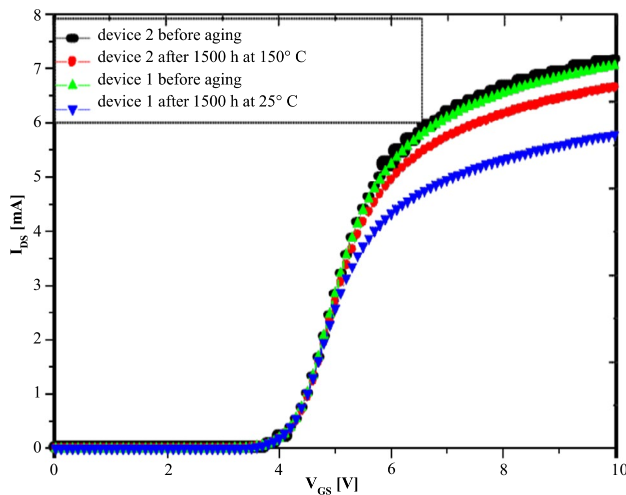



**Fig. 4** Evolution of the threshold voltage after aging, with $V_{GS}$ = [0–10 V] and $V_{DS}$ = 10 mV

**Table 2** Summary of parameter changes electrical DC after aging at 25 °C

| Device 1 at 25 °C | $V_{TH}$ (V) | $G_M$ (S) | $ID_{SAT}$ (mA) | $R_{DSON}$ (Ω) |
|---|---|---|---|---|
| Before aging | 4.19 | 0.53 | 240 | 1.42 |
| After aging | 4.14 | 0.52 | 200,200 | 1.74 |
| Variation in % | −1.2 | −1.9 | 16.6 | +22.5 |

**Table 3** Summary of parameter changes electrical DC after aging at 150 °C

| Device 2, 150 °C | $V_{TH}$ (V) | $G_M$ (S) | $ID_{SAT}$ (mA) | $R_{DSON}$ (Ω) |
|---|---|---|---|---|
| Before aging | 4.17 | 0.54 | 231 | 1.4 |
| After aging | 4.14 | 0.53 | 221 | 1.52 |
| Variation in % | −0.72 | −1.8 | −4 | +7 |

interface [1, 6]. For the threshold voltage, it has not shifted significantly by these two temperatures. After an aging of 1500 h, the $I_{DQ}$ quiescent current remained identical, namely 2.79 mA. This current is depends heavily on the threshold voltage level [15]. Therefore, this confirms that the threshold voltage parameter has not substantially drifted and that the integrity of the gate oxide is not affected (no failure catastrophic).

Tables 2 and 3 show that the threshold voltage and transconductance have not practically not varied, regardless of the thermal condition used during the tests. Consequently, this type of "Life-test RF" has no effect in degradation mechanism of these two DC indicators. On the other hand, as the constraint thermal increase, the percentage change of IDSAT and RDSON decreases. In other words, for the temperature 150 °C, IDSAT and RDSON evolve less than 10%. For the temperatures 25 °C, the two DC indicators vary from minus 15%. This can be thought a signature of a notable degradation mechanism.

## 4.2 AC measurement

In Fig. 5, device 1 exhibited a significant decrease in Miller capacity ($C_{RSS}$) after aging at 25° C, $C_{RSS}$ is defined by two capacitors in series, the capacity oxide ($C_{OX}$) and drifting region capacity ($C_{SI}$) (Fig. 6). The mathematical relationship is as follows [16]:

$$C_{RSS} = \frac{C_{OX} \cdot C_{SI}}{C_{OX} + C_{SI}} \quad (1)$$

Moreover, the cross-section regarding the power RF LDMOS (Fig. 6) device used in this study was implemented and simulated with ATLAS-SILVACO in order to explain qualitatively electrical parameter shifts [12, 13]. Figure 6 shows the device's structure with approximate doping wells. The device recommended structure is a Gaussian

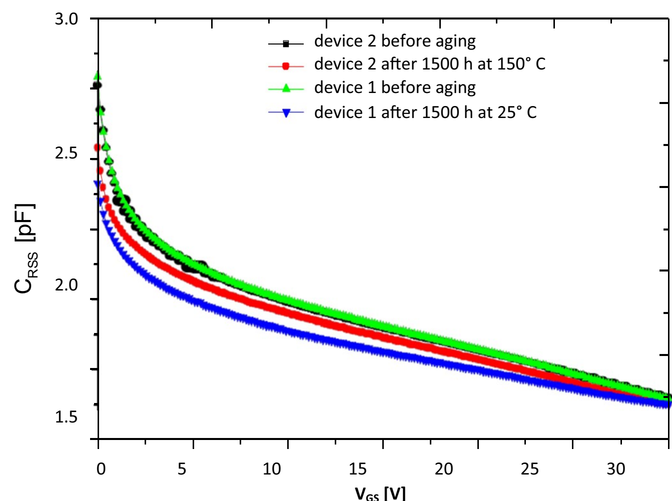



**Fig. 5** Experimental curves of $C_{RSS}$, with $V_{GS}$ = 0 V and Freq. = 1 MHz

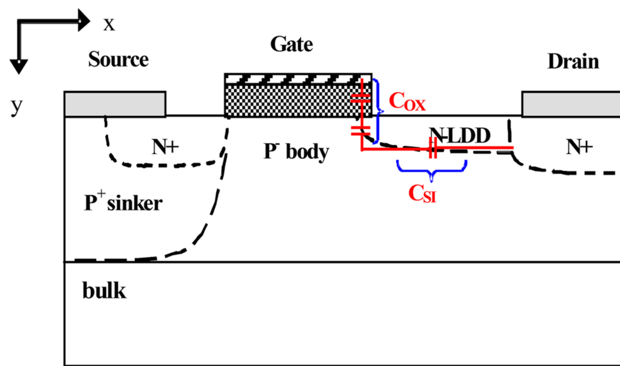



**Fig. 6** Cross-section view of RF LDMOS device implemented in Silvaco-Atlas, with its intrinsic capacitances

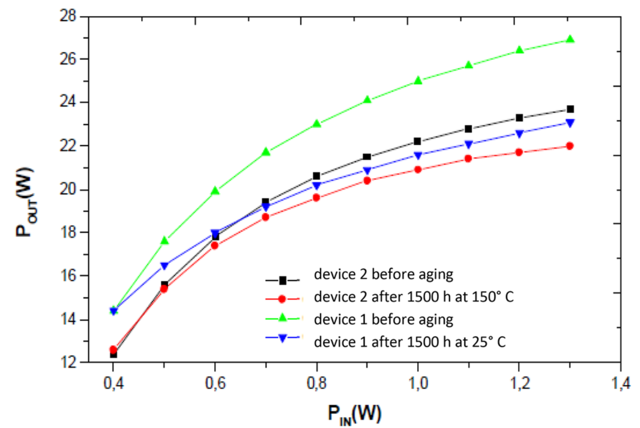



**Fig. 7** Evolution of $P_{OUT}$ measured versus $P_{IN}$ after aging

doping profile model along the channel surface and the LDD area. The doping profile has been optimized with a technological process 2D simulation carried out by SSUPREM3 [12].

For LDMOS power RF devices, the Miller capacitance value at zero volts is mainly caused by the oxide capacity [17]:

$$C_{RSS} \approx C_{OX} \text{at } V_{DS} = 0\,\text{V} \tag{2}$$

The device 1 experienced a strong shift of $C_{RSS}$ profile, in particular at zero $V_{DS}$ (Fig. 5). In the other hand, device 2 exhibited almost two times less $C_{RSS}$ offset at zero $V_{DS}$ (Tables 4 and 5) than device 1.

A summary in table form presents the shifts each AC parameters to conclude in a way quantitative of analysis capacitive state of the samples after aging at 25 °C and 150 °C. Miller capability at 0 V or at 26 V decreased sharply (by at least 15%) regardless of the thermal stress (Tables 4 and 5). The significant decrease is that obtained after the aging test at 25 °C. Two elements notables can also be reported: first, the capacity intrinsic input ($C_{ISS}$) has not varied at all and the values are virtually the same. Second, the intrinsic output capacitance ($C_{OSS}$) is slightly shifted after a test at 25 °C, contrary to 150 °C, where the latter has not practically shifted.

### 4.3 RF measurement

At low input power value (between 0.4 and 0.6 W), the degradation is not important. When the input power increases, the shift becomes more remarkable. Although the characterization is carried at 25 °C, the variation of $P_{OUT}$ (at $P_{IN}$ = 1.1 W, Fig. 7) remains predominant after an RF aging test at 25 °C.

## 5 Results analysis and discussion

After the characterization step, the devices aged under various thermal stresses show a degradation for the electrical behavior performance (DC, dynamic and microwave). When the temperature constraint is low, the parameters undergo a more consequent variation. The degradation mechanism causes adverse effects even in static and

**Table 4** Variations of intrinsic capacitances after aging at 25° C

| Device 1 at 25 °C | $C_{ISS}$ (pF) at 26 V | $C_{OSS}$ (pF) at 26 V | $C_{RSS}$ (pF) at 0 V | $C_{RSS}$ (Ω) at 26 V |
|---|---|---|---|---|
| Before aging | 15.3 | 10.25 | 2.58 | 0.43 |
| After aging | 15.36 | 9.77 | 1.82 | 0.34 |
| Variation in % | +0.4 | −4.6 | −29.5 | −21 |

**Table 5** Variations of intrinsic capacitances after aging at 150° C

| Device 1, 150 °C | $C_{ISS}$ (pF) at 26 V | $C_{OSS}$ (pF) at 26 V | $C_{RSS}$ (pF) at 0 V | $C_{RSS}$ (Ω) at 26 V |
|---|---|---|---|---|
| Before aging | 15.3 | 10.1 | 2.52 | 0.44 |
| After aging | 15.4 | 9.9 | 2.1 | 0.37 |
| Variation in % | +0.65 | −3 | −16.6 | −15.9 |

dynamic mode. Because of some parameters that are highly related to a device structure region [14], the degradation can likely locate. Same results proven by several authors like Maanane et al. [7] and Rahmet et al. [18] that have investigated the accelerated aging test effects for these critical electrical parameters of RF LDMOSFETs, specially the $V_{TH}$, $R_{DSON}$, $C_{RSS}$ and $P_{OUT}$.

The electrical and physical results of the degradation phenomena allows to deduce that the degradation is related to the hot carriers. To ensure these results, a device physical model was implemented with the ATLAS-SILVACO simulator [10].

During all the life tests, threshold voltage $V_{TH}$, drain-source current $I_{DS}$ and on-state resistance $R_{DSON}$ are shifted. We noticed that the DC behavior, specially these parameters, are affected by the RF life aging. Vth is increased and has a good interdependence with the $I_{DS}$ current downturn (the $R_{DSON}$ increases due to lower $I_{DS}$). As a result, numerous electrons are accelerated to high velocities with this peak of higher electric field. They become very energetic and should be accelerated to move away from their ordinary directional flow.

At high voltage $V_{DS}$ bias (44 V) with a 3.8 $V_{GS}$ voltage applied to the device structure. The presence of an intense electric field under gate oxide by a peak in area LDD (Fig. 8) and a high electrons concentration at the $SiO_2$/LDD interface (Fig. 9) contributed to the appearance of hot carriers [5, 19]. The simulation results tend to prove that for these tests conditions (polarization, temperature, etc.) given, all the favors met to a degradation induced by hot carriers. Like the congestion of current lines (Fig. 9) is greater at low temperature at the $SiO_2$/LDD interface, the probability of

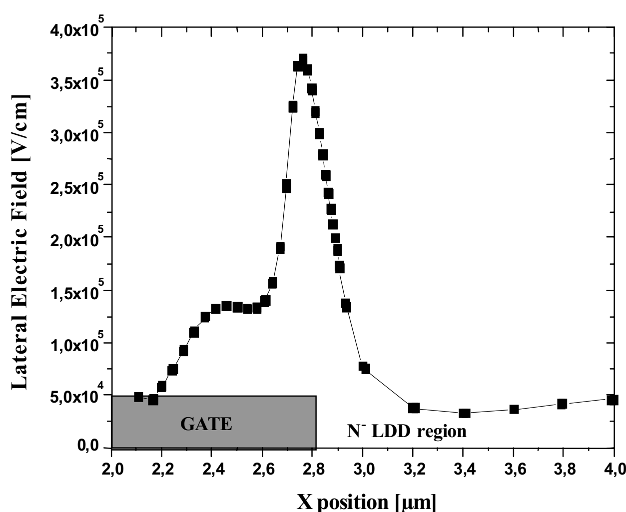



Fig. 8 Simulation of lateral electric field distribution of N-LDMOSFET structure in the gate/N-LDD region, with $V_{ds}$ = 44 V and $V_{gs}$ = 3.8 V bias

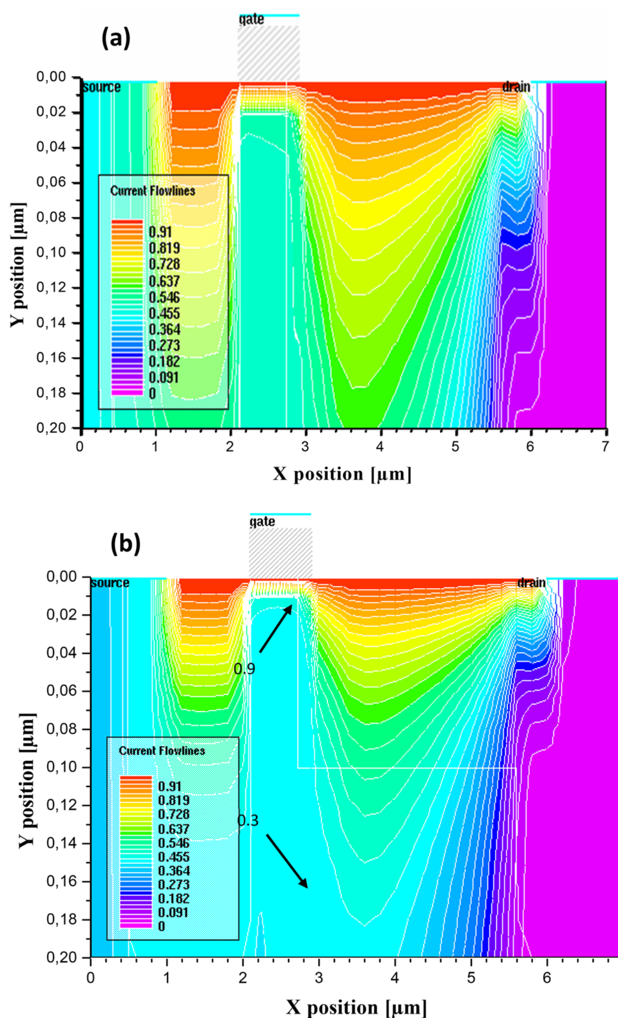



Fig. 9 Simulation of source drain current lines with polarization conditions $V_{DS}$ = 44 V and $V_{GS}$ = 3.8 V: at 25 °C (**a**), at 150 °C (**b**)

hot carrier injection is higher at this point at 25 °C than at 150 °C. Consequently, many electrons becomes accelerated to high velocities through this high electric field peak. They become highly energized and should be accelerated away from their normal directional flow.

The origin of the observed shift related to the presence of very high electric field which increase carrier injection into the grown silicon dioxide layer ($SiO_2$) and also into the interface state Si/$SiO_2$ [8, 20]. The hot carrier degradation effect is closely related with current density and with the most number of free electrons in the silicon oxide region, which majority electrons are concentrated deeply inside the drift region [8, 21].

The proven degradation mechanism for power RF LDMOS is, therefore, the creation of interface states by hot carriers (traps) [4, 8, 22]. The current mechanism of degradation is composed of interface states produced by hot carriers (traps) and a some quantity of the hot electrons

to be trapped in the later, than results in the accumulation of a negative charge at the Si–$SiO_2$ interface [20, 23]. These negative charges attract load-depleting holes in the device drift region [21, 23] and, therefore, increase the $R_{DSON}$ resistance and reduce the ability of Miller $C_{RSS}$. Finally, increasing the $R_{DSON}$ resistor, reduces the peak saturation current ($I_{DSS}$) and related to that, the output power ($P_{SAT}$) also reduces. Therefore, more interface states are generated in low temperature. All these aspects clearly explain why the drifts of $I_{DSS}$, $P_{OUT}$ and for electrical parameters are more significant at 25 °C than at 150 °C.

## 6 Conclusion and prospects

In this study, a comparative result has been done to reliability of power RF LDMOS device by two accelerated aging tests. The temperature variation has a repercussion on the electrical parameters and the device behavior; it can also influence its amplification performance. The robustness variations of critical parameters (DC, AC and RF) show that the devices that have been subjected to an RF aging test at 25 °C experience a greater degradation than at 150 °C.

The reliability is shown by monitoring $I_{DS}$, $V_{TH}$, $R_{DSON}$, $P_{out}$, T°C and $C_{RSS}$ parameters in order to put in evidence the LDMOS performances. This study highlights that the phenomenon of hot carrier injection is the main degradation mechanism in LDMOS on this defined stress conditions, and that these parameters are sensitive to the electrons injected in gate/$SiO_2$ interface traps. To conclude, the variation of the current during the 1500 h could be due to a hot carrier phenomenon with consequences on device performances.

Other type of aging tests at other conditions is in progress and may be with different technologies such as IGBT and VDMOS.

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### Compliance with ethical standards

**Conflict of interest** On behalf of all authors, the corresponding author states that there is no conflict of interest.

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