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Model based current mode control design and experimental validation for a 3ϕ rectifier under unbalanced grid voltage conditions

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Abstract This paper addresses the control design and the experimental validation of a current mode control for a three phase voltage source rectifier. The proposed control law is able to fulfill the voltage regulation and the current tracking control objectives despite of unbalanced and distorted grid voltages. The proposed control law consists of two loops, which are referred as inner tracking loop and the outer voltage regulation loop. The inner loop is designed to provide damping to the system, which also includes and adaptive mechanism. The construction of the current reference is based on the positive component detection of the grid voltage. Therefore, the current produced by the power rectifier is proportional to the fundamental component of the grid voltage, despite of the presence of unbalanced grid voltages. The voltage regulation loop is designed as a proportional-integral controller, which is aimed to regulate the DC output voltage to a desired level. Finally, experimental results are obtained in an experimental prototype of 2 kW to evaluate the performance of the proposed controller.

Keywords PWM rectifier, Power factor correction, Positive-component, Current mode control

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1 Introduction

The increasing use of electronic loads has produced several power quality issues to the utility grid [1]. This kind of loads, also referred as nonlinear loads (NLLs), have negative effects on the power system, for instance, distorted grid currents, low power factor, distorted grid voltage, overheating of electrical machines as well as distribution transformers, among others [2]. Since the power quality is a measure of the efficient use of the electrical energy, this concept has become a critical concern in electrical distribution systems. Thus, several standards like IEC 555-2, IEC 1000-3-2 and IEC 519 [3–5] have been developed to maintain safe limits on the harmonic distortion produced and injected by the NLL to the grid. The power electronics equipment involved in a rectification process is commonly related with current harmonic distortion. Examples of these equipments are uncontrolled rectifiers, phase angle controller rectifiers among others, which produce highly distorted grid currents. As a solution, power converters with capacity of

power factor corrector (PFC) have been developed [6, 7]. This kind of power converters are able to mitigate the harmonic pollution and thus, achieve a power factor close to unity.

The idea behind of the PFC based on pulse-width modulation (PWM) rectifier is to select an adequate power converter and design a proper control law aimed to regulate the DC output towards a desired reference keeping a power factor close to the unity. The later means that the control law is able to track a desired line current reference, which is constructed free of harmonic distortion and in phase with the grid voltage. In this sense, several control approaches have been proposed for voltage source rectifiers to deal with the harmonic pollution problem. For example, in [8–10] direct power control (DPC) approach is applied to reduce the harmonic content by providing a sinusoidal line current. In this technique, the real and reactive powers are used to generate the modulating signals for the power devices. In [11] and [12], model predictive control (MPC) is used to improve the DPC technique. In [13], virtual-flux-based approach is applied to enhance DPC strategy. The current mode control (CMC) approach is focused on solving the current tracking problem, that is, the line current is forced to track a desired current reference. Several strategies have been developed following the CMC. For instance, in [14] a current control strategy to deal with the offset in measurement error and input voltage is proposed. This control strategy is designed in the synchronous reference frame, therefore, the resulting control scheme is designed as two PI vector controllers. In [15], sliding mode control is applied to improve the CMC technique. In recent years AC-DC conversion has been used in smart grid applications due to the need of a power factor close to unity [16–18]. In [19] the smart grid approach is presented as a solution to grid power quality problems by using several power conversion techniques where the DC-DC stage is used to provide power conditioning the DC-DC stage. Another application of voltage source rectifers (VSRs) is in high voltage direct current (HVDC) transmission systems. For instance, in [20] the VSR is used as a stage of a back-to-back converter. In this case, VSR is used to control the DC-link voltage and reactive power, and acts as an interface between the converter and the AC source.

Besides harmonic distortion, the voltage unbalance is one of the most common power quality disturbances in industrial systems. The voltage unbalance frequently occurs due to unsymmetrical impedances of transmission and distribution lines, unequal distribution of single-phase loads, unbalanced three-phase loads, faulty delta transformer connections and single-phase-to-ground faults, among others. Most of the electric equipment have damage susceptibility under unbalance voltage conditions. For instance, operation of induction motors at 5% of voltage unbalance factor (VUF) is not recommended [21, 22]. Additionally, three-phase uncontrolled rectifiers with large output capacitive filters are seriously affected by voltage unbalance. This class of rectifiers produce an unbalance current factor of 100% with only a 0.3% of VUF. It has been also previously reported that 0.3% of VUF in three-phase uncontrolled rectifiers causes non-characteristics harmonics. In this case, third harmonic currents as large as 19.2% of magnitude may appear. As a consequence, several international standards have a restriction on the unbalance factor, such as the IEC 61000-2-2 which limits the VUF to be less than 2% [23]. Important efforts have also been done to propose advanced control strategies for PFCs based on PWM rectifiers which must be able to maintain an adequate system performance despite of input voltage unbalance conditions. In [24], active power oscillation cancelation methods used to enhance the DPC technique, are presented. It was shown that the controller was able to deal with input unbalance voltages. In [25], a new definition of the reactive power is presented for a DPC technique which is aimed to deal with the input voltage unbalance, and does not require the estimation of positive and negative sequences of the grid. In [26], an improved dead-beat based control for a three-phase PWM rectifier under harmonic and unbalance disturbances is presented. In [27], a control scheme for a voltage source converter (VSC) under input voltage disturbances is presented. This scheme is based on a sinusoidal disturbance estimation, and is aimed to model the voltage unbalance as a disturbance, which is estimated and used in a feedback control.

In this paper, the experimental validation and controller design of a three-phase PFC based on a VSR PWM rectifier under unbalance and distorted grid voltages are presented. The proposed control law is designed directly in $\alpha\beta$ coordinates avoiding extra transformation as occurs in DPC techniques. The construction of an adequate current reference is essential in the proposed control design, where the positive component of the grid voltage is used for this purpose. The current reference results in a signal proportional to the positive component of the grid voltage despite of grid voltage unbalance and grid voltage harmonic distortion. To obtain the positive component of the grid the guidelines presented in [8] and [9] have been considered. The proposal of the controller considers the decoupling assumption, which establishes that the faster dynamics can be decoupled from the slower dynamics, that is, the dynamics of the current decoupled from the capacitor voltage dynamics. Therefore the controller can be splitted in two main loops, namely, current tracking loop and voltage regulation loop. The first is formed by a proportional gain plus a couple of adaptive estimators, which are capable to deal with the parameter uncertainties of the input filter. The purpose of the current loop is to track a

desired current reference constructed by using the estimation of the positive component of the grid voltage, this allows to obtain a sinusoidal line current despite the slight amount of harmonic pollution and the unbalanced operation of the grid voltage. Also, the inner loop is designed including a feedforward term since the system model considers the grid impedance. This term is added to deal with the grid impedance effects since it acts as a decoupling term. The voltage regulation loop consists of a proportional-integral (PI) controller which guarantees the regulation of the DC voltage to a constant reference. The output of the voltage loop is used to construct the current reference together with the estimation of the positive component of the grid voltage. The PI controller includes a low pass filter (LPF), that allows restricting the bandwidth and avoids the harmonic pollution in the current reference produced by the rectification process.

The rest of the paper is organized as follows. In Section 2, the model of the VSR is presented. In Section 3, the design of the proposed controller is presented. In Section 4, experimental results, in a 2 kW prototype, are presented including unbalanced and distorted grid voltage conditions. Finally, in Section 5, the conclusions of the paper are presented.

2 System description

In Fig. 1, the representation of a full bridge three-phase VSR topology is shown. As it can be observed, the rectifier is connected at the point of common coupling (PCC) into the grid through an inductive filter. This converter is used as PFC due to its capability to achieve a power factor close to unity. The dynamics of the rectifier as PFC is described by the average model,

$$L_S \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{S,\alpha\beta} = -R_S\boldsymbol{i}_{S,\alpha\beta} - \boldsymbol{e}_{\alpha\beta} + \boldsymbol{v}_{\alpha\beta} \tag{1}$$

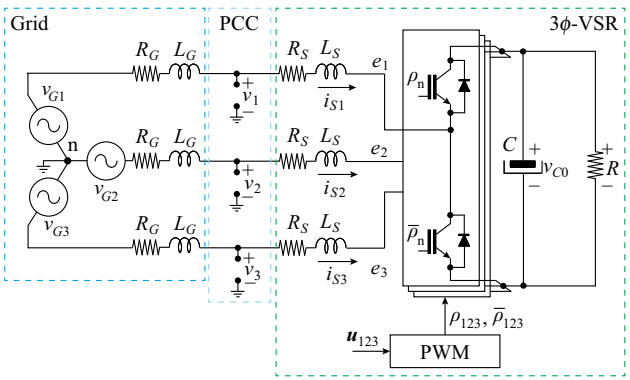


Fig. 1 Three-phase three-wire VSR

$$C\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{v_{C0}^2}{2}\right) = \boldsymbol{e}_{\alpha\beta}^{\top}\boldsymbol{i}_{S,\alpha\beta} - \left(\frac{v_{C0}^2}{R_S}\right) \tag{2}$$

$$\boldsymbol{e}_{\alpha\beta} = \frac{v_{C0}\boldsymbol{u}_{\alpha\beta}}{2} \tag{3}$$

where $\boldsymbol{i}_{S,\alpha\beta} = [i_{S\alpha}, i_{S\beta}]^{\top}$, $\boldsymbol{v}_{\alpha\beta} = [v_\alpha, v_\beta]^{\top}$ and $\boldsymbol{u}_{\alpha\beta} = [u_\alpha, u_\beta]^{\top}$ are the currents flowing through the grid impedance, the voltages at the PCC and the duty cycles, respectively, all in $\alpha\beta$ reference frame. Notice that, $\boldsymbol{v}_{\alpha\beta} = \boldsymbol{v}_{G,\alpha\beta} - L_G\dot{\boldsymbol{i}}_{S,\alpha\beta} - R_G\boldsymbol{i}_{S,\alpha\beta}$ represents the voltage between the PCC and the neutral point, which includes the impedance of the grid. The signal $\boldsymbol{e}_{\alpha\beta} := (v_{C0}\boldsymbol{u}_{\alpha\beta})/2$ is the control input; v_{C0} is the DC voltage in the capactior; L_S, R_S, C and R are the inductance of the input filter, the parasitic resistor of the input filter, the output capacitance and the load resistor, respectively. In order to obtain the average model of the VSR, the switching vector $[\rho_1, \rho_2, \rho_3]^{\top}$ is substituted in the dynamics equations by the respective duty cycles vector $[u_1, u_2, u_3]^{\top}$. Note that, in this paper, bold typeface characters denote either vectors or matrices and normal typeface characters depict scalar quantities. The Clarke's transformation is used to transform $\boldsymbol{v}_{123}$ to $\boldsymbol{v}_{\alpha\beta}$,

$$\boldsymbol{v}_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

2.1 Grid voltage model under unbalanced condition and positive component estimation

In order to simplify presentation, the assumption is made that the grid voltage is considered without any harmonic pollution, then the model under balanced and unbalanced conditions is obtained. The grid voltage can be considered formed by positive- and negative-components, whose fundamental frequency is $f = \omega/2\pi$. A mathematical description of the grid voltage under unbalanced operation in $\alpha\beta$ reference frame is obtained by means of the method presented in [8] as follows.

$$\begin{cases} \boldsymbol{v}_{\alpha\beta} = \boldsymbol{e}^{\boldsymbol{J}\sigma_0}\boldsymbol{V}_{dq}^{+} + \boldsymbol{e}^{-\boldsymbol{J}\sigma_0}\boldsymbol{V}_{dq}^{-} = \boldsymbol{v}_{\alpha\beta,p} + \boldsymbol{v}_{\alpha\beta,n} \\ \boldsymbol{e}^{\boldsymbol{J}\sigma_0} = \begin{bmatrix} \cos(\sigma_0) & \sin(\sigma_0) \\ -\sin(\sigma_0) & \cos(\sigma_0) \end{bmatrix} \\ \boldsymbol{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \end{cases} \tag{4}$$

where $\boldsymbol{v}_{\alpha\beta,p}$ and $\boldsymbol{v}_{\alpha\beta,n}$ represent the positive and negative symmetrical components of the grid voltage $\boldsymbol{v}_{\alpha\beta}$; σ_0 represents the phase angle; $\boldsymbol{V}_{dq}^{+} = \left[V_d^{+}, V_q^{+}\right]^{\top}$ and $\boldsymbol{V}_{dq}^{-} = \left[V_d^{-}, V_q^{-}\right]^{\top}$ are vectors of harmonic coefficients. Next, the guidelines shown in [8] and [28] are applied to obtain the

positive component of the grid voltage. From (4), the model of the grid voltage in unbalanced operation is expressed as:

$$\dot{\boldsymbol{v}}_{\alpha\beta} = \boldsymbol{J}\omega\boldsymbol{\varphi}_{\alpha\beta} \tag{5}$$

$$\dot{\boldsymbol{\varphi}}_{\alpha\beta} = \boldsymbol{J}\omega\boldsymbol{v}_{\alpha\beta} \tag{6}$$

It is important to note that the term $\boldsymbol{\varphi}_{\alpha\beta}$ is defined as $\boldsymbol{\varphi}_{\alpha\beta} := \boldsymbol{v}_{\alpha\beta,p} - \boldsymbol{v}_{\alpha\beta,n}$, which completes the model of the voltage of the grid in unbalanced operation. Observe that, in balanced condition, the model of $\boldsymbol{v}_{\alpha\beta}$ can be simplified to $\dot{\boldsymbol{v}}_{\alpha\beta} = \boldsymbol{J}\omega\boldsymbol{v}_{\alpha\beta}$, and $\boldsymbol{\varphi}_{\alpha\beta} = \boldsymbol{v}_{\alpha\beta}$. Considering (4) and the definition of the complementary term $\boldsymbol{\phi}_{\alpha\beta}$, the following relationship is established,

$$\begin{bmatrix} \boldsymbol{v}_{\alpha\beta} \\ \boldsymbol{\varphi}_{\alpha\beta} \end{bmatrix} = \begin{bmatrix} \boldsymbol{I} & \boldsymbol{I} \\ \boldsymbol{I} & -\boldsymbol{I} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_{\alpha\beta,p} \\ \boldsymbol{v}_{\alpha\beta,n} \end{bmatrix} \tag{7}$$

where $\boldsymbol{I}$ is the 2×2 identity matrix. Next, from (7) $\boldsymbol{v}_{\alpha\beta,p}$ and $\boldsymbol{v}_{\alpha\beta,n}$ are obtained as a linear combination of $\boldsymbol{v}_{\alpha\beta}$ and $\boldsymbol{\varphi}_{\alpha\beta}$, this leads to

$$\begin{bmatrix} \boldsymbol{v}_{\alpha\beta,p} \\ \boldsymbol{v}_{\alpha\beta,n} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \boldsymbol{I} & \boldsymbol{I} \\ \boldsymbol{I} & -\boldsymbol{I} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_{\alpha\beta} \\ \boldsymbol{\varphi}_{\alpha\beta} \end{bmatrix} \tag{8}$$

The term $\boldsymbol{v}_{\alpha\beta,p}$ is the fundamental signal used to generate the current reference for the current tracking loop. As will be observed later, the positive component of $\boldsymbol{v}_{\alpha\beta}$ is obtained from (8). Observe that, $\boldsymbol{v}_{\alpha\beta,p}$ is produced by a linear combination, which is dependent of $\boldsymbol{\varphi}_{\alpha\beta}$ and $\boldsymbol{v}_{\alpha\beta}$. Nonetheless, the term $\boldsymbol{\varphi}_{\alpha\beta}$ is unavailable for measurement. Hence, to deal with this inconvenience, auxiliary estimators of $\boldsymbol{v}_{\alpha\beta,p}$ and $\boldsymbol{\varphi}_{\alpha\beta}$ are proposed. By adding a damping term to the system model (5)–(6), the following structure for the estimators is obtained,

$$\dot{\hat{\boldsymbol{v}}}_{\alpha\beta} = \boldsymbol{J}\omega\hat{\boldsymbol{\varphi}}_{\alpha\beta} + \varsigma\tilde{\boldsymbol{v}}_{\alpha\beta} \tag{9}$$

$$\dot{\hat{\boldsymbol{\varphi}}}_{\alpha\beta} = \boldsymbol{J}\omega\hat{\boldsymbol{v}}_{\alpha\beta} \tag{10}$$

where $\tilde{\boldsymbol{v}}_{\alpha\beta} := \boldsymbol{v}_{\alpha\beta} - \hat{\boldsymbol{v}}_{\alpha\beta}$; ς is a positive design term, which provides damping. Observe that, by estimating the signals $\hat{\boldsymbol{v}}_{\alpha\beta}$ and $\hat{\boldsymbol{\varphi}}_{\alpha\beta}$ through the use of the proposed estimator, (9)–(10), the positive component of the grid voltage is calculated as $\hat{\boldsymbol{v}}_{\alpha\beta,p} = (\hat{\boldsymbol{v}}_{\alpha\beta} + \hat{\boldsymbol{\varphi}}_{\alpha\beta})/2$.

2.2 Control objectives

The main purpose of a three-phase VSR performing as PFC is to achieve a power factor close to unity, that is, to compensate the harmonic distortion and provide a sinusoidal line current in phase with the grid voltage and also supply a regulated DC voltage to the load. To ease the controller design, a time-scale separation is assumed between the faster current, and the slower DC capacitor voltage dynamics, this is also known as decoupling assumption. This provides the possibility to separate the design of the controller in two main loops, namely, current tracking loop and voltage regulation loop [29]. Before starting the design of the controller, these control objectives for the three-phase VSR must be formally expressed as follows:

1) Current tracking control objective

The current of the grid must track a current reference signal $\boldsymbol{i}_{S,\alpha\beta}$ in order to achieve a power factor close to unity, that is,

$$\boldsymbol{i}_{S,\alpha\beta} \to \boldsymbol{i}^*_{S,\alpha\beta} \text{ as } t \to \infty$$

The current reference signal can be calculated as a signal proportional to the positive component of the grid voltage $\boldsymbol{v}_{\alpha\beta,p}$, that is,

$$\boldsymbol{i}^*_{S,\alpha\beta} = \frac{P^*}{\|\boldsymbol{v}_{\alpha\beta,p}\|^2}\boldsymbol{v}_{\alpha\beta,p} \tag{11}$$

where $\boldsymbol{i}^*_{S,\alpha\beta}$ represents the current reference; P^* is a scalar representing the power reference, which is calculated at the voltage regulation loop. Observe that, the term $\|\boldsymbol{v}_{\alpha\beta,p}\|^2$ represents the root-mean-square (RMS) value of $\boldsymbol{v}_{\alpha\beta,p}$.

2) Voltage regulation control objective

The voltage of the capacitor must be regulated towards a desired constant reference V_{ref}, that is,

$$v_{C0} \to \langle V_{ref} \rangle_0 \text{ as } t \to \infty$$

This guarantees that a regulated DC voltage is delivered to the load. Fulfilment of this objective yields an output signal, from the voltage regulation loop, that together with $\hat{\boldsymbol{v}}_{\alpha\beta,p}$ is used to construct the current reference.

3 Controller design

In this section, the controller of the VSR based on positive component estimation is presented. The controller consists in two main loops, namely, current tracking loop to allow a proper tracking of the current reference constructed by using the estimate of the positive component of the grid voltage, and a voltage regulation loop, which achieves the delivery of a properly regulated DC capacitor voltage to the load. The following equations provide a more complete model than system (1)–(3) since it includes the grid impedance modeling.

$$(L_S + L_G)\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{S,\alpha\beta} = -(R_S + R_G)\boldsymbol{i}_{S,\alpha\beta} - \boldsymbol{e}_{\alpha\beta} + \boldsymbol{v}_{G,\alpha\beta} \tag{12}$$

$$C\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{v_{C0}^2}{2}\right) = \boldsymbol{e}_{\alpha\beta}^{\top}\boldsymbol{i}_{S,\alpha\beta} - \left(\frac{v_{C0}^2}{R}\right) \tag{13}$$

$$\boldsymbol{e}_{\alpha\beta} = \frac{v_{C0}\boldsymbol{u}_{\alpha\beta}}{2} \tag{14}$$

3.1 Current tracking loop

To design the current control loop, only the subsystem (12) is considered which represents the dynamics of the grid current. First of all, the current dynamics (12) is expressed in terms of its increments as:

$$\begin{aligned}(L_S + L_G)\dot{\tilde{\boldsymbol{i}}}_{S,\alpha\beta} = &- \boldsymbol{e}_{\alpha\beta} - (R_S + R_G)(\tilde{\boldsymbol{i}}_{S,\alpha\beta} - \boldsymbol{i}^*_{S,\alpha\beta}) \\ &- (L_S + L_G)\dot{\boldsymbol{i}}^*_{S,\alpha\beta} + \boldsymbol{v}_{G,\alpha\beta}\end{aligned} \tag{15}$$

It can be observed that, the current reference derivative $\dot{\boldsymbol{i}}^*_{S,\alpha\beta}$ can be approximated as $\dot{\boldsymbol{i}}^*_{S,\alpha\beta} = P^*\dot{\hat{\boldsymbol{v}}}_{\alpha\beta,p}/\|\boldsymbol{v}_{\alpha\beta,p}\|^2$, where the term $\dot{\hat{\boldsymbol{v}}}_{\alpha\beta,p}$ is obtained as:

$$\dot{\hat{\boldsymbol{v}}}_{\alpha\beta,p} = \frac{1}{2}\left(\dot{\hat{\boldsymbol{v}}}_{\alpha\beta} + \dot{\hat{\boldsymbol{\varphi}}}_{\alpha\beta}\right) = \omega\boldsymbol{J}\hat{\boldsymbol{v}}_{\alpha\beta,p}$$

Therefore, the derivative of the current reference is obtained in terms of the current reference as $\dot{\boldsymbol{i}}^*_{S,\alpha\beta} = \omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta}$ and with this, the error model of the system can be established as:

$$\begin{aligned}(L_S + L_G)\dot{\tilde{\boldsymbol{i}}}_{S,\alpha\beta} = &- \boldsymbol{e}_{\alpha\beta} - (R_S + R_G)(\tilde{\boldsymbol{i}}_{S,\alpha\beta} - \boldsymbol{i}^*_{S,\alpha\beta}) \\ &- (L_S + L_G)\omega_0\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta} + \boldsymbol{v}_{G,\alpha\beta}\end{aligned} \tag{16}$$

In order to provide a stable current tracking and taking into account the structure of the system (16) a controller can be proposed as,

$$\boldsymbol{e}_{\alpha\beta} = \boldsymbol{v}_{\alpha\beta} + \boldsymbol{K}_i\tilde{\boldsymbol{i}}_{S,\alpha\beta} - R_S\boldsymbol{i}^*_{S,\alpha\beta} - L_S\omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta}$$

where $\tilde{\boldsymbol{i}}_{S,\alpha\beta} := \boldsymbol{i}_{S,\alpha\beta} - \boldsymbol{i}^*_{S,\alpha\beta}$ and $\boldsymbol{K}_i = \mathrm{diag}\{k_{i\alpha}, k_{i\beta}\}$ is a design positive definite matrix. Due to the impossibility of taking measurements of the terms $R_S\boldsymbol{i}^*_{S,\alpha\beta}$ and $L_S\omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta}$, a couple of estimators of the parameters $\hat{R}_S$ and $\hat{L}_S$ are proposed. Observe that, the current reference is computed by making use of the output of the voltage regulation loop and $\boldsymbol{v}_{\alpha\beta,p}$. Hence, it is possible to express without loss of generality the controller as follows

$$\boldsymbol{e}_{\alpha\beta} = \boldsymbol{v}_{\alpha\beta} + \boldsymbol{K}_i\tilde{\boldsymbol{i}}_{S,\alpha\beta} - \hat{R}_S\boldsymbol{i}^*_{S,\alpha\beta} - \hat{L}_S\omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta} \tag{17}$$

The design of the estimations $\hat{R}_S$ and $\hat{L}_S$ is performed following the adaptive scheme described next. The closed loop subsystem (16) and controller (17) yields the following perturbed LTI system,

$$L_S\dot{\tilde{\boldsymbol{i}}}_{S,\alpha\beta} = -\boldsymbol{K}\tilde{\boldsymbol{i}}_{S,\alpha\beta} + \tilde{R}_S\boldsymbol{i}^*_{S,\alpha\beta} + \tilde{L}_S\omega_0\boldsymbol{J}\boldsymbol{i}^*_{S\alpha\beta} \tag{18}$$

which is known as the error dynamics. Where the terms $\tilde{L}_S := \hat{L}_S - L_S$, $\tilde{R}_S := \hat{R}_S - R_S$ and the term $\boldsymbol{K} := \boldsymbol{K}_i + R_S\boldsymbol{I}$, thus, the term K is of the form $\boldsymbol{K} = \mathrm{diag}\{k_\alpha, k_\beta\}$. It can be observed that the terms R_S and $\boldsymbol{K}_i$, which are present on the current error signal $\boldsymbol{i}_{S,\alpha\beta}$, are damping terms, where R_S is an unknown positive constant and $\boldsymbol{K}_i$ is a diagonal matrix that has positive control design parameters at its diagonal.

The design of the adaptive law follows the Lyapunov guidelines, where the following energy storage function is proposed:

$$W = \frac{L_S}{2}i_{S,\alpha}^2 + \frac{L_S}{2}i_{S,\beta}^2 + \frac{1}{2\eta_{Ls}}\tilde{L}_S^2 + \frac{1}{2\eta_{Rs}}\tilde{R}_S^2$$

The time derivative of the Lyapunov function $\dot{W}$ along the trajectories of (18) is given by

$$\begin{aligned}\dot{W} = &- k_\alpha\tilde{i}_{S,\alpha}^2 - k_\beta\tilde{i}_{S,\beta}^2 + \tilde{R}_S\tilde{\boldsymbol{i}}_{S,\alpha\beta}^{\top}\boldsymbol{i}^*_{S,\alpha\beta} + \frac{1}{\eta_{Rs}}\dot{\tilde{R}}_S\tilde{R}_S \\ &+ \tilde{L}_S\tilde{\boldsymbol{i}}_{S,\alpha\beta}^{\top}\omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta} + \frac{1}{\eta_{Ls}}\dot{\tilde{L}}_S\tilde{L}_S\end{aligned} \tag{19}$$

which is forced to be negative semidefinite by compelling the estimates $\hat{R}_S$ and $\hat{L}_S$ satisfy the following dynamics,

$$\dot{\tilde{R}}_S = \dot{\hat{R}}_S = -\eta_{Rs}\tilde{\boldsymbol{i}}_{S,\alpha\beta}^{\top}\boldsymbol{i}^*_{S,\alpha\beta} \tag{20}$$

$$\dot{\tilde{L}}_S = \dot{\hat{L}}_S = -\eta_{Ls}\tilde{\boldsymbol{i}}_{S,\alpha\beta}^{\top}\omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta} \tag{21}$$

where $\eta_{Rs} > 0$ and $\eta_{Ls} > 0$, are design parameters representing the adaptive gains. Therefore

$$\dot{W} = -k_\alpha\tilde{p}^2 - k_\beta\tilde{q}^2 \tag{22}$$

As W is radially unbounded and $\dot{W}$ is negative semi-definite then $\tilde{i}_{S,\alpha} \in \mathcal{L}_2 \bigcap \mathcal{L}_\infty$, $\tilde{i}_{S,\beta} \in \mathcal{L}_2 \bigcap \mathcal{L}_\infty$, $\tilde{R}_S \in \mathcal{L}_\infty$ and $\tilde{L}_S \in \mathcal{L}_\infty$. Assuming that $i^*_{S,\alpha}$ and $i^*_{S,\beta}$ are bounded, then $\dot{\tilde{i}}_{S,\alpha} \in \mathcal{L}_\infty$ and $\dot{\tilde{i}}_{S,\beta} \in \mathcal{L}_\infty$, and thus, $\tilde{i}_{S,\alpha} \to 0$ and $\tilde{i}_{S,\beta} \to 0$, asymptotically. Moreover, $\dot{W} \equiv 0$ implies $\tilde{i}_{S,\alpha} \equiv 0$, $\tilde{i}_{S,\beta} \equiv 0$, $\dot{\tilde{i}}_{S,\alpha} \equiv 0$, $\dot{\tilde{i}}_{S,\beta} \equiv 0$, $i_{S,\alpha} = i^*_{S,\alpha}$ and $i_{S,\beta} = i^*_{S,\beta}$, then from (18) the only solution for the estimation errors is $\tilde{R}_S = 0$ and $\tilde{L}_S = 0$, and thus, the estimates converge towards the right values asymptotically, i.e., $\hat{R}_S \to R_S$, $\hat{L}_S \to L_S$ as $t \to \infty$.

Remark 1: Notice that the introduction of the feedforward term $\boldsymbol{v}_{\alpha\beta}$ in controller (17) causes the decoupling of the line impedance dynamics. That is, the terms associated with this impedance are eliminated from the error dynamics (18).

3.2 Voltage regulation loop

The design of the voltage regulation loop involves subsystem (13). Moreover, based on the decoupling assumption, it is considered that the current tracking objective has been fulfilled after a relative short time, that is, $\tilde{\boldsymbol{i}}_{S,\alpha\beta} \to 0$. Otherwise, it is assumed that $\boldsymbol{e}_{\alpha\beta}$ is bounded. The latter turns out to be true if the terms at $\boldsymbol{e}_{\alpha\beta}$ as well as the adaptive estimations $\hat{L}_S$ and $\hat{R}_S$ are bounded too. Therefore, subsystem (2) can be rewritten in terms of the increments of a new state $z_2 := v_{C0}^2/2$ as follows,

$$C\dot{\tilde{z}}_2 = \boldsymbol{v}_{\alpha\beta}^{\top}\boldsymbol{i}_{S,\alpha\beta} - \frac{2\tilde{z}_2}{R_S} = P^* - \frac{2x_2}{R_S} \tag{23}$$

where $\tilde{z}_2 := (z_2 - V_{ref}^2/2)$ and P^* is the control input. On the other hand, the voltage regulation control loop objective is established in terms of the average of the DC voltage, thus, it is equivalent to $\langle z_2 \rangle_0 \to V_{ref}^2/2$. Therefore, the DC component of z_2 is extracted of (23) which yields

$$C\dot{\tilde{z}}_{20} = P^* - \frac{2\tilde{z}_{20}}{R_S} \tag{24}$$

where $\tilde{z}_{20}$ represents the DC component of the state z_2 and this can be obtained by the average of the state z_2 in a definite time t by the following averaging operation

$$\langle x \rangle_0(t) = \frac{1}{T}\int_{t-T}^{t} x(\tau)\mathrm{d}\tau$$

Hence, to assure $\tilde{z}_{20} \to 0$ a controller is proposed as follows,

$$P^* = -k_{iv}\varepsilon - k_{pv}\chi \tag{25}$$

$$\dot{\varepsilon} = \tilde{z}_{20} \tag{26}$$

$$\tau\dot{\chi} = \tilde{z}_{20} - \chi \tag{27}$$

where the terms k_{pv}, k_{iv} are positive gains that represent the proportional and integral gains of a PI controller; τ is the time constant of a LPF. System (25)–(27) can be restructured in form of transfer function, that is,

$$P^* = \left[-\frac{k_{iv}}{s} - \frac{k_{pv}}{\tau s + 1}\right]\tilde{z}_{20} \tag{28}$$

where s represents the complex Laplace variable. It is important to note that, due to the rectification process an unavoidable second harmonic fluctuation appears in the current tracking loop. Hence, in the proposed control law, to guarantee the regulation of the DC component of z_2 into its reference, a suitable filtering must be included to decrease the impact of such fluctuation. In order to establish a straightforward solution to solve these issues, a PI controller with a relatively low bandwidth is proposed (28). This controller ensures the DC voltage regulation of z_2 unto its reference $V_{ref}^2/2$, and reduces the impact of the harmonic fluctuation on the DC-link.

3.3 Overall proposed controller

By summarizing, the complete controller for the three-phase VSR consists of a current tracking loop formed by (29)–(31) and a voltage regulation loop shown in (32),

$$\boldsymbol{e}_{\alpha\beta} = \boldsymbol{v}_{\alpha\beta} + \boldsymbol{K}_i\tilde{\boldsymbol{i}}_{S,\alpha\beta} - \hat{R}_S\boldsymbol{i}^*_{S,\alpha\beta} - \hat{L}_S\omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta} \tag{29}$$

$$\hat{R}_S = -\frac{\eta_{Rs}}{s}\tilde{\boldsymbol{i}}_{S,\alpha\beta}^{\top}\boldsymbol{i}^*_{S,\alpha\beta} \tag{30}$$

$$\hat{L}_S = -\frac{\eta_{Ls}}{s}\tilde{\boldsymbol{i}}_{S,\alpha\beta}^{\top}\omega\boldsymbol{J}\boldsymbol{i}^*_{S,\alpha\beta} \tag{31}$$

$$P^* = \left[-\frac{k_{iv}}{s} - \frac{k_{pv}}{\tau s + 1}\right]\tilde{z}_{20} \tag{32}$$

Observe that, the gain matrix $\boldsymbol{K}_i$ provides damping to the current tracking loop and the proportional terms associated with $\hat{R}_S$ and $\hat{L}_S$ compensate the parameter uncertainties of the input filter. Note that, the current reference $\boldsymbol{i}^*_{S,\alpha\beta}$ is constructed as follows,

$$\boldsymbol{i}^*_{S,\alpha\beta} = \frac{P^*}{\|\boldsymbol{v}_{\alpha\beta,p}\|^2}\boldsymbol{v}_{\alpha\beta,p}$$

where $\|\boldsymbol{v}_{\alpha\beta,p}\|^2$ is the square of the RMS value of $\boldsymbol{v}_{\alpha\beta,p}$. In order to recuperate the control signal $\boldsymbol{u}_{\alpha\beta}$ from the control signal $\boldsymbol{e}_{\alpha\beta}$ the following expression is considered.

$$\boldsymbol{u}_{\alpha\beta} = \frac{2\boldsymbol{e}_{\alpha\beta}}{v_{C0}} \tag{33}$$

Remark 2: The positive component estimation is obtained from (8), and it can be expressed in transfer function form as

$$\hat{\boldsymbol{v}}_{\alpha\beta,p} = \frac{1}{2}\left(\frac{\varsigma s\boldsymbol{I}}{s^2 + \varsigma s + \omega^2} + \frac{\varsigma\omega\boldsymbol{J}}{s^2 + \varsigma s + \omega^2}\right)\boldsymbol{v}_{\alpha\beta}$$

where ς represents a positive design gain that fixes the speed of response. The block diagram of the complete controller is shown in Fig. 2, which depicts the current tracking loop and the voltage regulation loop as described in the previous subsections.

3.4 Tuning guidelines

In this subsection the guidelines for tuning of the controller are presented in order to obtain a desired closed-loop performance. The development of these guidelines are based on the model of the system and the design of the controller.

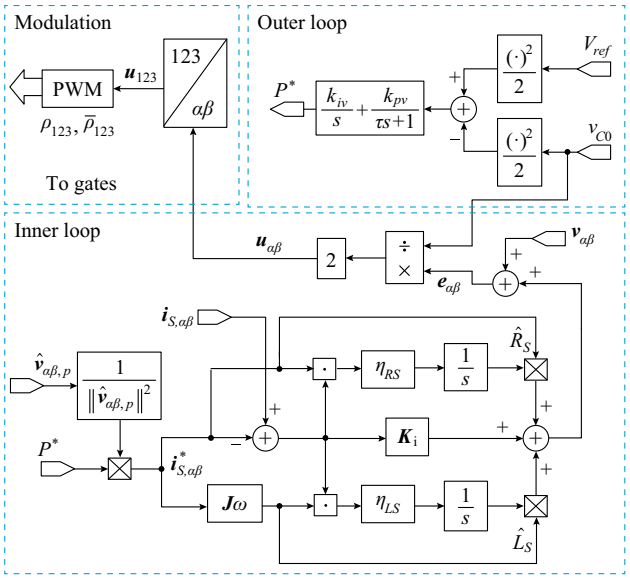


Fig. 2 Block diagram of the overall proposed controller

3.4.1 Tuning guidelines: current tracking loop

As it has been established before, the tracking error $\tilde{\boldsymbol{i}}_{S,\alpha\beta}$ converges to zero as the control parameter $\boldsymbol{K_i}$ is positive definite. Nevertheless, more specific design rules for $\boldsymbol{K_i}$ are still necessary to achieve a desired dynamic performance. For this, recall that the current loop dynamics (18) is considered as the fastest dynamics for the overall system. This dynamics can be expressed as,

$$L_S\dot{\tilde{\boldsymbol{i}}}_{S,\alpha\beta} + \boldsymbol{K_i}\tilde{\boldsymbol{i}}_{S,\alpha\beta} = \tilde{\boldsymbol{\psi}}_{\alpha\beta} \tag{34}$$

where $\tilde{\boldsymbol{\psi}}_{\alpha\beta} := \hat{\boldsymbol{\psi}}_{\alpha\beta} - \boldsymbol{\psi}_{\alpha\beta}$, represents the disturbance rejection error. Notice that, the bandwidth of (34) is given by $\omega_{BWi_{S,\alpha\beta}} = \boldsymbol{K_i}/L_S$. Thus, it is proposed to tune $\boldsymbol{K_i}/L_S$ by fixing that each entry of $\omega_{BWi_{S,\alpha\beta}}$ to be at most, 1/10 of the sampling frequency given by $2\pi f_s$, that is, each entry of $\omega_{BWi_{S,\alpha\beta}} \leq \pi f_s/5$. Therefore, each entry of $\boldsymbol{K_i}$ must be less or equal than $\pi f_s L_S/5$.

3.4.2 Tuning guidelines: voltage regulation loop

Guidelines for tuning controller parameters k_{iv} and k_{pv} in the voltage regulation loop can be obtained from the closed-loop subsystem (24)–(27), which can be rewritten as,

$$C\dot{\tilde{z}}_{20} = -k_i\varepsilon - k_p\chi - \frac{2\tilde{z}_{20}}{R_S} \tag{35}$$

$$\dot{\varepsilon} = \tilde{z}_{20} \tag{36}$$

$$\tau\dot{\chi} = \tilde{z}_{20} - \chi \tag{37}$$

It is common in practice to select $\tau \ll 1/(2\omega)$, where ω is the fundamental frequency. Thus, the effect of the pole located at $-1/\tau$ can be neglected as it is far enough with respect to the remaining dominant poles of the system (35)–(37). Therefore, the characteristic polynomial of the system can be reduced to,

$$s^2 + \frac{k_{pv}R_S + 2}{R_S C}s + \frac{k_{iv}}{C} \tag{38}$$

and therefore, the natural oscillation frequency and the damping factor are shown next,

$$\omega_{nv_{C0}} = \sqrt{\frac{k_{iv}}{C}} \tag{39}$$

$$\chi = \frac{k_{pv}R + 2}{2R\sqrt{k_{iv}C}} \tag{40}$$

Now, if the damping factor is restricted to $\chi \geq 1/\sqrt{2}$, the voltage dynamic must fulfill $\omega_{BWV_C} \leq \omega_{nv_{C0}}$. Moreover, to be consistent with the appealed time-scale separation, the bandwidth of $\omega_{nv_{C0}}$ must be at most 1/10 the bandwidth of the current dynamics $\omega_{BWi_{S,\alpha\beta}}$, i.e., $\omega_{nv_{C0}} \leq \omega_{BWi_{S,\alpha\beta}}$, which holds for $\omega_{nv_{C0}} \leq \omega_{BWi_{S,\alpha\beta}}/10$. Therefore, the parameters can be initially tuned as,

$$\begin{cases} k_{iv} \leq \dfrac{\pi^2 f_s^2 C}{2500} \\ k_{pv} \geq \dfrac{\sqrt{2}\pi f_s C}{50} \end{cases} \tag{41}$$

4 Experimental validation

The proposed controller in the last section has been experimentally validated in a 2 kW three-phase VSR PWM rectifier. The source voltage has been obtained from a Chroma 61705 programmable AC power supply that simulates a phase-to-ground fault to emulate an unbalanced

Table 1 Grid voltage vectors for balanced and unbalanced conditions

Voltage condition	Voltage vectors (V)	VUF (%)
Balanced	$v_1 = 170.0\angle 0$	0
	$v_2 = 170\angle 240$	
	$v_3 = 170.0\angle 120$	
Unbalanced	$v_1 = 170.0\angle 0$	18.5
	$v_2 = 132\angle 230$	
	$v_3 = 132.0\angle 130$	
Unbalanced	$v_1 = 170\angle 0$	25
	$v_2 = 109.7\angle 235$	
	$v_3 = 140.0\angle 140$	

operation in the grid voltage. Table 1 shows the vectors of the three-phase grid voltage in both balanced and unbalanced conditions. The experimental setup VSR rectifier is formed by three inductors $L_S = 3$ mH, three IGBT modules SKM100-GB124D, each module has a complete branch composed by two IGBTs in series connection, a capacitor $C = 1100$ μF, and a DC-load which may change between R and RL. The resistance R has step changes from 250 Ω to 125 Ω and the inductor is fixed to $L = 3$mH to RL DC-load. The DC-link voltage is fixed at $V_{ref} = 350$ V. The parameters of the overall system are shown in Table 2. The controller has been implemented in a dSPACE 1103 board with a sinusoidal modulation based on SPWM scheme has been used to generate the switching signal at a frequency of $f_{sw} = 12250$ Hz. The parameters used for the controller are shown in Table 3, which has been established following the guidelines presented in the previous section. In Fig. 3 the experimental setup of the VSR PWM rectifier is presented.

Table 2 System parameters

System parameter	Value/part number
Power converter	IGBTs, SKM100-GB124D
Input filter	$L_S = 3$ mH
Output filter and load	DC output filter capacitor $C = 1100\,\mu$F
	Resistive load 250 Ω (490 W) to 125 Ω (980 W)
	DC inductive load $L = 3$ mH

Table 3 Controller parameters

Parameter	Value
Current tracking loop	$\boldsymbol{K}_i = 29$
	$\eta_{Rs} = 255$
	$\eta_{Ls} = 0.02$
Voltage regulation loop	$k_{pv} = 0.02$
	$k_{iv} = 0.355$
	$\tau = 1/200$
Positive sequence estimation	$\varsigma = 20$

In this section experimental results are presented in order to validate the performance of the system under the proposed controller. The grid voltage is considered unbalanced with a voltage unbalance factor VUF between 18.5% and 25%. A comparison of the proposed controller and a CMC controller that consists of a proportional term plus a bank of resonant filters as in [30], and that follows the ideas in [31], is also included in this section. The set of experimental results comprises the steady-state responses of the system and transient responses due to load step changes considering R and RL DC-loads after the bulky capacitor. A power quality analyzer was also used in order to present steady-state plots for voltage and current phasor representations, and THD and FFT experimental plots and values in order to show system response to poor power quality conditions at the grid voltage. Experimental results are performed under unbalanced and distorted grid voltages, unless otherwise specified.

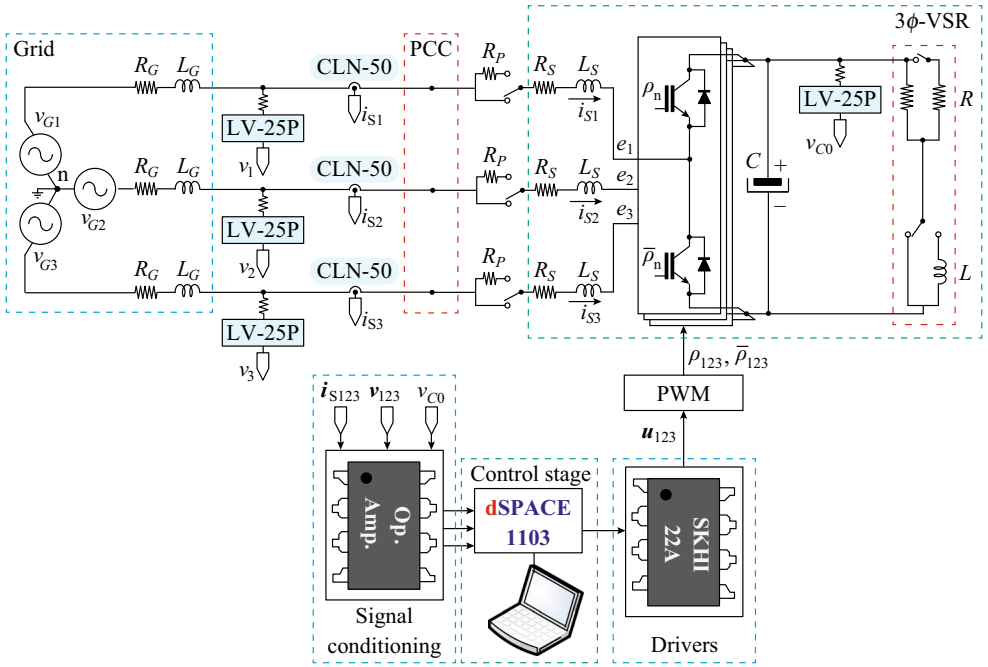


Fig. 3 Experimental setup of VSR PWM rectifier

Figure 4 shows the steady-state responses of $[v_1, v_2, v_3]$ and the compensated lines currents $[i_{S1}, i_{S2}, i_{S3}]$ under three different grid voltage conditions and with a resistive DC-load $R = 125\,\Omega$ from top to bottom. In Fig. 4b and c, a slight amount of grid voltage harmonic distortion can be noted which account for a $\text{THD}_V \leq 5\%$. As it can be observed in Fig. 4a, the grid voltage is balanced and free of harmonic distortion and the compensated line currents have sinusoidal waveforms and are in phase with the grid voltage. Therefore, the proposed control law is able to compensate the input currents under this grid voltage condition. Figure 4b and c show the steady-state responses under unbalanced and distorted grid voltage. It can be noted that the current mode controller also guarantees almost sinusoidal line currents and in phase with the positive sequence of the grid voltage despite of a VUF between 18.5% and 25% respectively. Notice that, in Fig. 4b and c, currents are in phase with v_{S1} which correspond to the positive sequence of the grid voltage. Figure 5a and b show (from top to bottom) the steady-state responses of $[v_1, v_2, v_3]$ and the compensated lines currents $[i_{S1}, i_{S2}, i_{S3}]$ under the same unbalanced grid voltage conditions however, the three-phase rectifier has an *RL* DC-load with $R = 125\,\Omega$ and $L = 3$ mH. It can be noted that, at both cases of grid voltage $\text{VUF} = 18.5\%$ and $\text{VUF} = 25\%$, the current mode controller is also able to assure sinusoidal currents and in phase with the positive sequence of grid voltages under this *RL* DC-load.

Figure 5c shows the performance of the grid currents of the PWM rectifier under the control law presented in [30] which consists of proportional term plus a bank of resonant filters. As it can be observed, if the grid voltage is unbalanced and distorted then the grid current is also unbalanced and distorted given that the control scheme does not consider a mechanism to deal with the grid voltage unbalanced. Notice also that, the proposed control law in this paper could be enhanced by using a similar strategy as in [30]. However, a bank of resonant filters in $\alpha\beta$ coordinates must be added and tuned at odd harmonics of the fundamental frequency. Therefore, the control scheme would become highly bulky. Figure 6 shows, from top to bottom, the time responses in steady-state of grid voltage $[v_1, v_2, v_3]$ and the estimation of the positive-component of the grid voltages $[\hat{v}_{1,p}, \hat{v}_{2,p}, \hat{v}_{3,p}]$ for the following conditions: ① balanced grid voltage and *R* DC-load; ② unbalanced grid voltage with a $\text{VUF} = 18.5\%$ and *R* DC-load; ③ unbalanced grid voltage with a $\text{VUF} = 25\%$ and *RL* DC-load. The positive component of the grid voltage is used to construct the current reference for the inner control loop. Notice that the estimations of the positive component $[\hat{v}_{1,p}, \hat{v}_{2,p}, \hat{v}_{3,p}]$ are balanced sinusoidal signals under the three different conditions described above, however the amplitude changes when an unbalance condition appears in the grid voltage. As it was expected if the VUF increases then the amplitude of the positive components decreases.

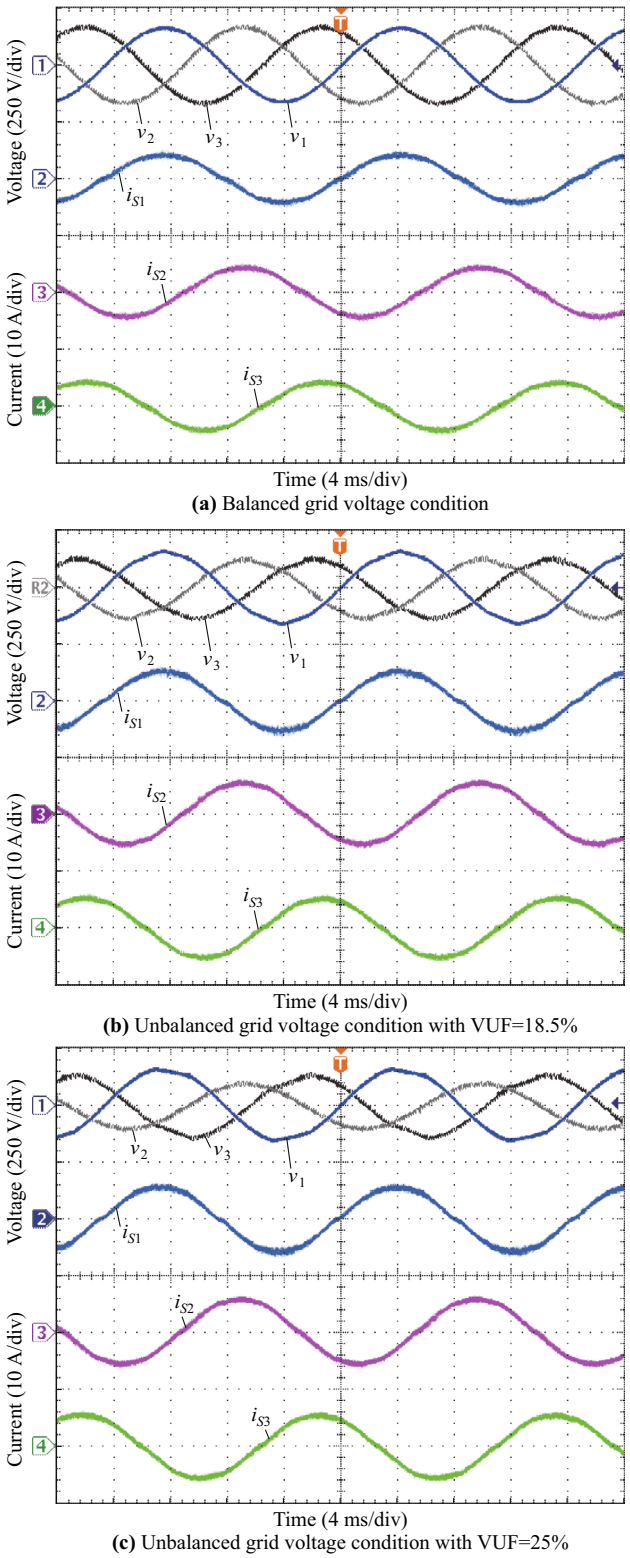
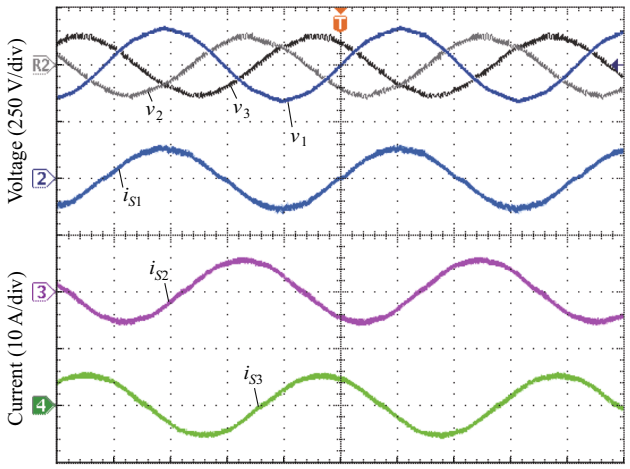
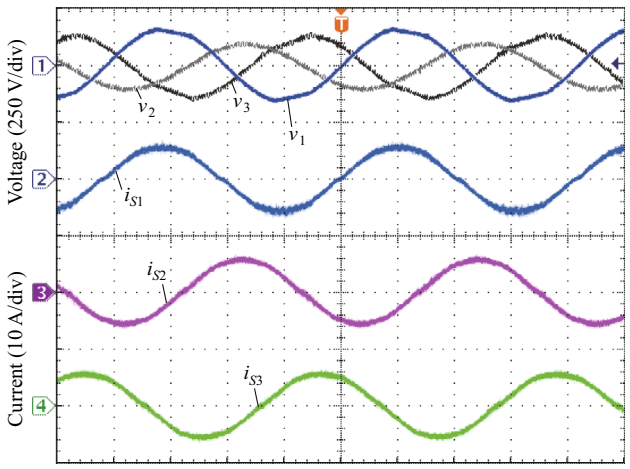


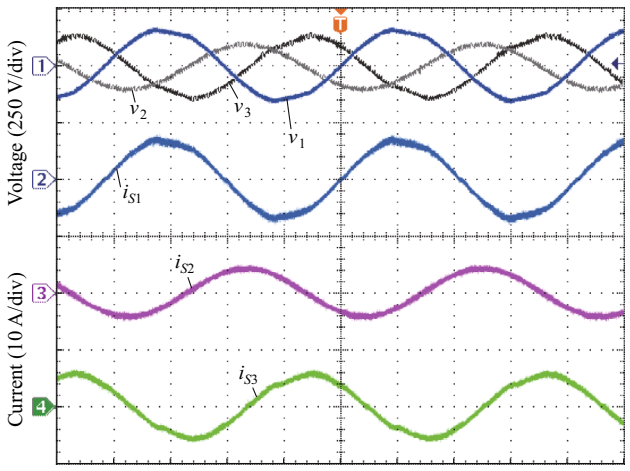
Fig. 4 Time responses



(a) VUF=18.5%

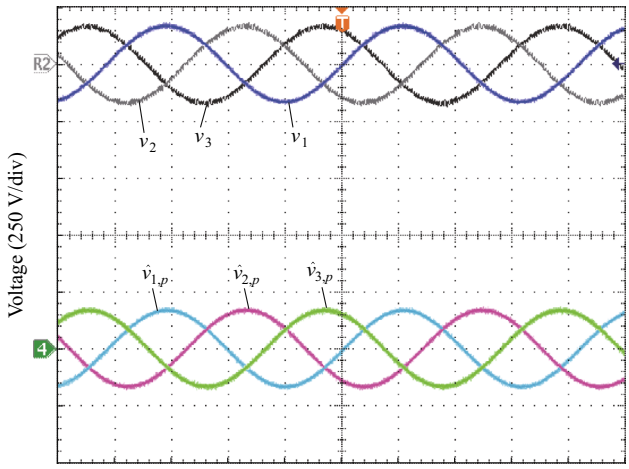


(b) VUF=25%

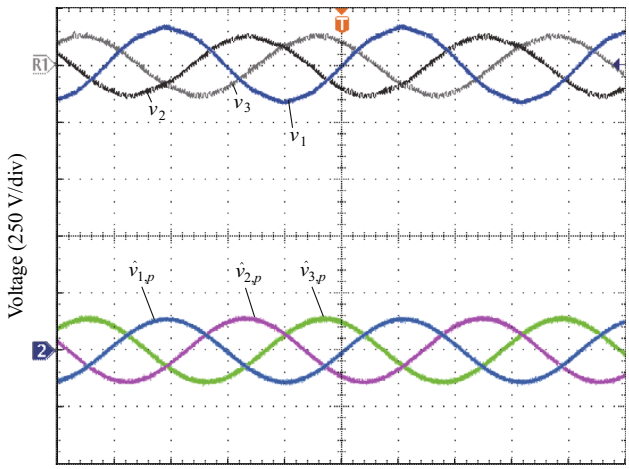


(c) VUF=25%, under control law presented in [30]

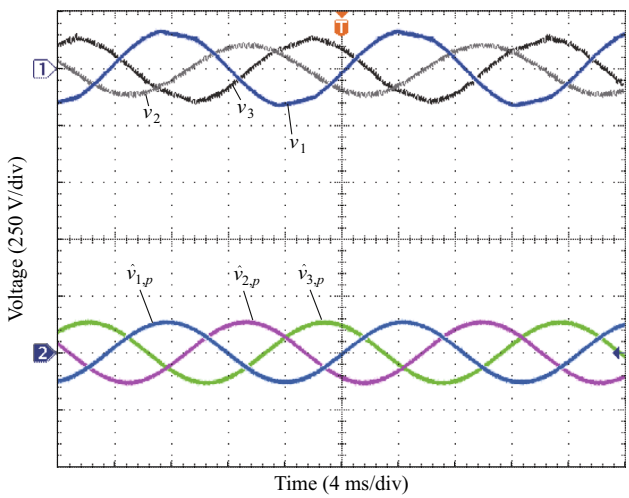
Fig. 5 Time responses for *RL* DC-load under unbalanced grid voltage conditions



(a) Balanced and *R* DC-load

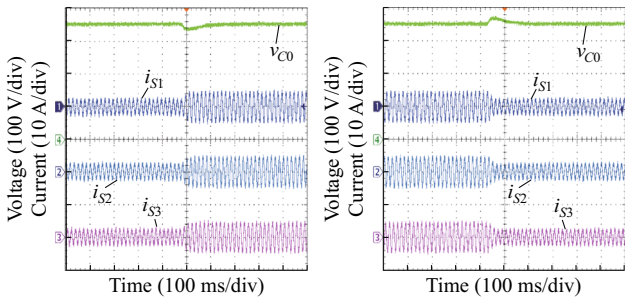


(b) Unbalanced, VUF=18.5% and *R* DC-load

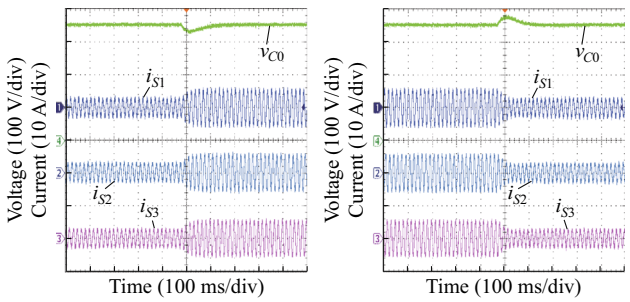


(c) Unbalanced, VUF=25% and *RL* DC-load

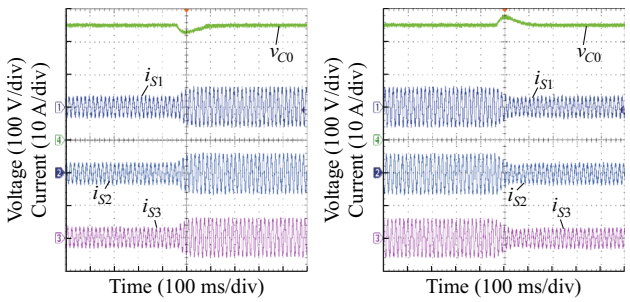
Fig. 6 Time responses of positive component estimator under different conditions



(a) Balanced and R DC load

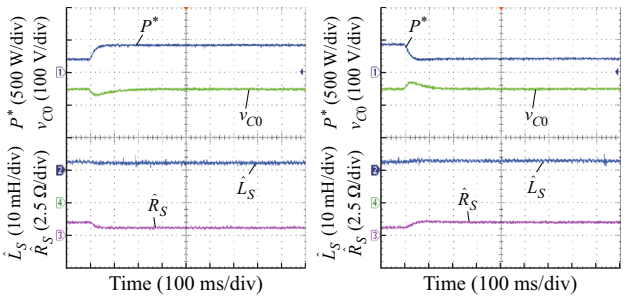


(b) Unbalanced with VUF=18.5% and R DC-load

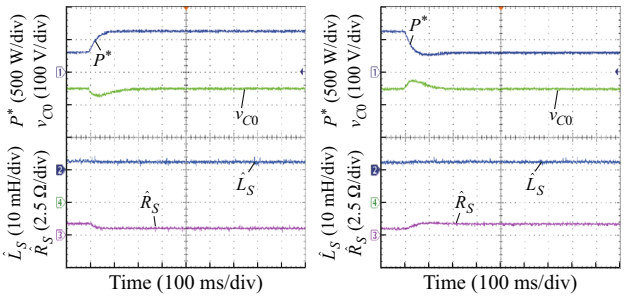


(c) Unbalanced with VUF=25% and RL DC load

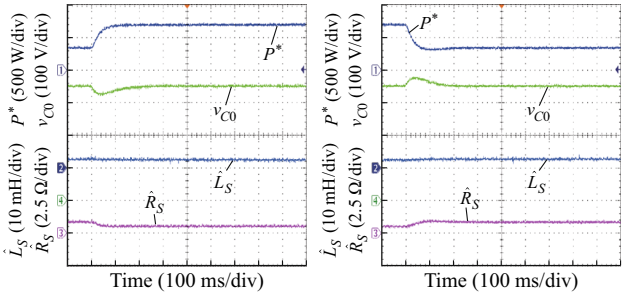
Fig. 7 Transient responses of proposed controller under different grid voltage conditions and loads



(a) Balanced and R DC-load



(b) Unbalanced with VUF=18.5% and R DC-load



(c) Unbalanced with VUF=25% and RL DC-load

Fig. 8 Transient responses of proposed controller under balanced and unbalanced operation during resistance load step changes from $R = 250\,\Omega$ to $R = 125\,\Omega$

Figure 7 shows, from top to bottom, the transient responses, during load step changes, of the capacitor voltage v_{C0} and the line currents $[i_{S1}, i_{S2}, i_{S3}]$ when the resistance R is changed from $R = 250\,\Omega$ to $R = 125\,\Omega$ and back under different grid voltage conditions in the RL DC-load case. In Fig. 7a, the grid voltage is balanced and an R DC-load is considered. In Fig. 7b, the grid voltage is unbalanced with a VUF $= 18.5\%$ and DC-load is of R type. In Fig. 7c, the grid voltage is also unbalanced with a VUF $= 25\%$ and the DC-load consists of a resistance R in series with a fixed inductor $L = 3$ mH. As it can be observed, the proposed controller is capable of providing smooth transient responses, both in line currents and capacitor voltage and, reach the steady state in a relative short time. The controller is also able to regulate the capacitor voltage to a reference fixed at $v_{C0} = 350$ V maintaining a small DC voltage ripple Δv_{C0}.

Figure 8 shows, from top to bottom, the transient responses of the power reference P^*, the DC capacitor voltage v_{C0}, the estimate of the filter inductance $\hat{L}_S$ and the estimate of the series resistance $\hat{R}_S$ under three different grid voltage conditions and DC-loads. In Fig. 8a, the input grid voltage is balanced and with R DC-load type. Figure 8b shows the transient responses under unbalanced grid voltage conditions with a VUF $= 18.5\%$ and a resistive DC-load R. Figure 8c shows performance for unbalance conditions with a VUF $= 25\%$ and an RL DC-load. Notice that, the estimation of the parameter $\hat{L}_S$ and the parasitics resistance $\hat{R}_S$ present small step changes during load changes, due to the increase of the rectifier power demand to the grid. Notice also that the output signal of the voltage control loop, P^*, acts as a modulating signal which is used to calculate the current reference $\boldsymbol{i}^*_{S,\alpha\beta}$. Figure 9 shows the

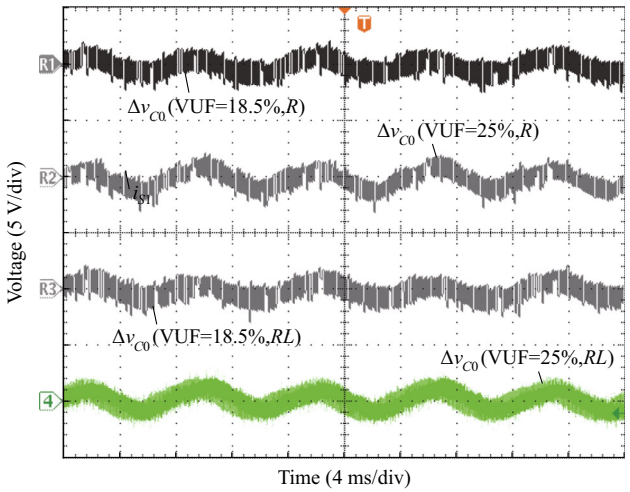
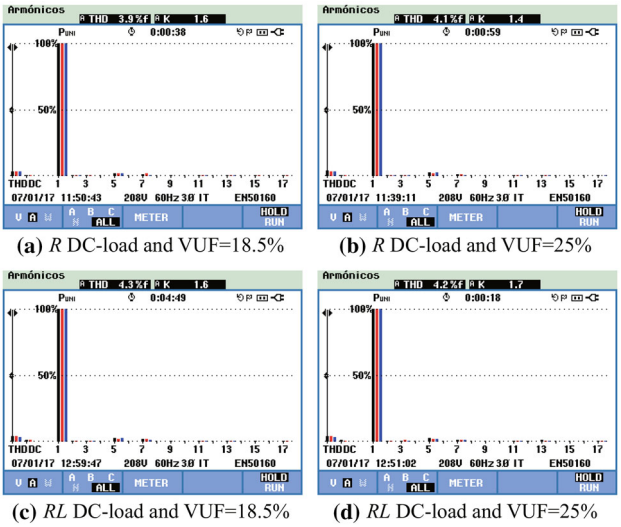


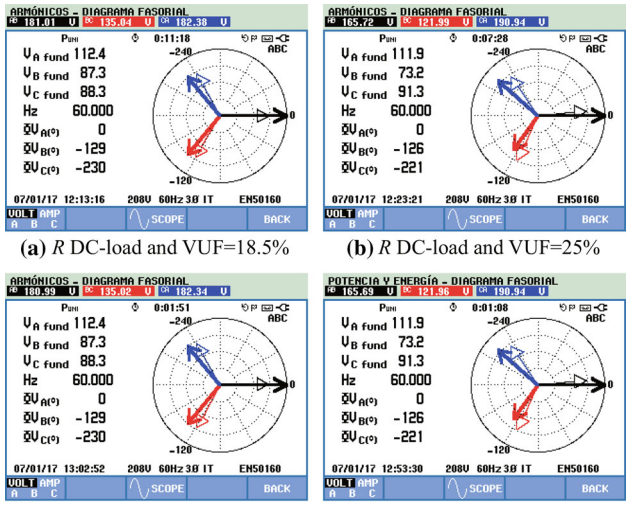
Fig. 9 Capacitor voltage ripple Δv_{C0} under unbalanced grid voltage with *R* and *RL* DC-loads



(a) *R* DC-load and VUF=18.5% **(b)** *R* DC-load and VUF=25%

(c) *RL* DC-load and VUF=18.5% **(d)** *RL* DC-load and VUF=25%

Fig. 10 FFT and THD of line currents



(a) *R* DC-load and VUF=18.5% **(b)** *R* DC-load and VUF=25%

(c) *RL* DC-load and VUF=18.5% **(d)** *RL* DC-load and VUF=25%

Fig. 11 Phasor representation of three phase voltages and currents

Table 4 PF and DPF under different VUFs and loads

Condition	$PF_{3\phi}$	$DPF_{3\phi}$	
Load *R*	1.00	1.00	$\phi_1 = 1.00$
(VUF = 0%)			$\phi_2 = 1.00$
			$\phi_3 = 1.00$
Load *R*	0.98	1.00	$\phi_1 = 1.00$
(VUF = 18.5%)			$\phi_2 = 0.99$
			$\phi_3 = 0.98$
Load *R*	0.97	0.99	$\phi_1 = 0.99$
(VUF = 25%)			$\phi_2 = 0.98$
			$\phi_3 = 0.97$
Load *RL*	1.00	1.00	$\phi_1 = 1.00$
(VUF = 0%)			$\phi_2 = 1.00$
			$\phi_3 = 1.00$
Load *RL*	0.98	1.00	$\phi_1 = 1.00$
(VUF = 18.5%)			$\phi_2 = 0.98$
			$\phi_3 = 0.99$
Load *RL*	0.97	0.99	$\phi_1 = 0.99$
(VUF = 25%)			$\phi_2 = 0.98$
			$\phi_3 = 0.97$

voltage ripple at the DC output voltage (Δv_{C0}) under unbalanced grid voltage conditions with *R* and *RL* loads. It can be observed that the voltage ripple Δv_{C0} presents a fluctuation of 120 Hz, which is caused by the rectification process of the three-phase voltage PWM rectifier. Also notice that, under a VUF = 25% and *RL* DC-load the Δv_{C0} presents a small increment of amplitude therefore the maximum peak to peak amplitude is $\Delta v_{C0} \leq 5$ V. The DC-output capacitor filter has been designed follow the guidelines presented in [32]. Figure 10 shows the FFT analysis obtained with a FLUKE 435-II power quality analyzer (PQA) for the three current phases and their corresponding THD. Notice that, despite of the voltage unbalance factor, the harmonic distortion and the load connected to the rectifier, the proposed controller is able to maintain the total harmonic distortion less than 5%. That means that the proposed controller is capable of guaranteeing a correct performance within the limits of harmonic distortion established by standards [3–5]. In Fig. 11, the three phase voltage and line currents vectors, under unbalanced conditions and with *R* and *RL* DC-loads, are shown. It can be observed that for a VUF = 18.5% the

controller provides line currents in phase with the fundamental components of the three phase voltages. Meanwhile, if the VUF = 25%, a small displacement of the current vectors with respect to the fundamental component of the voltage vectors is produced due to the high unbalance factor. Nevertheless, the controller is able to guarantee a three phase displacement power factor ($DPF_{3\phi}$) close to 1.00 and the three phase power factor ($PF_{3\phi}$) greater than or equal to 0.95 in all cases. Table 4 summarizes the $PF_{3\phi}$, $DPF_{3\phi}$ and the PF per phase (ϕ_n) obtained by the PQA. It can be noted that the controller is able to keep a power factor $PF_{3\phi} > 0.95$ and the DPF close to 1.00 under different operation conditions.

5 Conclusion

This paper presented an adaptive current mode controller for a three-phase VSR. The main purpose of the proposed controller was to guarantee a proper line current tracking despite of the unbalanced and harmonic distortion in the grid voltage, by means of the use of the positive component of the grid voltage estimation. The controller also assures an adequate regulation of the capacitor voltage towards a desired reference. The controller was composed by two main loops, namely, current tracking loop and voltage regulation loop. The first one is formed by a proportional gain with a couple of estimators capable to deal with the uncertainties of the input filter. The last one consists in a PI controller which guarantees the delivery of a regulated voltage to the load. A relevant contribution in the controller was the introduction of three estimators. First the estimators of the series resistance and the inductance of the filter, allowed the system to be able to overcome the parametric uncertainties of the filter. Second the estimation of the positive component of the grid voltage, which allows to deliver sinusoidal line currents to the grid despite of the unbalanced and distortion conditions. Finally, experimental results were performed to validate the proposed controller in grid fault conditions.

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