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Nanometer-thin pure boron CVD layers as material barrier to Au or Cu metallization of Si

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ABSTRACT

Metallization layers of aluminum, gold, or copper are shown to be protected from interactions with silicon substrates by thin boron layers grown by chemical-vapor deposition (CVD) at 450 °C. A 3-nm-thick B-layer was studied in detail. It formed the p^+-anode region of PureB diodes that have a metallurgic junction depth of zero on *n*-type Si. The metals were deposited by electron-beam-assisted physical vapor deposition (EBPVD) at room temperature and annealed at temperatures up to 500 °C. In all cases, the B-layer was an effective material barrier between the metal and Si, as verified by practically unchanged PureB diode *I–V* characteristics and microscopy inspections of the deposited layers. For this result, it was required that the Si surface be clean before B-deposition. Any Si surface contamination was otherwise seen to impede a complete B-coverage giving, sometimes Schottky-like, current increases. For Au, room-temperature interactions with the Si through such pinholes in the B-layer were excessive after the 500 °C anneal.

1 Introduction

In this paper, we examine nm-thin pure boron layers, deposited by chemical-vapor deposition (CVD), as material barriers between silicon and metallization layers of gold (Au) or copper (Cu). The work is motivated by the potential advantages of replacing aluminum (Al) metallization with these metals in pure boron (PureB) photodiode detector technology. This is a CMOS-compatible technology used for integrating robust detectors that are highly sensitive to a wide range of wavelengths [1, 2], and they have been commercialized for the lithography wavelengths of 193 nm deep ultraviolet (DUV) and 13.5 nm extreme ultraviolet (EUV) as well as for low-energy electron detection in scanning-electron-microscopy (SEM) systems [3, 4]. Generally speaking, Al is the traditional interconnect material of choice for the 3.0–0.25 μm CMOS technology nodes. However, with the progressive miniaturization and higher

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packing density of the technology nodes beyond 0.25 μm, as well as a push towards higher and higher circuit frequencies, the Al has in many situations been replaced by metals such as Au and Cu to lower series resistance and/or improve electromigration reliability [5, 6]. All three metals, Al, Au, and Cu, react with Si at temperatures commonly used in back-end CMOS processing, or as a result of high current densities, which can be destructive, particularly when contacting ultrashallow junctions. To prevent undesirable spiking, suitable thin-film barriers to the Si have been extensively sought after. At present, TiN is the most commonly used barrier layer, either sputtered for tens of nm thick layers or deposited by atomic layer deposition for thinner conformal layers [7]. TiN has the advantage of having low electrical resistivity and high thermal stability [7, 8].

As opposed to Al, the metals Au and Cu also have the disadvantage that they readily diffuse in Si even at temperatures well below 500 °C. Both metals are deep-level contaminants in Si [9] and, therefore, shorten the carrier lifetime [9, 10] increasing the diode currents, which can adversely affect device operational performance. An extra issue with Cu interconnect is that Cu diffuses rapidly, not only in Si but also through SiO_2 at temperatures as low as 200–300 °C [11]. Here also, TiN has been extensively studied as a diffusion barrier [12, 13], along with other barrier materials that become interesting for meeting the requirements of down-scaling such as W [14], Ta [14, 15], TaSi [15], TaN [15], Ti–Si–N [16], and Ru [17].

In PureB detectors, both series resistance and bonding problems were encountered when using Al interconnect. Nevertheless, Al has been an attractive metallization for fabricating these detectors because B-layers as thin as 2 nm functioned as perfect material barriers between the Al and Si [1, 18]. For EUV detectors, the fabrication of filter- and absorber-layer stacks containing metals such as Zr, was also facilitated by having B as a material barrier to the Si [1]. Many of the PureB photodiode detector applications were successfully developed using physical vapor deposition (PVD) of pure Al [1, 4]. The photodiode itself was formed by a chemical-vapor deposition of pure boron on Si. The interaction of the B with the Si surface creates a p^+-like region that on n-type Si forms a diode with metallurgic junction depth from a few nm down to zero, depending on the Si substrate temperature during deposition. In this way, the whole Si surface becomes photosensitive, which, combined with an nm-thin pure B capping layer, provides not only high responsivity but also a robust device for withstanding high-dose exposures. For both EUV and SEM detector applications, it was also important that the B-layer was chemically resistant to aggressive cleaning procedures [19]. Three properties of the Al-on-B system led to the development of a cost-efficient and potent process flow for producing detectors with PureB-only light-entrance windows. For the first, Al formed both good ohmic contact and good adhesion to the B-layer. Second, nm-thin B-layers prevented reactions of the Al with the underlying Si that otherwise cause pitting for alloying temperatures in the range of 400–500 °C [18]. Third, before alloying, the Al could be removed selectively to the B by resist patterning and a combination of plasma etching and wet landing in a diluted HF solution [4].

For very large detectors, several cm in size, and imaging arrays of, for example, single-photon avalanche diodes (SPADs), lower resistivity, and better electromigration properties that can be obtained with Al are often desirable. Moreover, Al is a soft metal that readily oxidizes, thus becoming covered by a hard non-conductive Al_2O_3 layer. Due to this, bonding to the Al pads decreased the yield because any excessive force needed to procure a good bond was able to damage the underlying oxide, and possible solutions in the detector design would have increased costs and complexity. Therefore, it was of interest to explore the application of metals like Au or Cu. The CVD PureB layers have already proven to be very efficient material barriers to Al, with the most robust, compact layers, as thin as 2 nm, being grown at a substrate temperature of 700 °C. Despite a high B-layer resistivity, such thin layers allow diode tunneling currents with which the trade-off between B-layer integrity and series resistance is acceptable for many photodiode applications [1, 2].

At 450 °C, the B surface roughness is higher, about 1 nm, and the compactness lower [20], and at least 3 nm was needed for Al barrier purposes. Since this layer is of great interest as a back-end CMOS-compatible deposition, it was chosen here as a "worst case" layer for testing the barrier potentials of B with respect to Au and Cu. In addition, the metals were deposited by electron-beam-assisted physical vapor deposition (EBPVD) with the substrate at room temperature which is not beneficial for a good adhesion.

Nevertheless, by using this method, all three metals, Au, Cu, and Al, could be deposited and patterned in the same way by using a lift-off process. The B-layer barrier properties were analyzed by imaging techniques such as optical microscopy, atomic-force microscopy (AFM), and high-resolution transmission electron microscopy (HRTEM). In addition, the *I–V* characteristics of PureB diodes fabricated with and without metal contacts were studied experimentally and via device simulations.

2 Theoretical considerations

The main parameter used here to characterize PureB diodes is the minority carrier electron current density, J_e, which tells us how well the PureB anode is capable of suppressing the electron injection from the substrate. The lower the J_e, the lower the dark current. The relationship between J_e and the concentration of fixed negative charge, N_I, at the B-to-Si interface, was studied experimentally and via simulations in [21]. It was concluded that for a B-deposition temperature of 450 °C, there would be no actual B-doping of the bulk Si, but the experimental PureB diodes without metal contacting had an electron saturation current density, J_{se}, at room temperature (RT) of about 20 pA/cm^2 to 30 pA/cm^2. In the simulations, this was found to correspond to the suppression of electron injection achieved by the potential barrier that could be created by an $N_I \approx 5 \times 10^{13}$ electrons/cm^2. For very thin layers, less than about 3 nm, the presence of a metal layer on the PureB had the effect of lowering this barrier to electrons. The lowering was stronger, the lower the work function, ϕ_M, of the metal.

As an example, to illustrate the expected current trends, we applied the same simulation parameters for bulk B and Si as used in [21] to make a 1-dimensional simulation of the PureB diode characteristics when contacted by metals with different work functions. In Fig. 1, a simulation is shown of the diode saturation currents as a function of the thickness of the B-layer when varied from 0.25 to 5 nm. The metal work functions were set to be 4.1 eV, 4.7 eV, and 5.1 eV to represent Al, Cu, and Au, respectively [22]. The hole saturation current density, J_{sh}, is determined by the integral doping of the *n*-Si substrate and is, therefore, the same for all samples. The simulation indicates that if the B-layer is thicker than 3 nm, then the hole current will dominate the total current in all 3 cases. The electron saturation current, J_{se}, of the Al-coated device goes rapidly to Schottky-like currents as the B-thickness goes below 2 nm, followed by the Cu at 1 nm, while the Au remains within a decade of the hole current even for a B-layer thickness as low as 0.25 nm.

In this simulation, the current levels will go to the ideal levels as governed by the metal-Si Schottky barrier height (SBH) when the B-layer thickness goes to zero, i.e., the Schottky diode currents will follow the same trend as the PureB diode currents, being highest for the lowest work-function metal. However, in reality, chemical reactions at the metal–silicon interface will often modify the experimentally observed SBH [23]. Much work has been devoted to developing layers between the metal and Si to disrupt this effect and nevertheless get either a low SBH, mainly for the purpose of making more low ohmic contacts [24], or, oppositely, a high SBH for increasing hole injection and/or reducing electron injection [25]. In this paper, it was also demonstrated that in simulations of experimental results, the effect of the interface and surrounding (charged) layers can often be reproduced by assuming the diode to have an appropriate SBH and surface recombination velocity. Alternatively, for PureB diodes, the model defining an interfacial fixed negative charge layer has been successful in describing a vast amount of experimental data [21, 26]. The bulk B-parameters of these very thin B-layers are not well known, but because the layers are so thin, the exact B-parameters may only have a small impact on the diode *I–V* behavior as compared to the external influence of parameters like N_I and ϕ_M. This was concluded from simulations presented in [27].

3 Experimental material and methods

All the layer stacks were investigated after deposition on Si substrates patterned with test structures, the processing of which is described in [28]. The basic PureB diode test structure is illustrated in Fig. 2, showing that the B-layer was deposited selectively on the Si through windows etched in a thermal oxide isolation layer. The devices were designed to enable electrical measurement directly after B-deposition, i.e., no metallization was needed for device probing. Instead, probe contact could be made to implanted

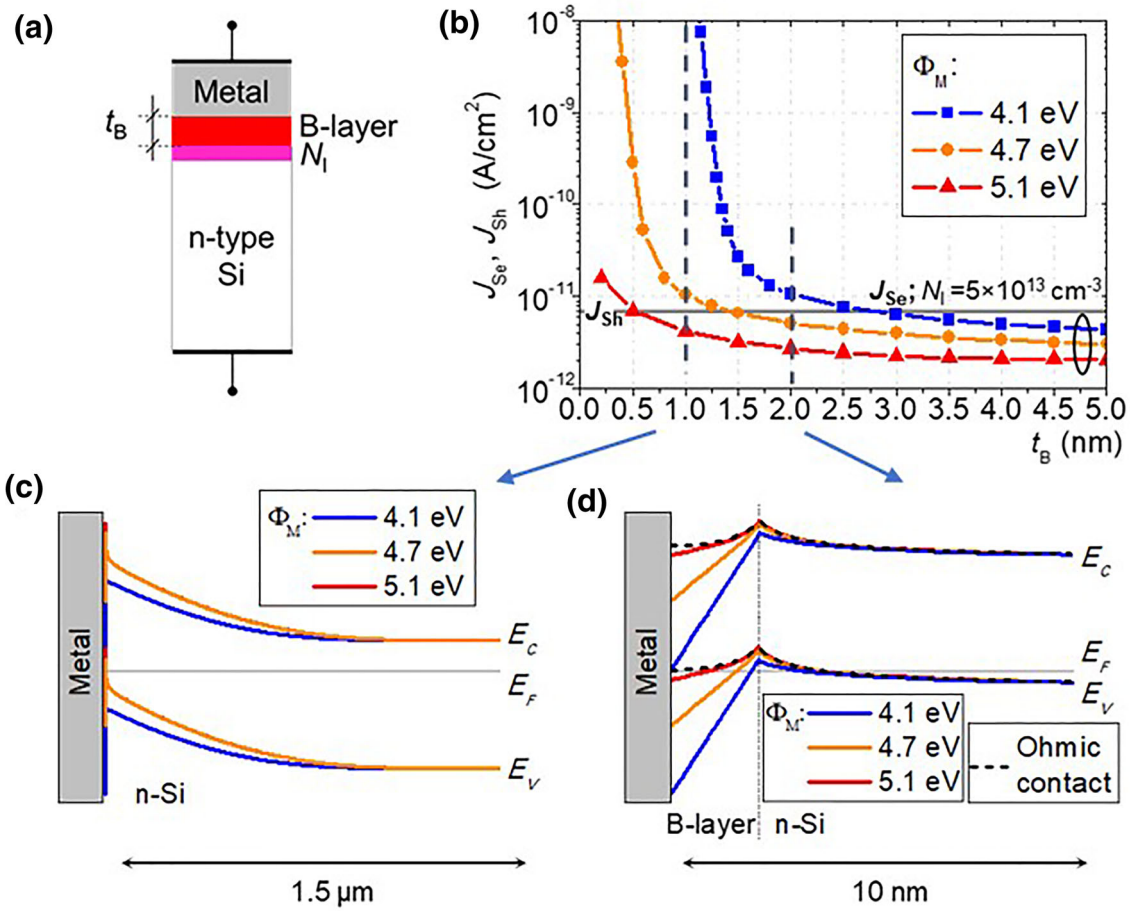

Fig. 1 **a** Basic 1-D structure of the simulated PureB diodes. **b** The hole and electron current densities as a function of the B-layer thickness, t_B, for 3 metal work functions representing Al (4.1 eV), Cu (4.7 eV), and Au (5.1 eV). The corresponding band diagrams are shown for 2 different widths at the B–Si surface region of **c** 1.5 µm and **d** 10 nm

p^+-regions that contact the PureB p-type regions via the Si. Implanted p^+-regions were also used to form guard rings around PureB structures so that the effect of perimeter currents could be isolated and eliminated when evaluating the laterally uniform properties of the PureB diode regions. The test structures enabled the extraction of diode I–V characteristics including the electron saturation current component, I_{se}, which is found by a differential method where the current in neighboring implanted p^+n diodes with the same layout is subtracted from the PureB diode current. This method works well because the current of the PureB diodes was measurably higher than the hole current, while the electron current of the implanted p^+n diodes was 10–100 times lower, depending on the exact n-substrate doping.

The B-deposition was performed on a whole 100-mm test wafer by CVD in an ASM Epsilon 2000 Si/SiGe epitaxy system equipped with diborane (B_2H_6) gas as precursor and nitrogen as carrier gas, following the recommendations given in previous work [1, 29] to achieve a clean Si surface. Therefore, the wafer was given an HF dip to remove native oxide and kept in the load lock for 1 h before depositing at a temperature of 450 °C using low flow rates that ensured B-deposition selectively on the open Si regions. The targeted B-layer thickness was 3 nm, which was checked by HRTEM. Using spectroscopic ellipsometry as described in [20], the thickness of the B-layer was found to be 2.85 nm with a roughness of 1.97 nm, which are typical values for layers grown at 450 °C. Previous work has shown that this roughness is associated with a less compact B-composition than that of layers grown at higher temperatures [20].

The wafer with the as-deposited B-layer was electrically characterized, after which it was broken into small pieces approximately 2 × 2 cm^2 in size. A lift-

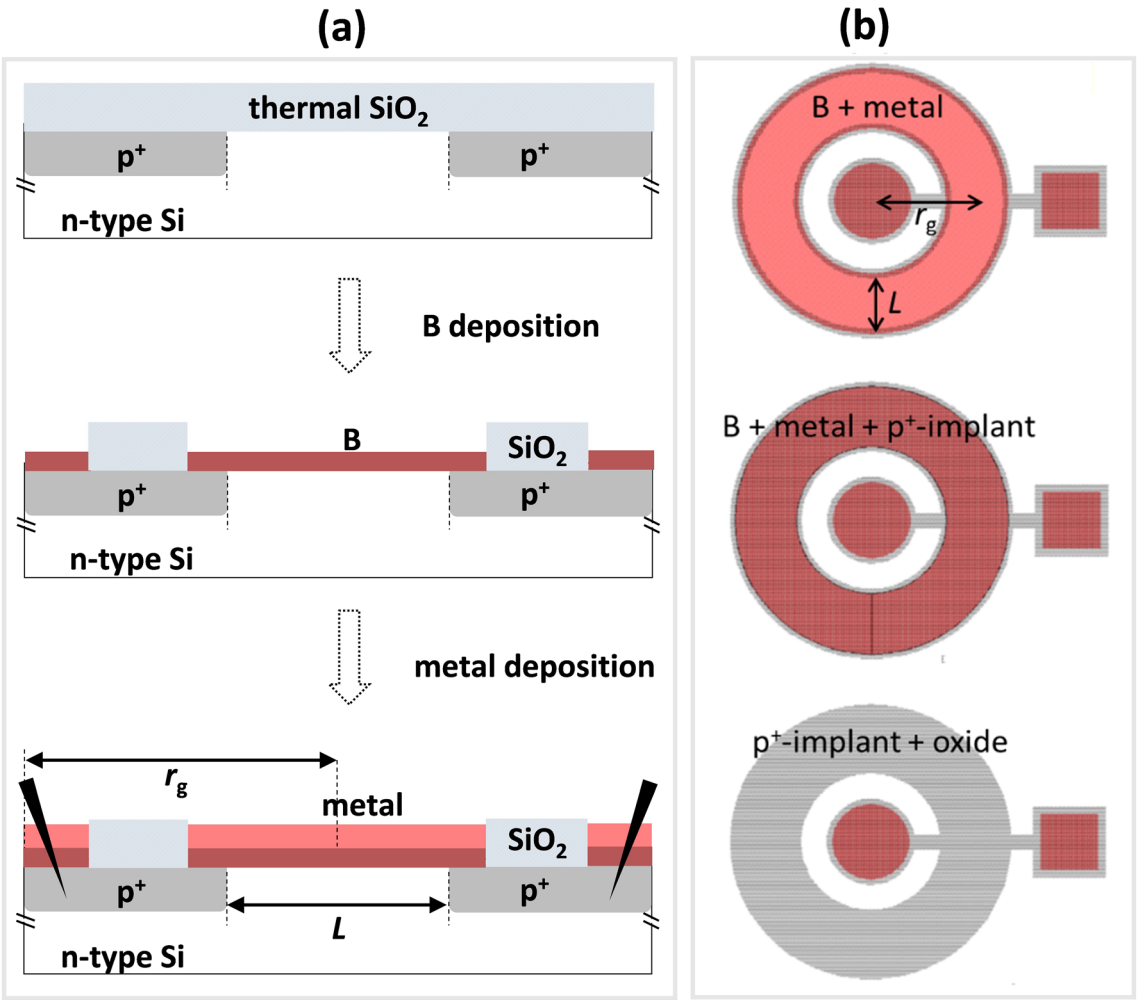

Fig. 2 **a** Schematic process flow for the fabrication of PureB diodes indicating the probe contacting via implanted p^+-regions, with and without metallization. **b** Top view layout of the basic ring-shaped devices of varying width, L, and radius, r_g, for rings covered with metal and B-layers, one ring with and one without an implanted p^+-region under the whole ring, and a ring with only an implanted p^+-region covered with oxide

off mask was patterned to define the region where metal was to be deposited, using a spin-coated 1.7-µm-thick positive photoresist. The metals, Al, Au, or Cu, were deposited without intentional substrate heating, corresponding to a substrate temperature of about 50 °C, in a BAK-600 EBPVD system at 1.5×10^{-7} mbar process base pressure. For each deposition, test-wafer samples with and without B-deposition, were deposited together in the same run. Lift-off was performed in an acetone solution, after which the samples were rinsed in demi-water followed by blow drying in dry N_2 gas. The samples were annealed sequentially at temperatures of 200 °C, 400 °C, or 500 °C for 30 min in a bell-jar setup with a vacuum less than 10^{-3} mbar. In this way, all three metals, Au, Cu, and Al, could be deposited and patterned in the same way. A list of the processing parameters for the electrically characterized samples is given in Table 1. It should be noted that test wafers, before metal deposition, were processed in CMOS-compatible cleanrooms. Up until the PureB deposition, our MESA+ ultraclean process line was used, while the B-layer was deposited by a commercial provider. In contrast, the metal patterning, deposition, and annealing were performed in MEMS-lab environments without CMOS compatible tools. Therefore, after the B-deposition, the samples were no longer protected from undesirable contamination that could have an effect on the electrical behavior of the diodes.

The diode n-region was contacted via the back of the wafer which was not metallized. This and the

Table 1 List of fabrication parameters of samples that were electrically characterized, including best-value electron saturation current densities, J_{se}, extracted from the low-voltage near-ideal forward I–V characteristics, and J_s for p^+n diodes

Diode name	B-barrier layer	Metallization	Metal thickness (nm)	30 min anneal temperature (°C)	J_s or J_{se} (A/cm^2)
Al[500]	No	Al	150	500	$J_{se} = 5 \times 10^{-9}$
Au[500]	No	Au	120	500	$J_{se} = 1 \times 10^{-6}$
Cu[500]	No	Cu	120	500	$J_{se} = 5 \times 10^{-5}$
Al–B[500]	Yes	Al	150	500	$J_{se} = 3.7 \times 10^{-11}$
Au–B[400]	Yes	Au	120	400	$J_{se} = 3.3 \times 10^{-11}$
Au–B[500]	Yes	Au	120	500	$J_{se} = 3.3 \times 10^{-11}$
Cu–B[400]	Yes	Cu	120	400	$J_{se} = 5 \times 10^{-11}$
Cu–B[500]	Yes	Cu	120	500	$J_{se} = 7 \times 10^{-11}$
PureB diode	Yes	–	–	–	$J_{se} = 2.0 \times 10^{-11}$
Implanted p^+n diode	Yes and no[(a)]	Al	150	500	$J_s = 1.8 \times 10^{-11}$
Implanted p^+n diode	Yes and no[(a)]	Au	120	500	$J_s = 2.4 \times 10^{-11}$
Implanted p^+n diode	Yes and no[(a)]	Cu	120	500	$J_s = 1.9 \times 10^{-11}$

[(a)]Implanted p^+n diodes were fabricated with and without the isolation oxide being removed. When removed, the open region was coated with a metal-B layer-stack or just the metal, depending on the type of sample

direct probing of the Si led to a variable, high series resistance, particularly for small sample pieces that had relatively small contact area to the probe-station chuck. Therefore, this study focuses on the low-voltage diode characteristics that are not attenuated by the series resistance and nevertheless allow the determination of the diode saturation currents.

In many ways, these experimental conditions represented a "worst case scenario" for testing the barrier potentials of B-layers. For the first, the ~ 3 nm B-layer thickness was found to be the minimum 450 °C deposition thickness suitable for use in PureB photodiodes where the B-layer surface was coated with sputtered Al. This Al was removed locally by wet etching in diluted HF selectively to the B to open light-entrance windows [4]. With a deposition temperature of 700 °C, a B-layer found to be 2.2 ± 0.4 nm thick by ellipsometry was sufficient to prevent interactions with the Si, but as the deposition temperature was decreased, the B became more loosely bound and the layers had a much higher surface roughness. The latter can aggravate adhesion difficulties, which are also more problematic when the metals are deposited by EBPVD at room temperature rather than at higher temperatures.

It was overly evident that, unlike with Al, the Au and Cu samples suffered from poor adhesion of the as-deposited metal. After lift-off, the metal in small closed structures had often been ripped off, and peeling-off could be seen around the edges of other structures. Nevertheless, enough structures remained intact, and annealing was performed to promote better adhesion. At 200 °C, the adhesion was improved but the metal would still flake off the bond pads upon probing. At 400 °C, these adhesion problems were alleviated and it continued to be good also after the 500 °C anneal. The surface of these metal-coated samples was inspected by optical microscopy and AFM.

4 Surface analysis

All three metals have interactions with the Si when deposited directly on the bare surface and exposed to anneal steps. In Fig. 3, examples of optical microscope inspection are shown for samples without the B-layer, Al[500], Au[500], and Cu[500], 3 months after the 500 °C anneal was performed. From an extensive literature on experimentation with these metal-Si systems [30], it is known that the final outcome of such anneals will depend on the exact thermal treatment where the cool-down time can be decisive for the structuring of the alloyed regions. In our case, the images reveal trends that are typical for each of the 3 metals. We explicitly paid attention to the differences between the implanted p^+-regions and non-implanted regions because p^+-regions are

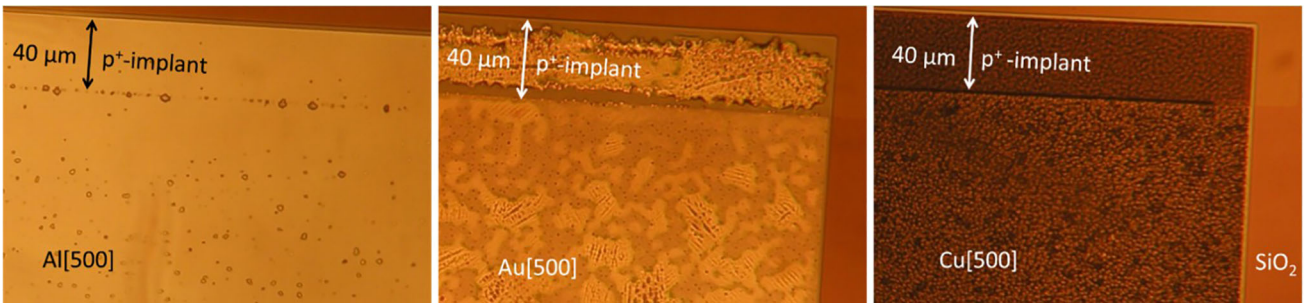

Fig. 3 Optical microscope images of metals deposited directly on Si in an oxide window after alloying at 500 °C. The window has a 40-µm-wide overlap with a p^+-implanted region. Taken 3 months after the anneal

commonly used for gettering metal contamination [31, 32]. Moreover, previous experiments using the same type of PureB diode test structures have shown that depositing on the implanted p^+-regions sometimes led to a weakening of B bonds [29]. This was seen in tests where the devices were exposed to the Si wet-etchant tetra-methyl ammonium hydroxide (TMAH). When the TMAH was able to seep through the PureB layer, it attacked the Si, giving a pitted surface of inverted pyramids typical of wet Si etching. This was not observed for the 450 °C B-deposition studied here. However, for a similar 400 °C deposition, we found considerable etching of the Si in the implanted p^+-regions, but none at all in the non-implanted regions [29]. Such a difference was also observed on samples with 700 °C B-deposition if the Si had been exposed to non-optimal surface treatments before deposition. Therefore, there was reason to suspect that the B-layer might be a less efficient barrier to the metals on the implanted surfaces.

The Al-coated samples were all shiny and smooth, and as seen in Fig. 3, there was no clear difference between the implanted and non-implanted regions. The Al does attack the Si, and this is seen here as a not very dense pattern of spots that were identified as pitting of the Si. At the boundary between the implanted and non-implanted regions, a relatively high density of pits arranged in a line surrounded by a tens-of-micron-wide region practically void of pits. This line corresponds to a defected Si region where the end-of-range implantation damage surfaces, and the energy needed for a Si reaction with Al is reduced. On oxide-covered regions no pits were observed. Apparently, a more extensive pitting was inhibited because the dissolved Si migrates quickly through the Al, saturating a large Al region around each pit and thus preventing further Al–Si reactions. This result is also in line with the well-established advantage of Al-metallization, i.e., when sputtered from an Al-target saturated with ~ 1% Si, reactions with the Si substrate can be suppressed [33].

In contrast, the Au-coated samples display a very aggressive interaction with the Si. In Fig. 3, much of the Au is seen to coalesce in large grains often with distinct alignment patterns while equally large areas are cleared of any visible metal and Si pitting is revealed. The pits are smaller and more densely distributed than for the Al case. In addition, the implanted region looks quite different with the central region being completely covered in Au while a 5-µm-wide region inside the perimeter is cleared of both Au and any signs of pitting. Presumably, the gettering properties of the implanted p^+-region reduces the diffusivity of the Au in the Si, promoting grain formation rather than pitting. In Fig. 4, AFM images of non-implanted Si surface regions with visible pits are shown. The surface morphology is no longer flat, indicating strong Au–Si reactions, and the pits are square with the orientation and cavity shape typical of the spiking of Si with such metals.

The Cu[500] samples also display aggressive interaction with the Si, forming a pattern of intertwining strings of bumps that are smaller in size on the implanted rather than the non-implanted regions. This bumpy nature is also seen in the AFM image shown in Fig. 5. The difference between the two regions is no doubt also related to the gettering properties of the p^+-region since the diffusivity of the Cu will be lower there [31].

The Au and Cu samples with B-barrier layers were first annealed at 400 °C. Visually their appearance was just like that of the as-deposited samples, with shiny and smooth surfaces on all three of the different substrate regions. These samples and the Al–B

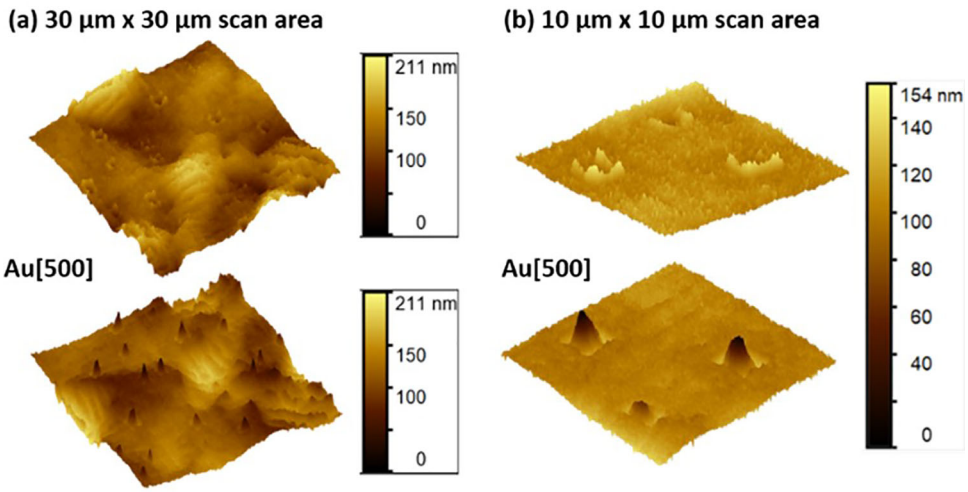

Fig. 4 AFM images of non-implanted Si surface regions with visible pits, for the same Au[500] sample as displayed in Fig. 3; **a** 30 × 30 µm^2, and **b** 10 × 10 µm^2 scan area

sample were then annealed at 500 °C, upon which their shiny, smooth appearance did not change. However, in contrast to the Al and Cu samples, the Au sample did visibly change in time. An inspection after 3 months shelf time revealed that some surface regions of an Au–B[500] sample processed near the wafer edge had changed from Au-covered to bare Si in appearance. This was no doubt related to the deficient nature of our wet-processing methods at the wafer edge which allows particle contamination that may inhibit a perfect B-coverage of the Si. An example of such defected regions is shown in Fig. 6 for a set of ring diodes. The mechanisms behind these changes will be discussed in connection with the electrical measurements presented in Sect. 5. After the first 3 months storage period, the appearance remained stable on both the defected regions and the shiny, smooth Au-covered regions. A HRTEM image taken in the middle of one of the latter regions is shown in Fig. 7, confirming that the 3-nm-thick B-layer is completely separating the Au from the Si.

5 Electrical characterization

Typical diode *I–V* characteristics of the samples without a B-barrier layer, annealed at 500 °C, are shown in Fig. 8, where also a comparison is made to the *I–V* characteristics of a non-metallized PureB diode and an implanted p^+n diode. The latter two diodes both have ideal characteristics, and the

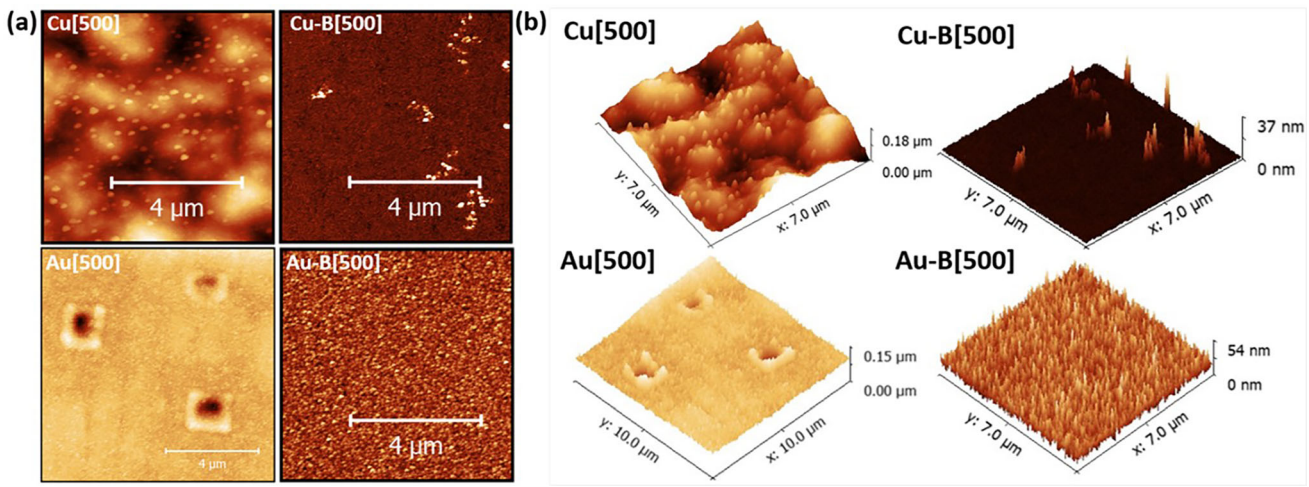

Fig. 5 Plan-view (**a**) and 3D (**b**) AFM images of Au[500], Au–B[500], Cu[500], and Cu–B[500] samples, taken 3 months after the 500 °C anneal on non-implanted Si regions. The Au–B[500] image is taken in the middle of a tens-of-micron-large surface region without any visible defects

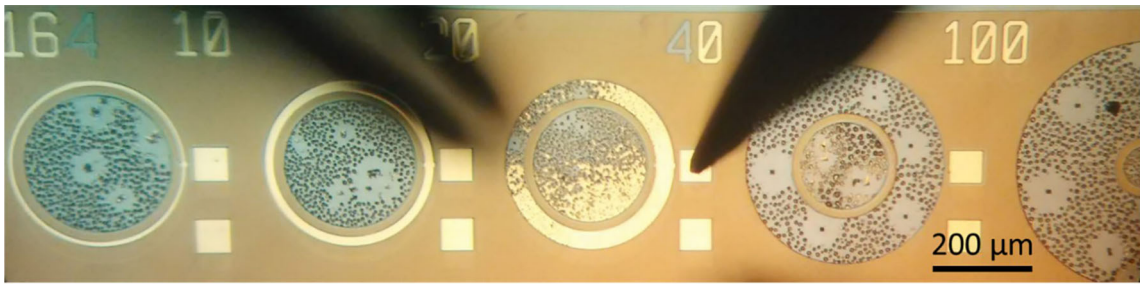

Fig. 6 Optical microscope image of a set of ring-structured diodes of the sample Au–B[500], taken 3 months after the 500 °C anneal. Two probe needles are visible; the one to the right is contacting a p^+-implanted measurement pad that connects to a 40-µm-wide PureB ring-diode via the Si

current level of the PureB diode is only slightly higher than that of the implanted diode. As expected, the current levels in the Schottky diodes are decades higher than the p^+n diode levels. A comparison to the simulation results shown in Fig. 1 reveals that the Schottky current levels predicted by only considering the work-function difference between the Si and the metal do not correspond to the experimental situation of Fig. 8. This is not surprising since the metal-Si reactions can create interface layers that have properties very different from the individual bulk materials. For example, Al is a *p*-dopant in Si and it is well known that at temperatures from 400 to 500 °C, alloying of Al and Si can lead to *p*-doping of the Si [34]. Therefore, instead of having the highest current levels, corresponding to the lowest work function of 4.1 eV, the Al[500] Schottky diodes have the lowest current levels that are only about 2 decades higher than the implanted p^+n junction diodes. The Au[500]

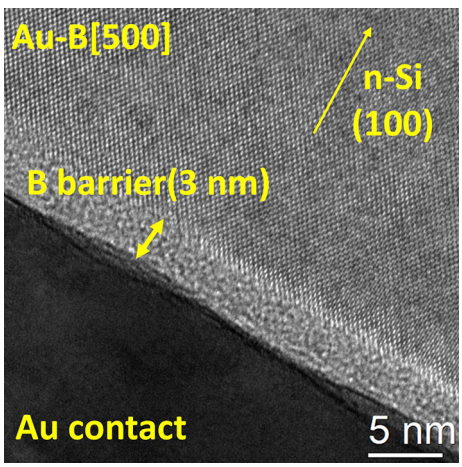

Fig. 7 HRTEM image of the sample Au–B[500], taken 3 months after annealing at 500 °C in the middle of a tens-of-micron-large non-implanted Si surface region without any visible defects

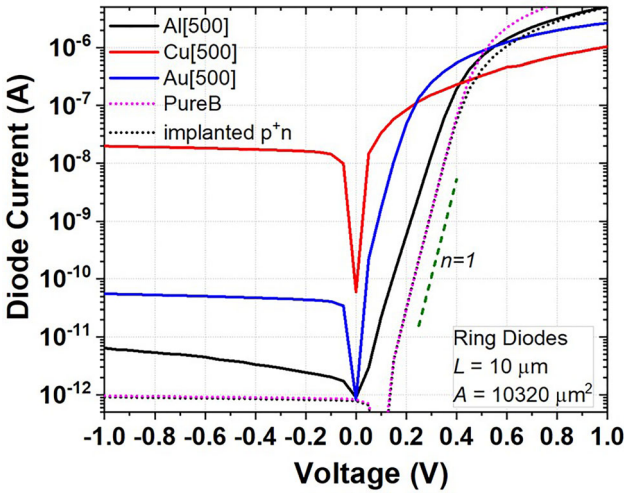

Fig. 8 Measured *I*–*V* characteristics of Schottky diodes for the Al[500], Au[500], and Cu[500] samples compared with those of non-metallized PureB diode and implanted p^+n diode

currents are 2 decades higher than those of the Al[500] diodes, while the Cu[500] currents are yet another 2 decades higher. Both display clear *p*-type Schottky behavior with relative current levels that could reflect the work-function difference. However, besides the influence of interfacial layers, these two metals also create midgap states in Si that could cause current increases.

Figure 9 displays *I*–*V* characteristics for PureB diodes after coating with each of the 3 metal types, and a comparison is made to those of neighboring implanted p^+n diodes. All characteristics are close to ideal with current levels decades lower than the corresponding Schottky diodes. The Al and Au diodes have ideality factors that are practically $n = 1$. In contrast, the Cu diodes display a small non-ideal leakage current that increases as the PureB diode area increases. This is clearly seen in Fig. 10 for a set of

ring diodes with L = 10 μm, 20 μm, 40 μm, 100 μm, and 200 μm. The perimeter of these ring diodes is constant and also protected by the implanted p^{+}-n guard ring, so it is eliminated as the source of the non-ideality. Factors that are likely to augment the current levels are contamination of the Si from either the processing equipment or, in the case of Au or Cu, from the metal itself. In addition, stress from changes in the metal morphology during annealing and associated cool down can play a role. Al and Cu layers are notorious for pushing up hillocks to relieve stress during anneal-induced grain formation [35, 36]. However, the present metal layers are quite thin, so grain formation is more likely to be associated with the creation of voids between the grains. In any case, all these factors could damage the B–Si interface and give non-idealities, which, however, are only significant in the case of Cu. In Fig. 11, the I_e at a forward bias of 0.3 V is plotted for all the diodes as a function of L, which is proportional to the PureB-only diode region area of $A = L \times 1032$ μm^2. For all 3 metals, the ideal part of the diode current is about the same, and about a factor 2 higher than the value for the non-metallized PureB diodes. The values for the diode current of the implanted $p^{+}n$ diodes on each of the samples are also shown in Fig. 11. These currents were not visibly affected by the metallization and anneal steps, whether the implanted region is covered with an oxide or a PureB region as illustrated in Fig. 2. Therefore, they do not directly give any information on the small current increases seen for the metallized PureB diodes, possibly because detrimental effects are reduced when the depletion region is moved away from the B–Si interface or because the presence of a full coverage of the p-type implant has some benefits with respect to gettering of contaminants.

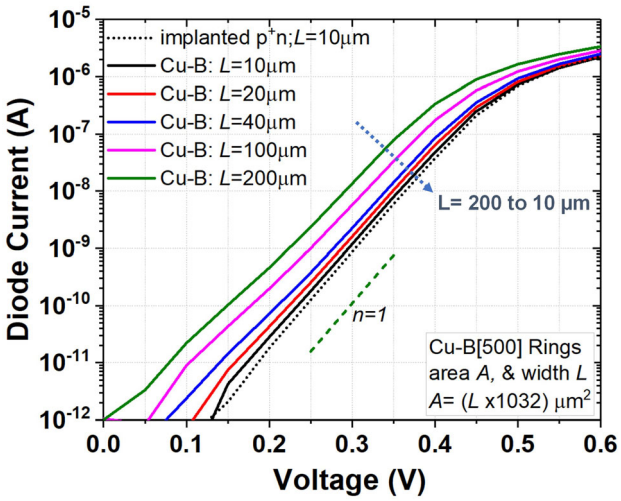

Fig. 10 Measured I–V characteristics of Cu–B[500] ring diodes, 3 months after a 500 °C anneal, as a function of ring width, L, compared to those of an implanted $p^{+}n$ diode with width L = 10 μm

In Table 1, a list of the J_{se} for the different samples is given along with the corresponding J_s of the

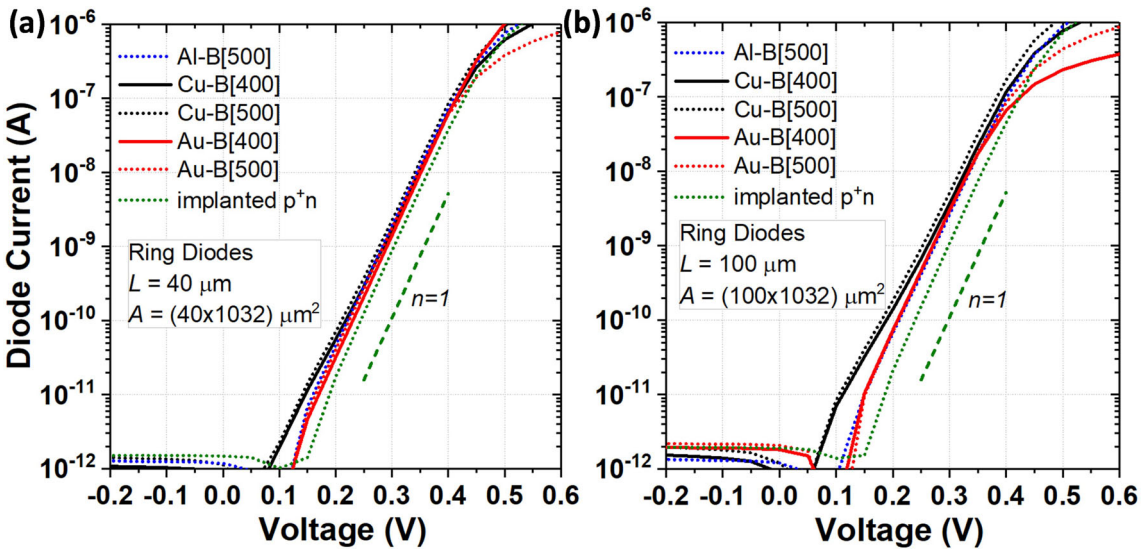

Fig. 9 Measured I–V characteristics of Al–B[500], Au–B[400], Au–B[500], Cu–B[400], and Cu–B[500] PureB diodes, compared to an implanted $p^{+}n$ diode of the same geometry. Ring-shaped diodes with L = 40 μm or 100 μm. The samples annealed at 500 °C were measured 3 months after the anneal step

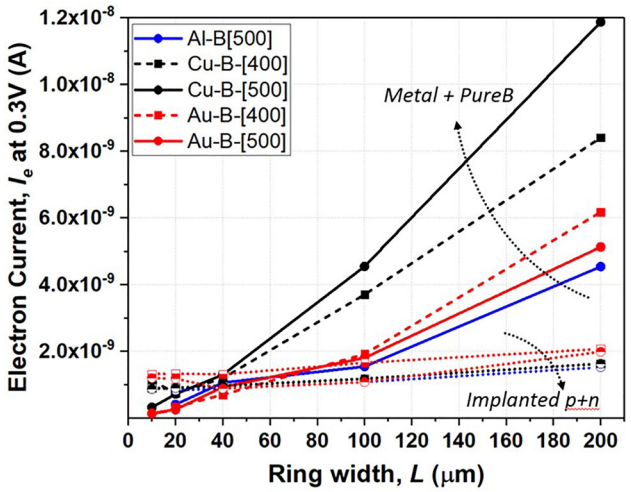

Fig. 11 The electron current at a forward bias of 0.3 V for Al–B, Au–B, and Cu–B PureB ring diodes compared to the diode current of neighboring implanted p^+n diodes, as a function of the ring width L, and for anneal temperatures 400 °C and 500 °C

implanted p^+n diodes. The calculation of these saturation currents is based on the lowest current values, "best" values, found among all the measured diodes. This approach is based on the observation that any imperfections in the fabrication of the metallized PureB diodes will lead to an increase of the current with respect to the non-metallized ones. Analyzing the statistical spread would in this case provide information on the quality of the processing, which, as noted, was not ideal and therefore not of pertinent interest.

As discussed in relationship to Fig. 6, samples taken from the edge of the wafer had B-layers with defects that only became optically discernable on the Au–B[500] sample, 3 months after the 500 °C anneal. Such a dramatic change in the otherwise shiny, smooth Au coating was not observed after the 400 °C anneal, even after long shelf life, nor on the samples from the center of the wafer annealed at 500 °C. For both these samples, practically all the measured PureB diodes had *I–V* characteristics that were ideal and stable in time, just like the examples shown in Fig. 9. For the defected Au–B[500] sample, the *I–V* characteristics were often degraded, as shown in Fig. 12 for measurements of the set of rings in Fig. 6. The 2 smallest diodes with no visible pits have well-behaved characteristics, but with about 3 times higher current levels than seen for the devices shown in Fig. 9. The two largest diodes have more than a decade higher current and display a kink at about 0.45 V after which the current reduces to PureB-like levels. Such a kink was previously observed for Al-metallization of large area PureB diodes with thin B-layers and was related to a few pinhole-sized defects where the metal could get close to or even contact the Si [21]. For the defected Au-coated sample, it is clear that the Au has found structurally weak spots or pinholes in the B-layer through which it has come into contact with the Si, etched visible pits, and, under the influence of the dissolved Si, migrated large distances along the surface of the otherwise closed B-layer. Most of the pits had a square-shaped surface indicating the morphology of inverted pyramids. It was possible to measure the sidewall length of the pit squares and relate it to the area around the pit that was cleared of any visible Au grains. The boundaries of this area are marked by red ellipses in Fig. 13, where the area is plotted as a function of the sidewall length, displaying a clear linear relationship. This suggests that the growth of the pit depends on how much Si can dissolve in the Au before competing coalescence processes that form Au–Si grains, cut off the Au supply. This room-temperature Si-assisted metal-mediation process made the identification of imperfections in the B-layer very easy. For the other metals, changes in the morphology could not be identified through visual inspection even when supposedly defected PureB samples were used and identified by electrical measurement.

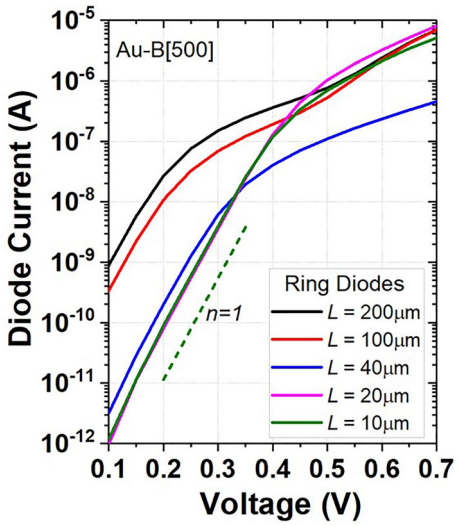

Fig. 12 Measured *I–V* characteristics of the set of Au–B[500] ring diodes with visible Au–Si interactions shown in Fig. 6

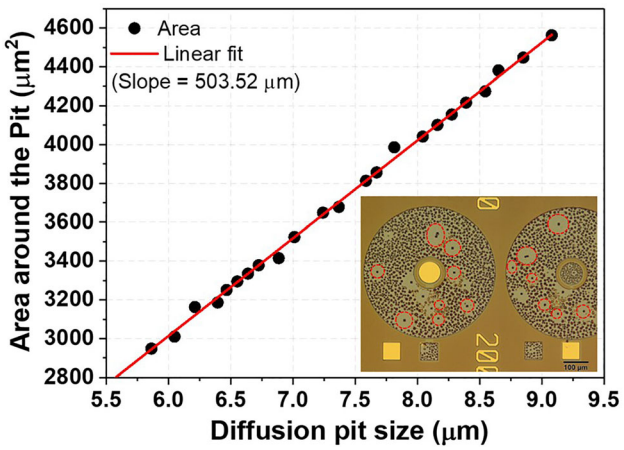

Fig. 13 The area of smooth Si around pits, indicated by red ellipses in the microscope image of the inset, as a function of the pit size for Au–B[500] diode surfaces where the Au has diffused into the Si

6 Conclusions

By studying the *I–V* characteristics of PureB diodes, it has been experimentally verified that pure boron CVD layers as thin as 3 nm and fabricated at the BEOL-compatible temperature of 450 °C, are effective material barriers between Si and the metals Al, Cu, and Au for post-metal processing temperatures up to 500 °C. The fabricated PureB diodes were compared to Schottky diodes fabricated with each of the metals deposited directly on the Si and annealed at 500 °C. The electron saturation current levels in metallized PureB diodes were decades lower than those of the Schottky diodes and for Al–B and Au–B samples within a factor 2 higher than the non-metallized PureB diode values of about 20 pA/cm^2. For Cu, the values were slightly higher due to a small non-ideal area-dependent current component. All these very small current increases were possibly related to contamination of the Si substrates during exposure to the metal-contaminated deposition and anneal equipment, or to stress-related damage to the B-Si interface caused by the metal anneal steps.

Metallized diodes on test-structure samples known to have defected B-layers, revealed that structurally weak B-bonded regions and pinholes would allow the metal to approach the Si causing current increases. Occasionally, very prominent kinks were observed in the forward *I–V* characteristics indicating that pinhole-sized Schottky diodes were formed. Simulations suggested that local thinning of the B-layer could also give significant current increases that would be higher the lower the work function of the metal, but overall, no clear relationship was found between the current levels and the work function. For the Au-coated B-layers annealed at 500 °C, the presence of Si pitting through pinholes became visually evident a few months after fabrication when large areas of B-coated Si were seen to be cleared of Au in the region surrounding a pit. The pit size was proportional to the area of the Au-free regions.

The fact that all 3 metals, when deposited on defect-free B-layers, result in practically the same PureB diode *I–V* characteristics, is one more manifestation of the efficiency with which an interfacial, high-concentration layer of negative fixed charge can be instrumental in realizing extremely shallow p^+n-like junctions with deep-junction-like saturation currents. Furthermore, this research once more emphasizes the importance of having a clean defect-free Si surface if nanometer-thin B-layers are to be deposited and used for PureB (photo)diode fabrication with optimally low current levels.

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Compliance with ethical standards

Competing interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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