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Editorial

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With 2019, we welcome Luca Cassano, Behnam Ghavami and Naghmeh Karimi to the Editorial Board of *JETTA*. Their biographies appear on the following pages. Leaving the Board after several years of service are Yiorgos Makris and Matteo Sonza Reorda.

Peer reviewing is an essential part of *JETTA*'s editorial policy. We acknowledge the contributions of our reviewers and thank them for devoting their expertise and time to serve the profession. A list of those who completed reviews for *JETTA* in 2018 appears in this issue.

This issue contains nine articles, including two *JETTA Letters*. The topics discussed are fault tolerance, reliability, fault modeling, radio frequency testing, aging and verification. Papers appearing as first, second, fourth and sixth are expanded versions of those presented at the *Nineteenth IEEE Latin-American Test Symposium* (LATS) during March 12–16, 2018 in São Paulo, Brazil. *JETTA* Editor Leticia M. B. Poehls, who has a longstanding association with LATS, conducted the peer reviewing of the journal versions of the four papers.

To start, we have three papers that focus on fault tolerance and reliability. The first paper implements time-redundancy in a processor using duplicate execution of instructions to detect an error caused by single event upset (SEU). The system recovers from error by rolling back to the last checkpoint. Authors are Villa from Federal Institute of Rio Grande do Sul, Brazil, Travessini from Federal University of Santa Catarina (UFSC), Brazil, Goerl and Vargas from Catholic University - PUCRS, Brazil, and Bezerra from UFSC, Brazil and LIRMM, France.

The second paper considers the reliability of on-chip networked multi-processors. Since commercial off the shelf (COTS) components are used, the authors achieve fault-tolerance by implementing a software module added to the real-time operating system. The level of fault-tolerance is customized based on the need of the application. Contributors are Avramenko and Violante from Politecnico di Torino, Torino, Italy.

The third paper addresses the reliability concerns of a radio frequency identification (RFID) system. The authors set up the network simulator NS2 for fault injection and fault detection in RFID devices conforming to the Electronic Product Code (EPC) standards. The NS2 is then used to study performance of various security and robustness algorithms. Researchers reporting this work are Benfraj, Beroulle and Fourty from University of Grenoble Alpes, Valence, France, and Meddeb from University of Sousse, Sousse, Tunisia.

The fourth paper discusses modeling and test of resistive short defects. A node shorted to ground or to VDD, is a defect if it causes some logic state in the circuit to change. For a short to be a defect, its resistance should be below a threshold value defined as the *critical resistance*. In this paper, the critical resistance is modified using Monte Carlo characterization of the cell library for random process variations. Illustrations include 28 nm Bulk and FDSOI technologies. Contributors are Karel, Azaïs, Comte, Gallière and Renovell from LIRMM – CNRS, University of Montpellier, Montpellier, France.

RF testing is the topic in the fifth paper, written by Ahmad and Dąbrowski from Linköping University, Linköping, Sweden. The authors design a two-tone RF signal generator in 65 nm CMOS technology for on-chip measurement of intermodulation product (IP).

In the sixth paper, Gomez from Universidad Manuela Beltrán, Santander, Colombia and Champac from National Institute for Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico visit the subject of guardbanding against process variation and aging. They argue that a worst-case gate-sizing method amounts to wasteful overdesign resulting in area and performance costs. The proposed workload aware aging analysis, new gate-sizing metrics and various heuristics minimize overdesign while maintaining the required guardband.

The seventh paper presents a verification methodology employing a simulation and regression based procedure. The

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system function is expressed as a set of executable segments, each with its starting checkpoint. The proposed strategy tries to increase the coverage of segments with minimal set of tests. The author is Cieplucha from Warsaw University of Technology, Warsaw, Poland.

We end the issue with two *JETTA Letters*. The first of these presents a physical layout for a flip-flop protected against single event upset (SEU). Contributors are Wang, Dai, Ibrahim and Sun from Hohai University, Changzhou, China, Nofal from iRoC Technologies, Grenoble, France, Cai and Guo from China Institute of Atomic Energy, Beijing, China, Shen from Beijing Institute of Spacecraft Environment Engineering, Beijing, China, and Chen from University of Saskatchewan, Saskatoon, Canada.

The second *Letter* compares the performance of a gate-all-around (GAA) transistor against a finFET. The authors, Taghipour and Asli from University of Guilan, Rasht, Iran, report that GAA devices have lower power consumption and they age slower.