Journal of Electronic Testing (2018) 34:507–508
https://doi.org/10.1007/s10836-018-5754-5

Editorial

Vishwani D. Agrawal [1]

Received: 16 September 2018 / Accepted: 16 September 2018 / Published online: 22 September 2018

This issue presents articles on acceleration technique for test pattern generation, analog circuit diagnosis, electromagnetic compatibility (EMC), memory test, hardware security, temporal degradation of hardware, and approximate computing. There are eight papers including one *letter*.

Automatic test pattern generation (ATPG) is a complex problem that demands practically limitless computing resources. Present day massive computing platforms with many simple graphics processing units (GPU) require new algorithms. The first paper describes recent research on a new ATPG algorithm using Boolean satisfiability (SAT) and its implementation on a parallel computing system. Authors are Osama, Gaber, Hussein and Mahmoud from Minia University, Minia, Egypt. Hussein also has an affiliation with Effat University, Jeddah, Saudi Arabia.

The second article relates to the operation of safety critical systems. Online fault diagnosis becomes complex because the actual operating conditions often differ from those under which tests are derived. In this work, the solution of an optimization problem leads to fault identification. Contributors are S. Zhang, Wang, Liu, X. Zhang and Yang from National University of Defense Technology, Changsha, China.

The third article addresses the effects of electromagnetic pulse (EMP) radiation on circuits. This has been recognized a hazard for electronic devices for a long time. EMP effects have become significant for nanometer technologies due to their increased sensitivity to radiation. Authors are Chepelev, Parfenov, Radasky, Titov and Zdoukhov from Russian Academy of Sciences, Moscow, Russia, and Li, Chen, Kong and Xie from Xi'an Jiaotong University, Xi'an, China. They identify a set of key parameters of EMP that determine its influence on specific electronic devices and implemented functions.

Next, Lu and Zhong of National Taiwan University of Science and Technology, Taipei, Taiwan and Hashizume of Tokushima University, Tokushima, Japan present a method for enhancing the yield of NAND flash memories. Their adaptive hardware allows remapping of addresses based on the physical locations of faulty cells so that faults evenly distribute in a logical sense. This enhances the effectiveness of the existing error correction scheme.

Then, we have two papers on hardware security. Karimi from University of Maryland Baltimore County, Baltimore, Maryland, USA, and Danger and Guilley from Telecom ParisTech, Paris, France study effects of aging on a physically unclonable function (PUF). They examine arbiter and loop PUFs where delay is the relevant quantity. An aging-resilient arbiter circuit is also given.

The second paper on security focuses on guarding against a side-channel attacker who monitors the power consumption to gain sensitive information about the system. An on-chip voltage regulator is proposed as a power-PUF. Contributors are Yu and Wen from Old Dominion University, Virginia, USA, Köse from University of South Florida, Tampa, Florida, USA, and Chen from University of Minnesota - Twin Cities, Minneapolis, Minnesota, USA. The authors originally presented this work at the 27th IEEE North Atlantic Test Workshop (NATW) in May 2018 and then submitted to JETTA upon a recommendation from the workshop.

The seventh paper in this issue is authored by Qing, Zeng, Li, Zhang, Sun, and Shi from East China Normal University, Shanghai, China. They present a model for analyzing the age-related degradation in semiconductor devices due to negative bias temperature instability (NBTI). The paper especially examines the H_2 locking and electron fast capture/emission effects.

The final article, a *JETTA Letter*, resorts to the use of significance probability to implement an approximate multiplier

✉ Vishwani D. Agrawal
agrawvd@auburn.edu

[1] Auburn University, Auburn, AL 36849, USA

circuit. By slightly giving up on accuracy, the technique gains on reducing area, power and delay. The contributors are Jothin from KGiSL Institute of Technology, Coimbatore, India and Vasanthanayaki from Government College of Technology, Coimbatore, India.

As this issue nears completion, we will be preparing for our annual meeting of the Editorial Board. After almost a long deliberation, we are close to selecting a 2017 JETTA/TTTC Best Paper Award winner. Look for these details in my upcoming editorials.