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RETRACTED ARTICLE

RETRACTED ARTICLE: Hybrid Cascode Miller Compensation with Bandwidth Extension for 28-nm CMOS Multistage Amplifiers Driving Large Capacitive Loads

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The authors have retracted this article [1]. After constructing the amplifier circuit as proposed in this article, it became apparent that the capacitance range of the capacitor CL is much smaller than the simulation data in the article. Subsequent analysis revealed that there were errors in the theoretical analysis: the proposed circuit is incomplete and flawed in design and implementation. The data in this article are therefore unreliable. [All authors agree with this retraction.]

References

1. C. Zhang, Z. Yan, M. Wang, Hybrid Cascode Miller Compensation with Bandwidth Extension for 28-nm CMOS Multistage Amplifiers Driving Large Capacitive Loads. Circuits Syst. Signal Process (2019). https://doi.org/10.1007/s00034-019-01202-1

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