ParaPhrase Workshop 2012

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Foreword

ParaPhrase (*Parallel Patterns for Adaptive Heterogeneous Multicore Systems*) is a three year FP7 EU funded project that started in October 2011[1]. The project aims to develop and deploy new high-level design patterns for parallel applications that support alternative parallel implementations that can be initially mapped and subsequently dynamically re-mapped to the available *heterogeneous* (CPU+GPU) hardware. The ParaPhrase approach leverages a two-level (or ultimately multi-level) model of parallelism, where the implementations of parallel programs are expressed in terms of interacting components, and where components from different applications are collectively mapped to the available system resources. By expressing parallelism in terms of high-level parallel patterns that have alternative parallel implementations, ParaPhrase tools are able to redeploy/refactor parallel components to match the available hardware resources. *Refactoring* (programmer-directed source code transformation) is assumed to take place within ParaPhrase both at an application level and at a complete systems level, involving multiple parallel workflows running on a heterogeneous collection of CPU/GPU execution units. Moreover, by using a strong component basis for parallelism, ParaPhrase tools are expected to achieve potentially significant gains in terms of enhancing sharing at a high level of abstraction, and so in reducing or even eliminating the costs that are usually associated with cache management, locking, and synchronization.

ParaPhrase organized the 2012 ParaPhrase workshop, co-located with Euro-Par in Rhodes Island, Greece, as its second open ParaPhrase workshop, following on from the successful HPLGPU 2012 on High-Level Programming for Heterogeneous and Hierarchical Parallel Systems (January 2012, co-located with HiPEAC, Paris).

The 2012 ParaPhrase workshop aimed to bring together researchers working on the various research issues covered by ParaPhrase and to discuss achievements, open research problems and perspectives in the area. Topics of interest included: Advanced parallel programming models, Methods for targeting Heterogeneous parallel architectures, Refactoring techniques for parallelism, Algorithmic skeletons, Parallel design patterns, Parallelism in functional programming

[1] `http://www.paraphrase-ict.eu`

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languages, Formal tools for parallel programming, Efficient mechanisms supporting multi-/many-core programming, Deployment and configuration tools for parallel heterogeneous architectures.

In addition to unrefereed project-specific talks, including a general overview by the project coordinator (Kevin Hammond, St Andrews University), the ParaPhrase workshop included the two refereed papers which are published here. The first, *Using the SkelCL Library for High-Level GPU Programming of 2D Applications* by M. Steuwer, S. Gorlatch, M. Buß, and S. Breuer discusses the implementation of particular applications using the algorithmic skeleton library SkelCL, offering pre-implemented recurring computation and communication patterns (skeletons) which greatly simplify programming for single- and multi-GPU systems. The second, *Structured data access annotations for massively parallel computations* by M. Aldinucci, S. Campa, P. Kilpatrick and M. Torquati, introduces a methodology aimed at supporting the joint exploitation of control (stream) and data parallelism in algorithmic skeleton based parallel programming environments. Both of these papers focus on research topics that are central to ParaPhrase research activities. Overall, the workshop ran smoothly, with a good number of attendees and plenty of discussion. We are grateful to the Euro-Par organizing team for their ongoing support, publicity, and excellent choice of location, as well as to the contributing authors, who helped to make this early workshop a success.

We are just at the start of a new period of increasing architectural heterogeneity. The ParaPhrase approach offers a way of abstracting/virtualising this heterogeneity so that much of the complexity can be managed at design/implementation time, and so that parallel applications are resilient to future architectural changes. We look forward to an exciting period of research dealing with the challenges that will arise from this exciting new research area.