Efficient Multi-rate Hybrid Continuous-Time/Discrete-Time Cascade 2-2 Sigma-Delta Modulators for Wideband Telecom

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Abstract. This chapter discusses the use of hybrid continuous-time /discrete-time fourth-order cascade two-stage 2-2 $\Sigma\Delta$ modulators for wideband low-power wireless applications. The modulator architecture under study is based on a new concept of multi-rate operation, in which the front-end stage – implemented using continuous-time (Gm-C) integrators – operates at a higher rate than the back-end (switched-capacitor) stage. This strategy benefits from the faster operation of continuous-time circuits while keeping power efficiency and high robustness against circuit element tolerances. A comparison with conventional multi-rate and single-rate (continuous-time) $\Sigma\Delta$ modulators is carried out based on the impact of main circuit-level error mechanisms, namely: mismatch, finite OTA dc gain and finite gain-bandwidth product. Closed-form analytical expressions are derived for the nonideal in-band noise power of the different architectures under study, demonstrating a good agreement with simulations and showing the benefits of the presented approach. Simulation results show that the proposed modulator is able to operate with a maximum sampling rate of up to 1GHz, digitizing signals with a 44-to-92dB peak signal-to-(noise+distortion) ratio within a programmable 5-to-60MHz bandwidth.

Keywords: Analog-to-digital conversion, multi-rate sigma-delta modulators, continuous-time and discrete-time circuits.

1 Introduction

In the last decade the number of wireless applications and operation modes have increased significantly, demanding higher and higher data rates in hand-held mobile devices. The efficient implementation of these multi-standard devices requires using power-efficient wideband Analog-to-Digital Converters (ADCs).

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Among other ADC techniques, Sigma-Delta Modulators (ΣΔMs) implemented with Continuous-Time (CT) circuits have demonstrated to be a suited solution in these applications. Compared with Discrete-Time (DT) ΣΔMs – mostly implemented with Switched-Capacitor (SC) circuits – CT-ΣΔMs achieve faster rates with less power consumption. However, CT-ΣΔMs are more sensitive than DT-ΣΔMs to some circuit nonideal effects, mainly: clock jitter error and circuit element tolerances [1].

The mentioned limitations of CT-ΣΔMs has motivated exploring other alternative ΣΔM strategies like the so-called Hybrid CT/DT ΣΔMs (H-ΣΔMs). In these hybrid topologies some parts of the modulator – usually the front-end blocks – are implemented with CT circuits, thus benefiting from their faster operation, embedded anti-aliasing filtering and reduced power dissipation, while keeping a higher robustness against circuit errors than in pure CT-ΣΔMs [2–6].

The main drawback of H-ΣΔMs is that their sampling rate is indeed limited by the DT part of the system. For that reason, reported H-ΣΔM Integrated Circuits (ICs) did not really exploit the speed advantages of using CT circuits. A possible solution to palliate this limitation might be using a different sampling frequency for each part (either CT or DT) of the H-ΣΔM, i.e. using a *multi-rate* system [7]. This approach has been applied to both DT- [8] and CT-ΣΔMs [9]. However, in both cases, the strategy was based on using a lower OverSampling Ratio (OSR) in the front-end parts of the modulator – where most of the power is consumed – and a higher OSR in the subsequent stages or blocks – where the dynamic requirements can be relaxed. The same idea has been also applied to cascade H-ΣΔMs, by using double-sampling technique in order to implement the DT back-end stage of the modulator more efficiently [10].

In spite of their potential benefits, *conventional* Multi-Rate (MR) H-ΣΔMs are not feasible in practice when digitizing wideband signals, for instance in the order of 10-100 MHz. In these applications, the back-end SC stages of the modulator need to operate at unfeasible sampling rates (in the order of GHz) in order to achieve low-medium effective resolutions (8-10 bits). These specifications demand for prohibitive values of the Gain BandWidth (GBW) product required for the operational amplifiers [11]. These problems can be alleviated if the signal is *downsampled* across the cascade modulator, so that the CT front-end stage operates at a higher clock rate than the DT back-end stage. This way, the dynamic requirements of the corresponding SC integrators can be relaxed and the resulting effective resolution can be improved by properly combining the different OSRs in a multi-rate operation [12].

This chapter contributes to this topic and presents the high-level design of a multi-rate fourth-order cascade 2-2 H-ΣΔM, in which the CT (Gm-C) front-end stage uses a higher OSR than the SC back-end stage. The aliasing error derived from the downsampling operation can be attenuated in the digital domain so that no extra analog circuits are required as compared to conventional cascade ΣΔMs. Simulation results including all circuit-level error mechanisms show a correct operation of the circuit, demonstrating the feasibility of the presented architectures for the implementation of wideband ADCs in wireless telecom systems.

The chapter is organized as follows. Section 2 overviews the basic principles underlying the operation of multi-rate cascade H-ΣΔMs, considering both the conventional *upsampling* approach and the proposed *downsampling* approach. The effect of circuit nonidealities is analyzed in detail in Section 3, where closed-form expressions for the IBN degraded by several error mechanisms is obtained for all the architectures under study. As an application and case study, the presented analysis is applied to the systematic high-level synthesis of a fourth-order cascade GmC/SC H-ΣΔM, described in Section 4. Finally, simulation results are presented in Section 5 to demonstrate the potentiality of the presented approach.

2 ΣΔ Modulator Architectures under Study

Fig. 1 shows the block diagram of the ΣΔMs under study, where $H(s) = 1/s$ and $H(z) = z^{-1}/(1 - z^{-1})$, denote the transfer functions of the CT and DT integrators, respectively. The same loop filter topology is used in all cases, consisting on a fourth-order cascade 2-stage (2-2) architecture, where the front-end stage includes feed-forward paths to implement a Unity Signal Transfer Function (USTF). Embedded multi-bit quantization is considered in both stages of the modulators. The circuit technique used to implement each stage, either CT or DT, as well as their corresponding sampling frequencies, f_{si}, are highlighted in the figure.

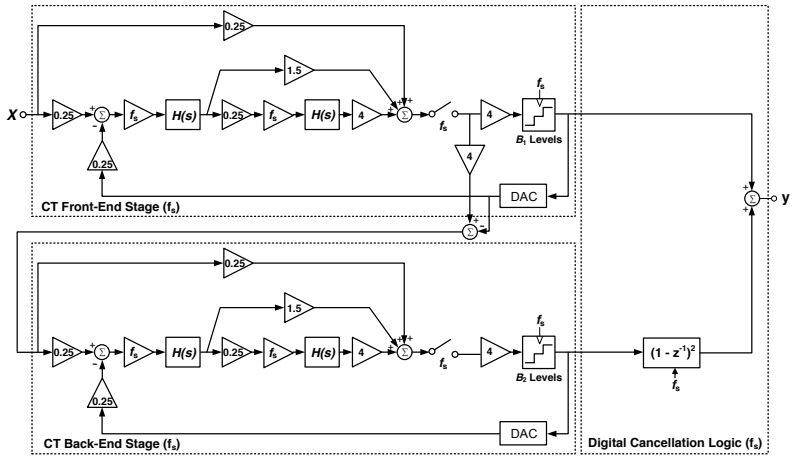
Three different topologies are considered attending to the sampling rate of each stage and its circuit nature, either CT or DT. Thus, Fig. 1(a) is a Single-Rate (SR) CT-ΣΔM, where both stages operate at the same sampling frequency, f_s. Fig. 1(b) is a conventional UpSampling (US) MR H-ΣΔM, where the back-end stage operates at a higher sampling frequency than the front-end stage, i.e. $f_{s2} = r \cdot f_{s1}$, where $r > 1$ denotes the *upsampling ratio*. The opposite operation is carried out in Fig. 1(c), which corresponds to a DownSampling (DS) MR H-ΣΔM, in which the front-end stage operates at the highest sampling rate, i.e. $f_{s1} = p \cdot f_{s2}$, with $p > 1$ being the *downsampling ratio*.

2.1 Quantization Noise Transfer Function

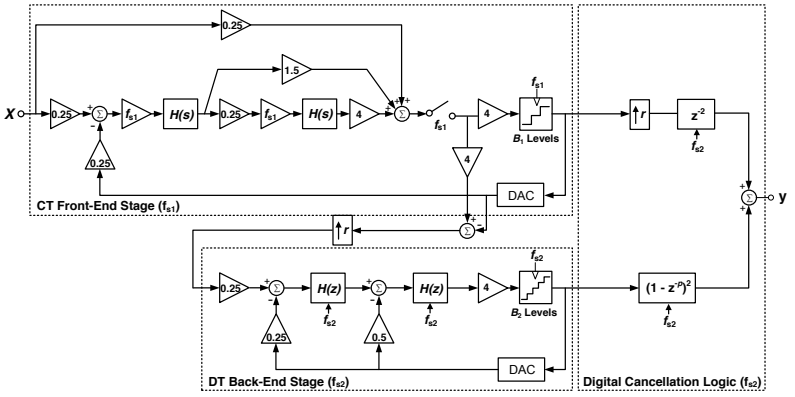
The analysis of the modulators in Fig. 1 can be carried out in the Z-domain by applying a CT-to-DT transformation to the CT stages. The resulting DT-ΣΔMs are equivalent to the original architectures. This CT-to-DT equivalence can be guaranteed because of the DT nature of the (open) loop transfer function from the quantizer output to the sampled quantizer input [1, 13]. Thus, assuming a linear model for the quantizers in Fig. 1(a)-(b), it can be shown that the quantization Noise Transfer Function (NTF) at the output of both modulators are respectively given by:

$$\mathrm{NTF}_{\mathrm{SR}}(z) = (1 - z^{-1})^{(L_1+L_2)} \tag{1}$$

$$\mathrm{NTF}_{\mathrm{US}}(z) = (1 - z^{-r})^{L_1}(1 - z^{-1})^{L_2} \tag{2}$$



(a)



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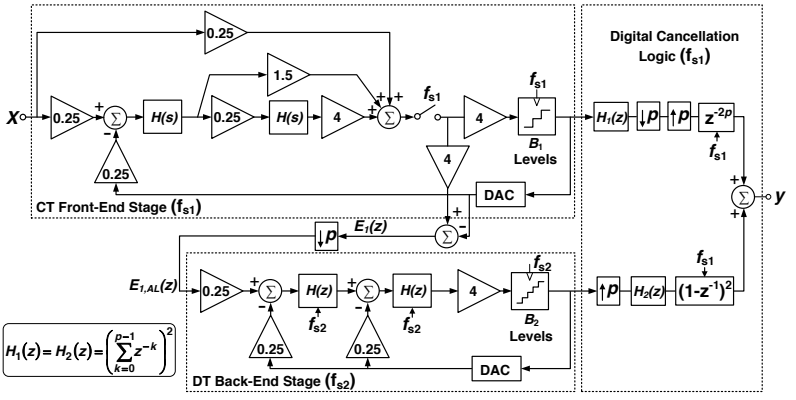


(c)

Fig. 1. Block diagram of the cascade 2-2 ΣΔMs under study: (a) SR CT-ΣΔM, (b) US MR H-ΣΔM, (c) DS MR-ΣΔM

where $L_1 = 2$ and $L_2 = 2$ stand for the order of the front-end and the back-end stages of the modulators, respectively.

In contrast to the conventional US MR H-ΣΔM of Fig. 1(b), the back-end (DT) stage of the DS MR H-ΣΔM shown in Fig. 1(c) operates at a lower rate than the front-end (CT) stage, i.e $f_{s2} < f_{s1}$. Therefore, the quantization error signal, $E_1(z)$, that is fed to the back-end stage, is *downsampled*, thus containing aliased components at multiples of f_{s2}. This can be expressed in the Z-domain as [12]:

$$E_{1,\mathrm{AL}}(z) = \frac{1}{p}\sum_{k=0}^{p-1} E_1(z^{1/p}e^{j(2\pi k/p)}) \tag{3}$$

Note that $E_{1,\mathrm{AL}}(z)$ is indeed an error signal, that contains the quantization error, $E_1(z)$, and its aliased components. Therefore, $E_{1,\mathrm{AL}}(z)$ can be also cancelled out by the Digital Cancellation Logic (DCL) transfer functions. To this purpose, the digital functions $H_1(z)$ and $H_2(z)$ in Fig. 1(c) are used. These functions must be reconfigurable and programmable according to the value of p.

Assuming a linear model for the quantizers in Fig. 1(c), it can be shown that both $E_1(z)$ and its aliased error components can be completely cancelled out if $H_1(z)$ and $H_2(z)$ are given by the following expression:

$$H_1(z) = H_2(z) = \left(\sum_{k=0}^{p-1} z^{-k}\right)^{L_1} \tag{4}$$

Taking into account the above expression, it can be shown that the NTF of Fig. 1(c) can be written as:

$$\mathrm{NTF}_{\mathrm{DS}}(z) = (1 - z^{-1})^{L_1}(1 - z^{-p})^{L_2} \tag{5}$$

As an illustration, Fig. 2 shows the output spectra of the modulators in Fig. 1 for different cases of r and p, showing the variation of the notch frequency caused by the multi-rate operation.

2.2 In-Band Quantization Noise Power

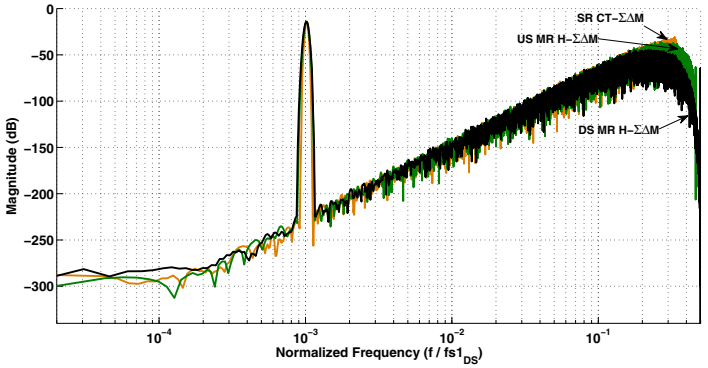
Integrating the expressions (1), (2) and (5) within the signal bandwidth, B_w, it can be shown that the In-Band Noise (IBN) power at the output of the modulators in Fig. 1(a)-(c) are respectively given by [1, 12]:

$$\mathrm{IBN}_{\mathrm{SR}}^{\mathrm{ideal}} \simeq \frac{\Delta^2\pi^{2L}}{12(2L+1)\mathrm{OSR}^{2L+1}} \tag{6}$$

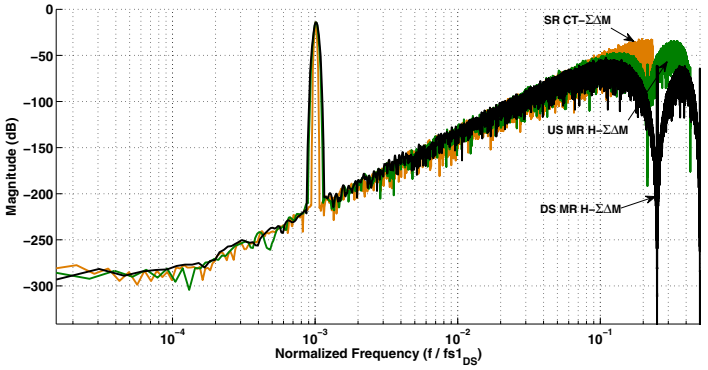
$$\mathrm{IBN}_{\mathrm{US}}^{\mathrm{ideal}} \simeq \frac{\Delta^2\pi^{2L}r^{2L_1}}{12(2L+1)\mathrm{OSR}_{2_{\mathrm{US}}}^{2L+1}} \tag{7}$$

$$\mathrm{IBN}_{\mathrm{DS}}^{\mathrm{ideal}} \simeq \frac{\Delta^2 \pi^{2L} p^{2L_2}}{12(2L+1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{2L+1}} \tag{8}$$

where Δ stands for the quantization step of the last quantizer; $L \equiv L_1 + L_2 = 4$ is the loop-filter order of the ΣΔMs in Fig. 1; $\mathrm{OSR}_{\mathrm{SR}} \equiv f_s/(2B_w)$ is the OSR of the SR CT-ΣΔM [Fig. 1(a)], and $\mathrm{OSR}_{2_{\mathrm{US}}} \equiv f_{s2}/(2B_w)$ and $\mathrm{OSR}_{1_{\mathrm{DS}}} \equiv f_{s1}/(2B_w)$ denote the value of the largest OSR in the US MR H-ΣΔM [Fig. 1(b)] and DS MR H-ΣΔM [Fig. 1(c)], respectively. It can be noted that the expressions in (7) and (8) reduce to the one obtained by conventional *single-rate* (SR) ΣΔMs, shown in (6), provided that $r = p = 1$ and $\mathrm{OSR}_{2_{\mathrm{US}}} = \mathrm{OSR}_{1_{\mathrm{DS}}} = \mathrm{OSR}_{\mathrm{SR}}$, where $\mathrm{OSR}_{\mathrm{SR}}$ denotes the OSR of the SR modulator. Note also that the same ideal IBN can be achieved by all ΣΔMs in Fig. 1, by properly choosing the values of r, p, $\mathrm{OSR}_{\mathrm{SR}}$, $\mathrm{OSR}_{2_{\mathrm{US}}}$ and $\mathrm{OSR}_{1_{\mathrm{DS}}}$.



(a)



(b)

Fig. 2. Output spectra of the ΣΔMs under study for: (a) $r = p = 2$, (b) $r = p = 4$

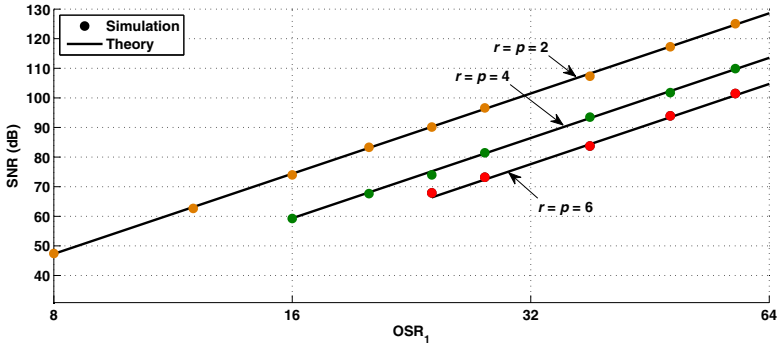


Fig. 3. SNR vs. $\mathrm{OSR}_{1_{\mathrm{DS}}}$ for different values of r and p

As an illustration, Fig. 3 depicts the Signal-to-Noise Ratio (SNR) versus $\mathrm{OSR}_{1_{\mathrm{DS}}}$ for different values of r and p, showing a good agreement between theory and simulations within a wide resolution range.

3 Performance Degradation Due to Circuit Errors

The analysis described in previous section assumed that the ΣΔMs in Fig. 1 were implemented with ideal building blocks. However, in practice, the noise shaping (and consequently the effective resolution) of these modulators is degraded by the action of circuit-level errors. This section analyses the IBN degradation caused by three of the most critical nonideal effects, namely: mismatch error, finite dc gain of the finite Operational Transconductance Amplifier (OTA) and Gain-BandWidth (GBW) product. To this end, it will be assumed that the DT and CT integrators in ΣΔMs in Fig. 1 are implemented by Forward-Euler (FE) Switched-Capacitor (SC) integrators and Gm-C integrators, respectively.

3.1 Integrators' Weight Error

Let us assume that the integrators in Fig. 1 have a weight error caused by technology process variations. In the case of SC FE integrators, this gain error, denoted as ϵ_{DT}, is caused by the capacitor mismatch and it is modeled as a random deviation of the integrator's weight, i.e. the ratio between the sampling capacitor and the integrator capacitor [14]. In the case of Gm-C integrators, the weight error, ϵ_{CT}, is due to random variations of the time constant, i.e. the transconductance-capacitor product [1].

Considering the effect of ϵ_{DT} and ϵ_{CT} the integrator transfer functions in Fig. 1, $H(z)$ and $H(s)$, become degraded by the action of errors ϵ_{DT} and ϵ_{CT}, respectively [1, 14]. The effect of this error can be propagated through the modulator in order to obtain the nonideal NTF and IBN. Following this systematic

procedure, it can be shown that the IBN power at the output of the ΣΔMs in Fig. 1(a)-(c) can be respectively approximated by:

$$\mathrm{IBN}_{\mathrm{SR}}^{\mathrm{mis}} \simeq (1+\epsilon_{\mathrm{CT}})^2 \cdot \mathrm{IBN}_{\mathrm{SR}}^{\mathrm{ideal}} + \frac{\Delta_1^2 \pi^{2L_1} \epsilon_{\mathrm{CT1}}^2}{12(2L_1+1)\mathrm{OSR}_{\mathrm{SR}}^{2L_1+1}} \tag{9}$$

$$\mathrm{IBN}_{\mathrm{US}}^{\mathrm{mis}} \simeq (1+\epsilon_{\mathrm{DT}})^2 \cdot \mathrm{IBN}_{\mathrm{US}}^{\mathrm{ideal}} + \frac{\Delta_1^2 \pi^{2L_1} \epsilon_{\mathrm{CT1}}^2 r^{2L_1+1}}{12(2L_1+1)\mathrm{OSR}_{2_{\mathrm{US}}}^{2L_1+1}} \tag{10}$$

$$\begin{aligned}\mathrm{IBN}_{\mathrm{DS}}^{\mathrm{mis}} &\simeq (1+\epsilon_{\mathrm{DT}})^2 \cdot \mathrm{IBN}_{\mathrm{DS}}^{\mathrm{ideal}} + \\ &+ \frac{\Delta_1^2 \pi^{2L_1}}{12(2L_1+1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{2L_1+1}} \cdot \sum_{k=0}^{p-1} \left| \alpha(k)\epsilon_{\mathrm{CT11}} + \frac{\beta(k)}{2}\epsilon_{\mathrm{CT12}} \right|^2 \end{aligned} \tag{11}$$

where Δ_1 stands for the quantization step of the front-end quantizer in Fig. 1; $\epsilon_{\mathrm{CT}ij}$ denote the weight error of the j-th Gm-C integrator in the i-th stage $(i, j = 1, 2)$; and $\alpha(k)$ and $\beta(k)$ are respectively given by:

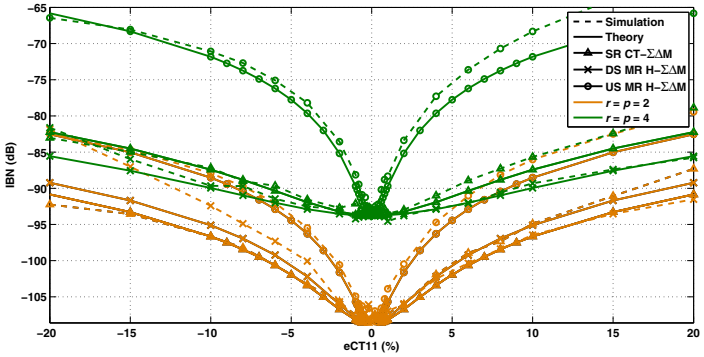
$$\begin{aligned}\alpha(k) &= (2e^{-j2\pi k/p} - e^{-j4\pi k/p}) \\ \beta(k) &= (e^{-j2\pi k/p} + e^{-j4\pi k/p})\end{aligned} \tag{12}$$

In order to verify the theoretical expressions given in (9)-(11), the ΣΔMs under study were simulated using SIMSIDES – a time-domain behavioral simulator for $\Sigma\Delta$Ms [15]. To make a fair comparison, the same ideal conditions, i.e. $r = p$ were assumed, and the values of the OSR for each modulator were computed from (6), (7) and (8), so that the same ideal IBN is achieved in all cases. The same embedded quantizers were used in all ΣΔMs, considering 4-bit quantization in both stages. Two values of signal bandwidths were simulated, $B_w = 20, 40$ and a 1-MHz input tone with amplitude −7dB below quantization full-scale range was applied in all cases. For the sake of simplicity, only the effect of errors associated to the front-end (CT) integrators – which are common in both ΣΔM architectures in Fig. 1 – have been taken into account in the simulations.

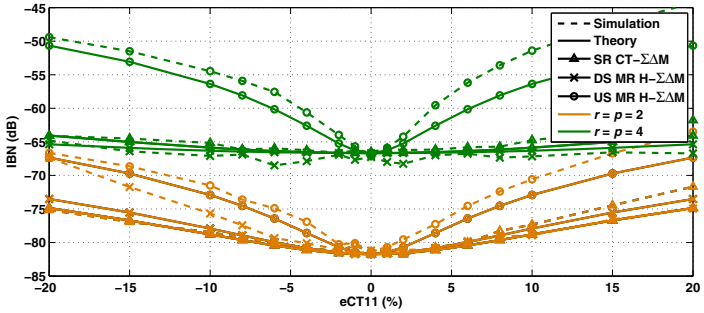
Fig. 4 shows the effect of circuit element tolerances in the time constant of the front-end Gm-C integrator. It can be noted how both theoretical calculations and simulations demonstrate that the DS MR H-ΣΔM achieves the largest robustness against mismatches, getting better as both p and B_w increase.

3.2 Finite OTA dc Gain Error

Let us consider now that the integrators in Fig. 1 have a finite OTA dc gain. This effect can be modeled as a finite dc gain of the opamp in SC integrators [14] and as a finite output resistance of the transconductor circuit in Gm-C [1]. Thus, taking into account this effect on the integrators' transfer functions, it can be demonstrated that the IBN at the output of the modulators in Fig. 1(a)-(c) are respectively given by:



(a)



(b)

Fig. 4. IBN vs. integrator's weight error for: (a) B_w=20MHz and (b) B_w=40MHz

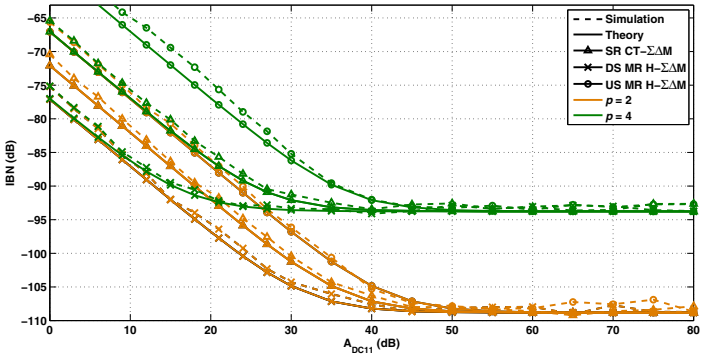
$$\mathrm{IBN}_{\mathrm{SR}}^{\mathrm{gain}} \simeq \left[1+\frac{2L+1}{2L-1}\cdot\left(\frac{\mu_2\cdot \mathrm{OSR}_{\mathrm{SR}}}{\pi}\right)^2\right]\cdot \mathrm{IBN}_{\mathrm{SR}}^{\mathrm{ideal}} + \\ + \frac{\Delta_1^2\pi^{2L_1-2}\mu_1^2}{12\cdot(2L_1-1)\cdot \mathrm{OSR}_{\mathrm{SR}}^{2L_1-1}} \tag{13}$$

$$\mathrm{IBN}_{\mathrm{US}}^{\mathrm{gain}} \simeq \left[1+\frac{2L+1}{2L-1}\cdot\left(\frac{\mu_2\cdot \mathrm{OSR}_{2_{\mathrm{US}}}}{\pi}\right)^2\right]\cdot \mathrm{IBN}_{\mathrm{US}}^{\mathrm{ideal}} + \\ + \frac{\Delta_1^2\pi^{2L_1-2}\mu_1^2 r^{2L_1-1}}{12\cdot(2L_1-1)\cdot \mathrm{OSR}_{2_{\mathrm{US}}}^{2L_1-1}} \tag{14}$$

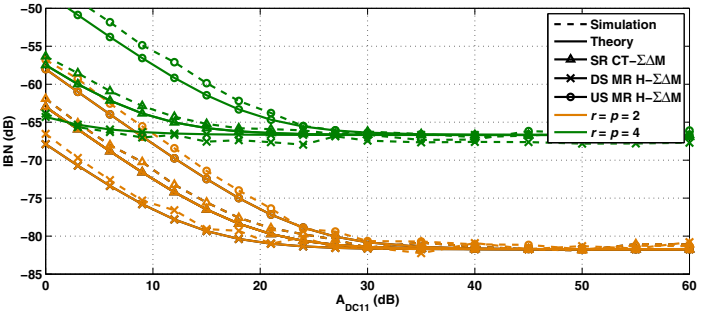
$$\mathrm{IBN}_{\mathrm{DS}}^{\mathrm{gain}} \simeq \left[1+\frac{2L+1}{2L-1}\cdot\left(\frac{\mu_2\cdot \mathrm{OSR}_{1_{\mathrm{DS}}}}{\pi p}\right)^2\right]\cdot \mathrm{IBN}_{\mathrm{DS}}^{\mathrm{ideal}} + \\ + \frac{\Delta_1^2\pi^{2L_1-2}\mu_1^2 p^{2L_1-1}}{12\cdot(2L_1-1)\cdot \mathrm{OSR}_{1_{\mathrm{DS}}}^{2L_1-1}} \tag{15}$$

where $\mu_i \equiv 1/A_{\mathrm{dc}i1} + 1/A_{\mathrm{dc}i2}$ and $A_{\mathrm{dc}ij}$ stand for the finite OTA dc gain of the j-th integrator in the i-th stage of Fig. 1.

As an illustration, Fig. 5 shows the impact of finite dc gain error of the first Gm-C integrator for the ΣΔMs under study. Note that both theoretical predictions and simulation results are in good agreement, showing that the DS MR H-ΣΔM is less sensitive to the impact of this error, regardless the value of r, p and B_w.



(a)



(b)

Fig. 5. IBN vs. finite OTA dc gain for: (a) B_w=20MHz and (b) B_w=40MHz

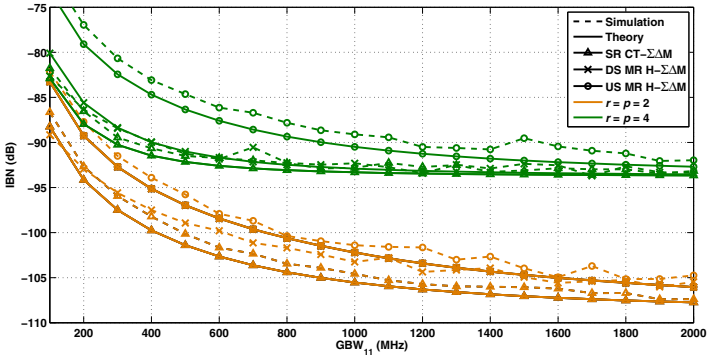
3.3 Finite GBW Error

Following the same procedure as in previous sections, it can be found that the IBN degradation caused by the effect of the integrators GBW can be modeled by replacing the expressions of $\epsilon_{\mathrm{CT}ij}$ and $\epsilon_{\mathrm{DT}ij}$ in (9)-(11) by the following expressions:

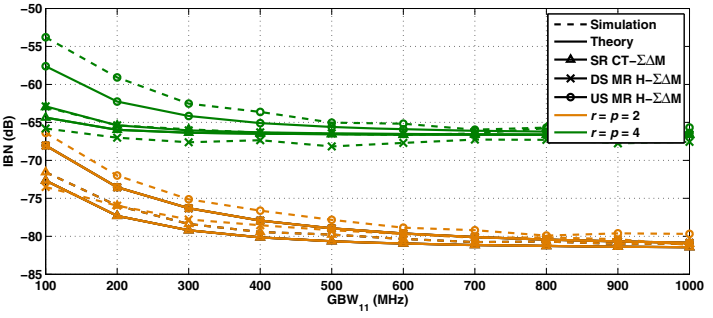
$$\epsilon_{\mathrm{CT}ij} \equiv \frac{f_s}{\mathrm{GBW}_{ij}}; \epsilon_{\mathrm{DT}ij} \equiv e^{\frac{-\pi \mathrm{GBW}_{ij}}{f_s}} \tag{16}$$

where GBW_{ij} is the value of GBW for the j-th integrator in the i-th stage.

The impact of GBW is illustrated in Fig. 6, highlighting a good matching between theory and simulations. A worse performance of the US MR H-ΣΔM is obtained, while a similar degradation is roughly obtained for the DS MR H-ΣΔM and the SR CT-ΣΔM. Indeed, the latter achieves a higher robustness against the impact of GBW in the first integrator.



(a)



(b)

Fig. 6. IBN vs. GBW for: (a) B_w=20MHz and (b) B_w=40MHz

4 Case Study: A Gm-C/SC Cascade 2-2 DS MR H-ΣΔM

As a case study, Fig. 7 shows a conceptual schematic of the modulator in Fig. 1(c). The front-end (CT) stage is realized using Gm-C integrators. All transconductors can be tuned in order to keep the time constants, C/g_m, unchanged over C variations. Table 1 shows the values of nominal loop filter transconductances, g_{mi} (expressed in terms of the unitary transconductance, g_{mu}) as well as the capacitances, C_i, used to realize both Gm-C and SC integrators.

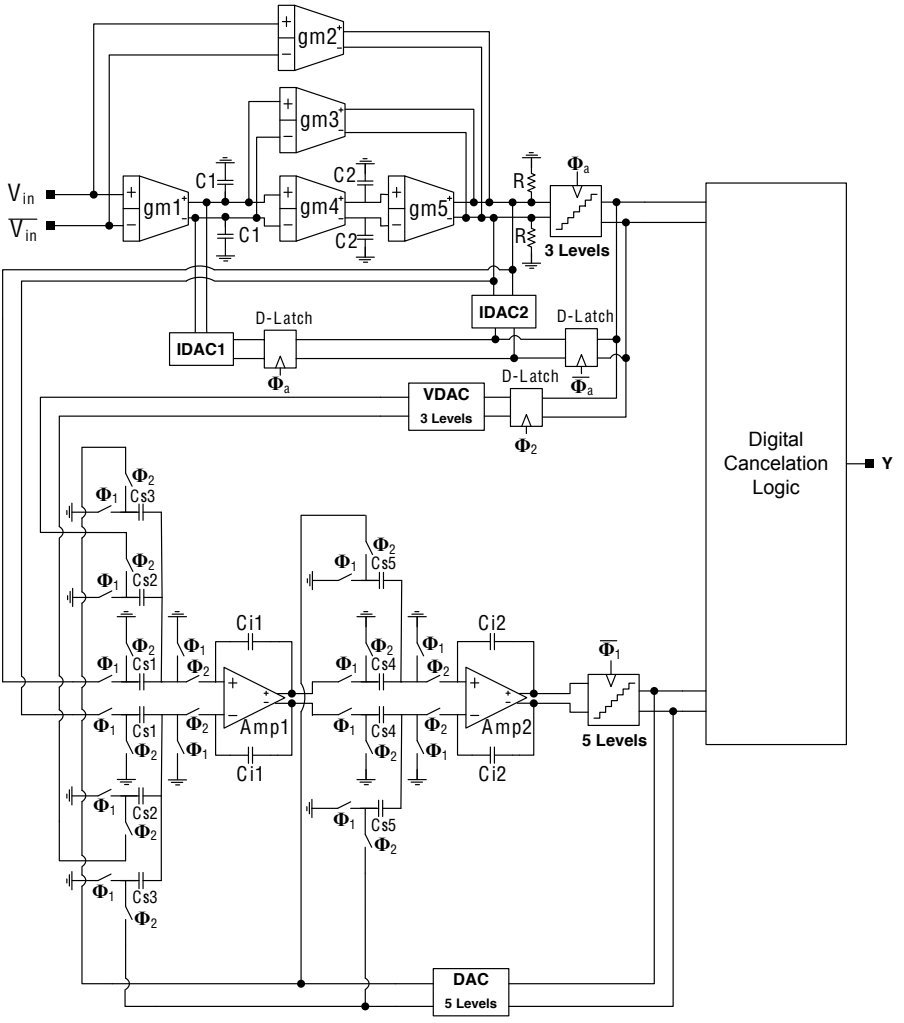


Fig. 7. Conceptual Gm-C/SC schematic of the modulator in Fig. 1(c)

Note that an extra feedback branch between the output and the input of the front-end quantizer and two additional D-latches are included in order to compensate for the excess loop delay [1]. This extra branch forces modifying the loop filter coefficients in order to obtain the ideal NTF given in (5). The back-end (DT) stage – realized with SC circuits – is a conventional second-order topology based on two feedback paths. Both stages include multi-level quantizers – 3-level in the front-end stage and 5-level in the back-end stage – in order to benefit from the extra level provided by fully differential implementation of the embedded flash ADCs.

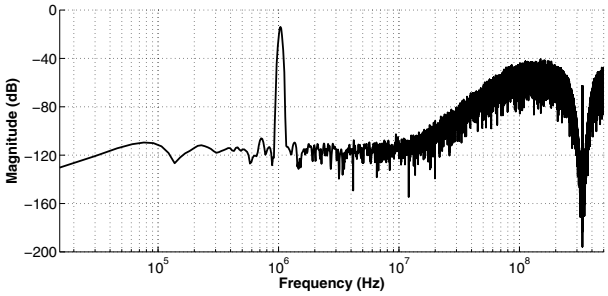
The Full-Scale (FS) reference voltage, V_{FS}, is 1V. Feedback DACs in the CT front-end stage are implemented as current steering Non-Return-to-Zero (NRZ) 3-level DACs (named IDACs in Fig. 7) because of their potential high-speed operation and the convenience to inferface with the Gm-C loop filter. The output currents provided by both IDACs are also shown in Table 1. An additional voltage-mode 3-level DAC, named VDAC in Fig. 7, is required in the inter-stage path. The digital cancellation logic is implemented as described in Section 2.

Fig. 8 shows the output spectra of the modulator in Fig. 7 for different values of p, considering a sampling frequency of the front-end stage of $f_{s1} = 1$GHz and including thermal noise corresponding to $g_{mu} = 75\mu$A/V. Ideally, the modulator is able to digitize signals with B_w from 5MHz to 60MHz and an effective resolution ranging from 9 to 16 bits. According to (8), these specifications can be satisfied for $\text{OSR}_1 \in [8, 128]$ and $p = [2, 3, 4, 5, 6]$. This is illustrated in Fig. 9 that represents IBN vs. B_w (Fig. 9(a)) and IBN vs. OSR_1 (Fig. 9(b)) for different values of p. In this case, three values of f_{s1} are considered, $f_{s1} = 1$GHz, 500MHz and 333MHz. The values of the Gm-C integration capacitors, $C_{1,2}$ are changed according to the expressions shown in Table 1, by using a switchable bank of three unit capacitances of value C_u=1.2pF. The sampling frequency of the SC back-end stage can be reconfigured through a programmable clock-phase generator[1], such that $f_{s2} = f_{s1}/p$. Both clock-phase generators are synthesized and controlled by a single master clock – generated by a digital PLL-based synthesizer whose reference frequency is f_{s1}. This is conceptually depicted in Fig. 10, where clock phases of both CT and SC stages are shown for different values of p.

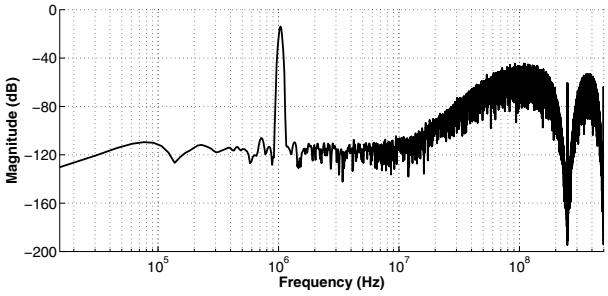
5 Simulation Results

The modulator has been simulated using SIMSIDES [15], considering main circuit error mechanisms. Fig. 11 shows the effect of finite OTA dc gain of front-end integrators, given by $A_{vi} \equiv g_{mi}R_{oi}$, where R_{oi} is the finite output resistance of the i-th Gm-C integrator. Note that $A_{v11,12} > 30$dB is enough to satisfy the required specifications. The effect of finite GBW of the front-end Gm-C integrator is illustrated in Fig. 12, considering f_{s1} =1GHz and different values of B_w and

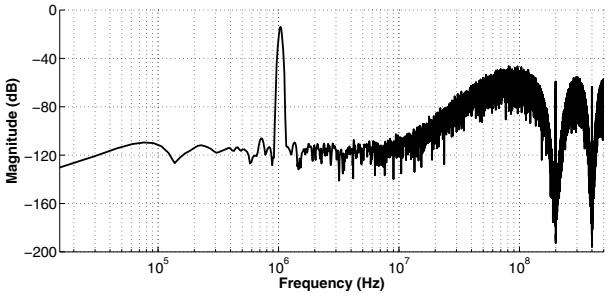
[1] Note that in this modulator, $f_{s1} = p \cdot f_{s2}$.



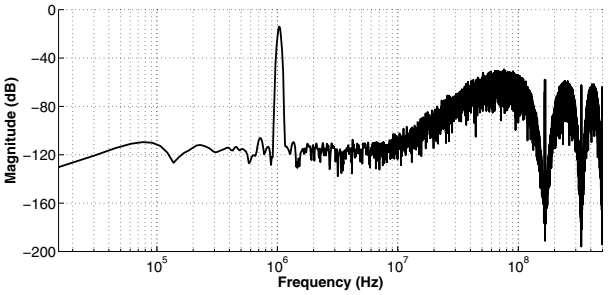
(a)



(b)



(c)

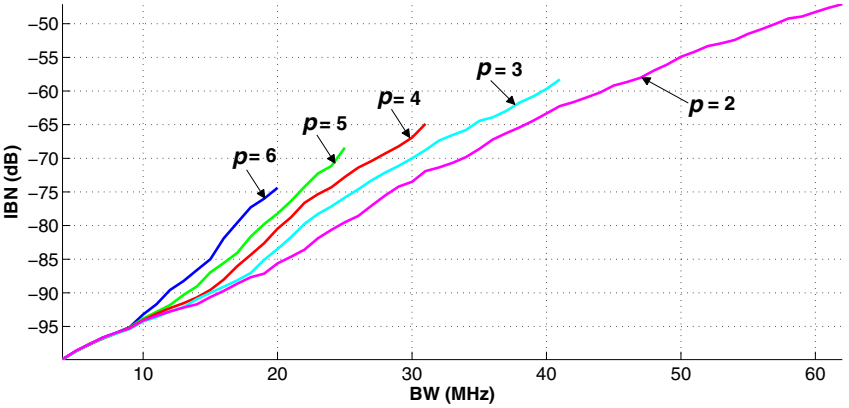


(d)

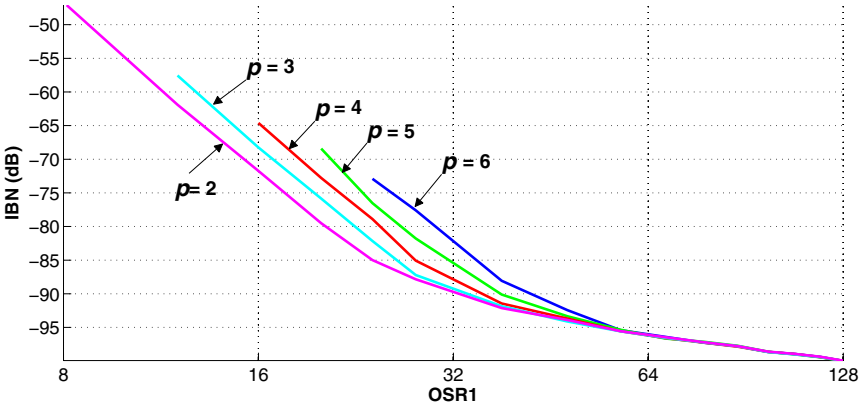
Fig. 8. Output spectra for: (a) $p = 3$, (b) $p = 4$, (c) $p = 5$, (d) $p = 6$

Table 1. Loop filter coefficient implementation of Fig.7

Transconductances	
$g_{m1} = 4g_{mu}$, $g_{m2} = g_{mu}$, $g_{m3} = 10g_{mu}$, $g_{m4} = 4g_{mu}$, $g_{m5} = 16g_{mu}$	
Capacitances	
Gm-C Integ.	$C_1 = g_{m1}/f_{s1}$, $C_2 = g_{m4}/f_{s1}$
SC Integ.	$C_{s1} = C_{s4} = 0.4$pF, $C_{s2} = C_{s3} = 0.1$pF, C_{s5} =0.2pF,$C_{i1} = C_{i2}$=0.4pF
Voltage-to-Current Converters and Feedback DACs	
$R = 1/g_{m1} = 3.3\text{k}\Omega$, $I_{\text{DAC1}} = 4g_{mu}V_{FS}$=300$\mu$A, $I_{\text{DAC2}} = 2g_{mu}V_{FS}$=150$\mu$A	



(a)



(b)

Fig. 9. IBN for different values of p: (a) IBN vs. B_w. (b) IBN vs. OSR_1.

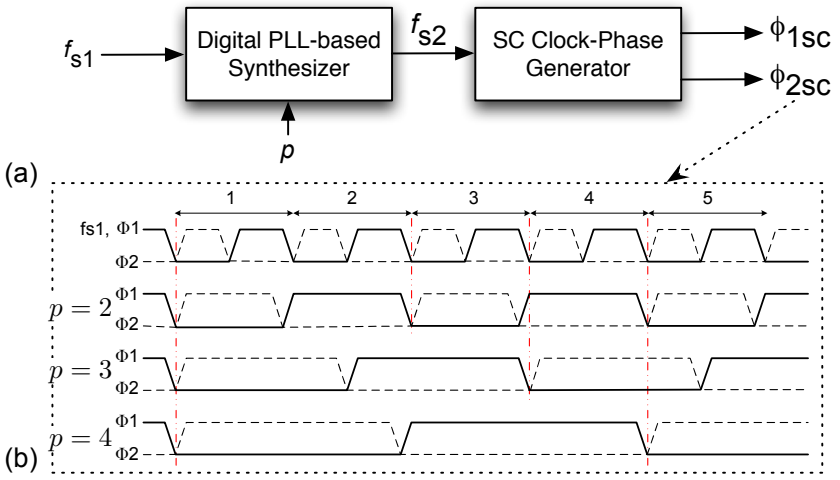


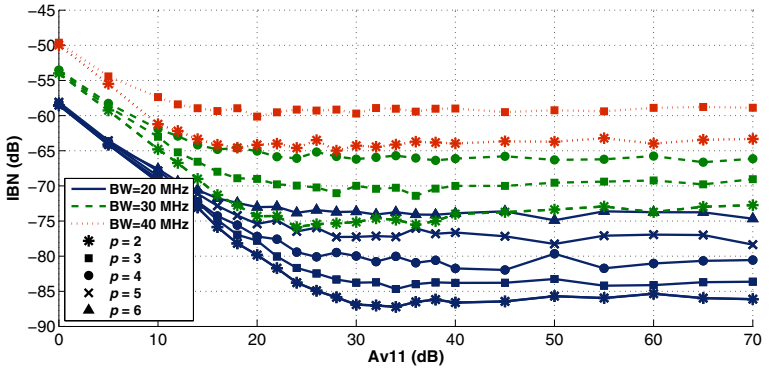
Fig. 10. Clock phase generator. (a) Conceptual block diagram. (b) Clock phases for different values of the multi-rate ratio.

p. It is noted that – depending on the value of p and B_w – the required GBW may vary from 700MHz to 1.5GHz.

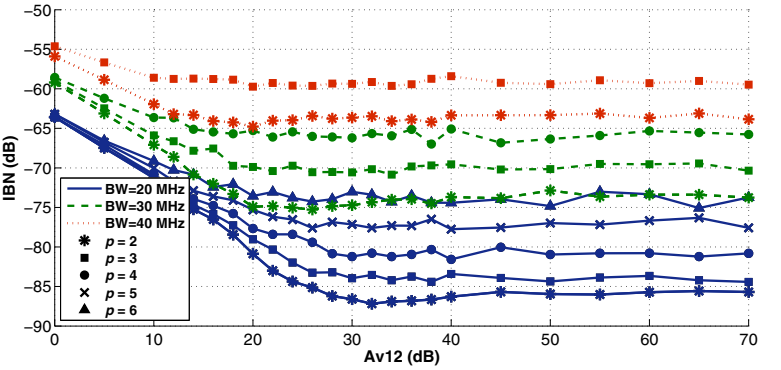
Fig. 13 illustrates the effect of circuit element tolerances in the CT part and capacitor mismatch in the DT part of the modulator, by showing an histogram of IBN for $B_w = 20$MHz and different values of p. In order to evaluate the impact of random circuit errors, a 250-sample Monte Carlo simulation was carried out, considering a standard deviation of 1% in the transconductances and 5% for the capacitors in the CT part of the circuit, while a 0.1% mismatch variation was considered for the SC stage. Note that the effective resolution degradation is similar to the one obtained in conventional cascade ΣΔMs.

Table 2 sums up the modulator performance in terms of the maximum signal bandwidth, B_{wmax}, that can be handled for a given value of p, f_{s1} and the Signal-to-(Noise+Distortion) Ratio ($SNDR$). The table includes also the circuit-level performance metrics required to achieve this modulator performance, including both nonideal and nonlinear effects, such as the input-referred third-order intercept point (IIP3). In the case of SC integrators, folded cascode operational amplifiers were considered and their electrical performance – extracted from transistor-level simulations carried out in Cadence Spectre – are also shown, considering a 1.2-V 90-nm CMOS technology.

The diverse range of specifications covered by the proposed modulator is illustrated in Fig. 14, that represents the $SNDR$ vs. input amplitude for f_{s1} =1GHz and considering different values of B_w and p, taking into account all circuit nonideal and nonlinear effects listed in Table 2. It can be noted that the modulator is able to cover a wide region in the resolution-vs-bandwidth plane.



(a)



(b)

Fig. 11. IBN degradation caused by finite OTA dc gain in (a) 1st and (b) 2nd Gm-C integrators

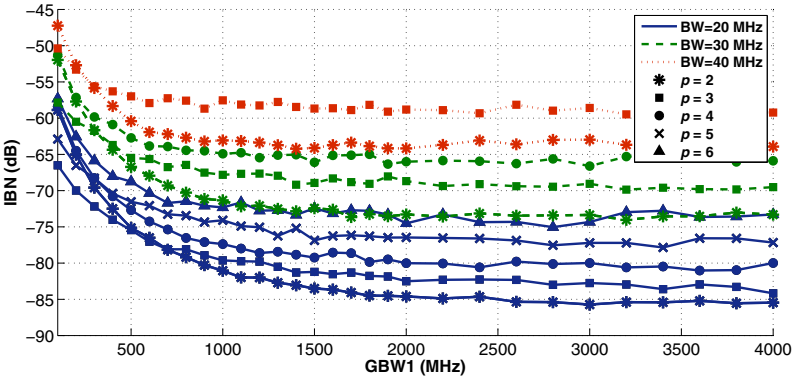


Fig. 12. IBN degradation due to GBW of the front-end Gm-C integrator

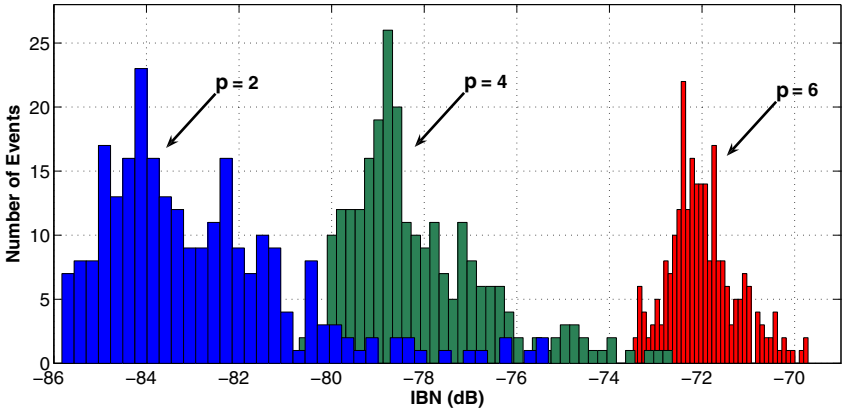


Fig. 13. Monte Carlo simulation for $f_{s1} = 1$GHz and $B_w = 20$MHz

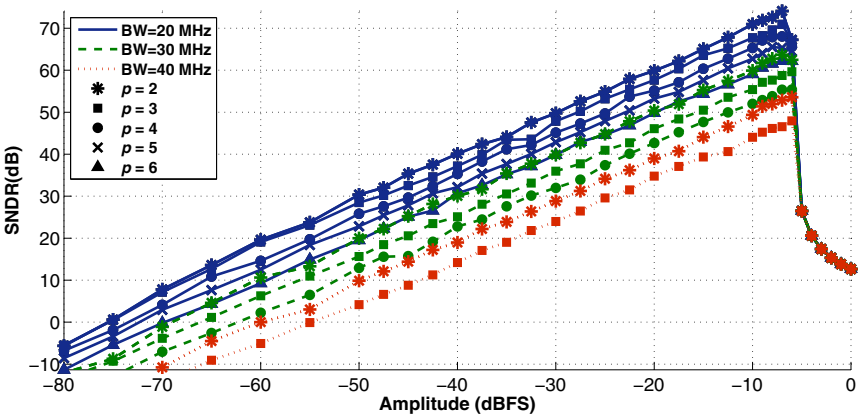


Fig. 14. $SNDR$ vs. amplitude for different values of B_w and p

Table 2. Modulator Performance Summary

Modulator									
p	2		3	4	5	6	(2,6)	2	
f_{s1}	1GHz						500MHz	333MHz	
B_{wmax} (MHz)	60	50	40	30	25	20	5	10	5
$SNDR$ (bits)	7	8.3	8.9	10	10.5	11.5	15	12.5	14.6
Clock Jitter (ps)	8.9	4	3	1.6	1.2	0.7	0.2	0.9	0.3
Front-End Gm-C Integrator									
DC Gain (dB)	20	20	20	25	25	30	40	35	40
GBW (GHz)	0.7	0.8	0.8	1	1.2	1.5	1.5	1.5	1.5
IIP3 (dBV)	10	13	15	18	20	25	35	30	35
Input Swing	500mV								
Output Swing	500mV								
Second Gm-C Integrator and Loop-filter Transconductances									
DC Gain (dB)	20	20	20	25	25	30	40	35	40
GBW (MHz)	200	250	250	300	350	400	500	450	500
IIP3 (dBV)	5	7	7	10	12	15	15	15	15
Input Swing	500mV								
Output Swing	500mV								
SC Integrators (Transistor-Level Performance)									
DC Gain (dB)	47								
g_m (mA/V)	4.4								
Phase Margin	73.4°								
Output Current (μA)	404								
Input Parasitic Cap. (pF)	0.2								
Out. Parasitic Cap. (pF)	0.1								
Output Swing (mV)	700								

6 Conclusion

Different approaches for the implementation of multi-rate cascade hybrid CT/DT $\Sigma\Delta$ modulators have been discussed in this chapter. One of them increases the clock rate across the cascade while the other uses a lower oversampling ratio in the back-end stage. Both multi-rate cascade topologies have been compared to conventional single-rate cascade continuous-time $\Sigma\Delta$ modulators. The effect of main circuit errors has been theoretically analyzed and verified by time-domain simulations, demonstrating that the downsampling multi-rate architecture exploits the capability of continuous-time circuits to operate at higher frequencies with less power consumption, while keeping a higher robustness against circuit errors. These characteristics make these kinds of $\Sigma\Delta$Ms very suited candidates for the implementation of analog-to-digital converters in the next generation software-defined-radio based mobile terminals. As a case study, the high-level design of a multi-rate hybrid Gm-C/SC fourth-order cascade 2-2 $\Sigma\Delta$M has been presented. The simulated performance demonstrates that the circuit can digitize 5-to-60MHz signals with programable effective resolutions ranging from 7 to 15 bits, thus covering a wide region of the resolution-vs-bandwidth plane.

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