A Low-Power Ultra-Fast Capacitor-Less LDO with Advanced Dynamic Push-Pull Techniques

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Abstract. A current-efficient, capacitor-less low-dropout regulator (LDO) with fast-transient response for portable applications is presented in this chapter. It makes use of an adaptive biasing common-gate amplifier to extend loop bandwidth of the LDO at heavy loads greatly. Also, the dynamic push-pull (DPP) slew-rate enhancement (SRE) circuit based on capacitive coupling detects rapid voltage spikes at the output to provide an extra current to charge and discharge the large gate capacitance of the power transistor momentarily. The proposed circuit has been implemented in a 0.35μm standard CMOS process. Experimental results show that it can deliver 100mA load current at 150mV dropout voltage. It only consumes 10μA quiescent current at no-load condition and is able to recover within 0.8μs even under the maximum load current change.

Keywords: adaptive biasing, dynamic push-pull technique, capacitive coupling, slew-rate enhancement, high bandwidth, low-dropout regulator, system-on-chips.

1 Introduction

Various multimedia and portable devices lead the trend of system-on-chip (SoC) integration. The power management is an essential part in the battery-powered system. To get a fast transient response and noise-less output supply voltage, the on-chip capacitor-less LDO is demanded to be integrated with the SoC systems. However, it takes the restriction of minimum load current and slow transient response into design consideration due to the low supply voltage [1]–[4].

Normally, transient response is a critical dynamic specification in LDO design, which is dominated by the loop-gain bandwidth and slew rate at the gate of the power transistor. Both the amplitude of voltage spike and recovery time of regulated output voltage will affect its overall accuracy. Unfortunately, the generic approaches to optimize the transient response using external capacitors and large bias current are no longer useful in the power-saving SoC application. Several techniques are thus proposed to improve the transient responses without increasing quiescent current so much [5]–[9]. An active-frequency compensation circuit is introduced in [5] to greatly boost the effective current multiplication factor by at least one order of magnitude and

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extend the loop bandwidth drastically. A low-power fast-transient low-dropout regulator with multiple small-gain stages is employed in [6] to provide loop gain enhancements without introducing low-frequency poles before the unity-gain frequency, which leads to larger loop gain and bandwidth. An adaptive reference control technique is proposed in [7] by dynamically and smoothly adjusting the reference voltage so as to increase the slew rate of error amplifier (EA). A low-power analog driver based on a single-stage amplifier with an embedded current-detection SRE circuit is presented in [8]. A low-dropout linear regulator topology with replica-biased common-source unity-gain buffer is used in [9] to overcome the bandwidth limitation of the feedback loop.

Recently, non-static biasing has been proved to be an effective way to improve transient responses in low-power design, which enables bias current to be dramatically increased for bandwidth extension and slew-rate improvement. Adaptive biasing (AB), that increases the bias current according to the magnitude of the output current, is employed in [10]–[12]. For example, the buffer stage is adaptively biased as shown in [10], where the increase in current in the buffer stage aids the circuit by pushing the parasitic pole associated with parasitical capacitors at the gate of power transistors to higher frequencies and by increasing the current available for slew-rate conditions; one more choice is used at the input stage in [11] and [12] to simultaneously extend both slewing and bandwidth. Another more current-efficient way is to utilize dynamic biasing technique where more bias current is adopted only at the transient instant when the output current is changed [13]. Based on this idea, the capacitive coupling and dynamic charging method is reported lately, which is very promising in increasing circuitry response speed while keeping static power consumption low. It can be utilized to increase the bias current of error amplifier momentarily [14]–[18] or construct a current-boosting voltage buffer [19] and a differentiator [20] for bandwidth and slew-rate improvement. Slewing detection can be made by either monitoring an internal node or at the output. The important issue here is that when the capacitive coupling circuit is used in a closed loop scheme, since it will introduce other control loop after being triggered when the capacitive coupling circuit is used in a closed loop scheme, the transient stability analysis is getting more complicated, which is very necessary to make sure it works robustly.

In this work, an adaptive biasing error amplifier with a low-power dynamic push-pull SRE circuit is applied to a capacitor-less LDO to show enhancements in transient responses. This chapter is organized as follows. Concept of the proposed LDO is discussed in Section 2. Circuit design and implementation are shown in Section 3. Experimental results and conclusions are given in Sections 4 and 5, respectively.

2 Design of the Proposed Circuits

As shown in Fig. 1, the basic structure of this ultra-fast capacitor-less LDO is similar with [13] focusing on dynamic biasing. It is constructed by two differential common-gate transconductance cells, a voltage buffer, a current-summation circuit and an additional SRE circuit. The two G_m cells, which are made basically by a pair of matched transistors (M_a and M_b in Fig. 1 as an example) in the form of a current mirror, are cross-coupled achieving a push-pull output stage to inject and withdraw

more current for charging and discharging during the transient instant. Because the output current I_o has a quadratic dependence on its input-voltage difference according to the square-law characteristic of MOS transistor, the maximum output current I_{omax} is no longer limited by the constant-current source as in the case of conventional amplifier with a tail-current. This is very practical for fully on-chip LDOs to improve transient response since low power and high slew rate can be realized at the same time.

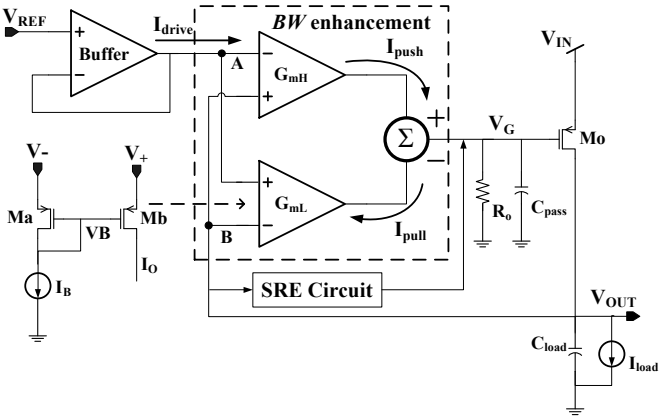


Fig. 1. Conceptual schematic of the proposed capacitor-less LDO regulator

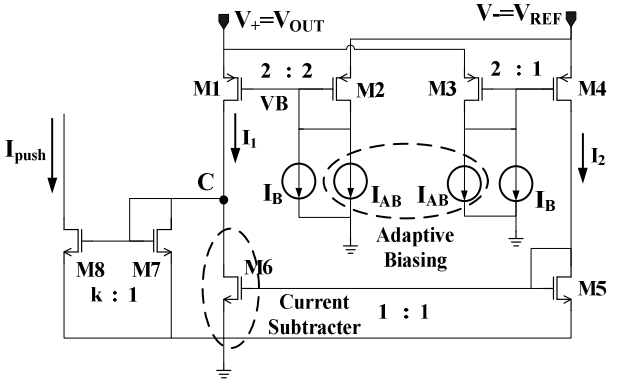


Fig. 2. Principle of the high bandwidth transconductance amplifier G_{mH}

Although the SR-limit problem has been improved by enabling a higher bias current during the transient instant, this differential common-gate amplifier has limited input common-mode range (ICMR) and, most importantly, limited bandwidth which is determined by transconductance G_m and gate capacitance C_{pass} of the power transistor as shown in Fig. 1. Therefore, fast changing voltage spike cannot be detected effectively by the amplifier at low bias current. Moreover, this approach is

not applicable when V_{OUT} is at a small value, which happens when providing an adaptive supply for a power-saving SoC design. To combat the aforementioned challenges, a current efficient and high bandwidth error amplifier with a dynamic push-pull SRE circuit is proposed in this chapter.

2.1 Adaptive Biasing Error Amplifier

It is obvious that a larger transconductance G_m means a larger GBW and faster transient response at the gate of the power transistor, which requires more power applied to the LDO. However, the traditional methods to improve G_m of this simple common-gate amplifier have some difficulties to be realized. For instance, a large bias current I_B will increase the minimum input voltage for the amplifier, deteriorating ICMR; also increasing the aspect ratios of input transistors may put them into weak-inversion region when a low quiescent current has been adopted. Here, a current-mode method called current subtracter can be utilized to resolve this problem. As shown in Fig. 2, another duplicated common-gate amplifier (M_3-M_4) has been cross-coupled with M_1-M_2 to provide a current I_{M4} that varies contrarily compared to I_{M1} and is redirected to node C. The only difference is the aspect ratio of input transistors, which is 2/1, to guarantee a normal bias point of the total output current I_{push}. The larger a voltage pike ΔV_+ is, the more I_{push} will be gained compared to using M_1-M_2 alone. As a result, the total transconductance G_m is enhanced by a factor of 1.5 as given by

$$G_m = k\left(g_{m1} + g_{m4}\right) = 1.5kg_{m1} \tag{1}$$

where k is the gain of current mirror M_7-M_8 and set to be 3 in the circuit for boosting output-driving ability. This structure has nearly the same effects as increasing I_B to increase G_m while introducing less pressure on ICMR design.

Note that the power transistor can be designed to work in linear region when heavy load occurs, such that a more efficient usage of the chip area is achieved. In saturation region, the relationship between I_d and V_{gs} is quadratic, and in linear region, it is linear, where an equal factor of increment in I_d requires a larger increment of V_{gs}. Therefore, the circuit needs larger bandwidth and slew rate at heavy load for high speed control, which is achieved successfully by adaptive biasing [9]. The operation revolves around sensing the output current of the regulator and feeding back a ratio of the current to the input stage of the amplifier. This can be done by a simple current mirror and a sense MOSFET that are area efficient. In addition to the small fixed biasing current I_B, a feedback current I_{AB} relating to load current I_{load} (i.e., $I_{AB}=\beta I_{load}$) is applied to the drain of transistor M_2 to control V_{gs2} at different loads. Because V_{gs1} and V_{gs2} are equal at DC operating point, the transconductance g_{m1} of M_1 can be expressed as

$$g_{m1} = \sqrt{2\mu_p C_{ox}\left(W/L\right)_1\left(I_B + I_{AB}\right)} \tag{2}$$

The resulting larger bias current at heavy loads increases transconductance of the input pair, leading to a larger bandwidth of the amplifier. During low load current

conditions, the feedback current I_{AB} is negligible, yielding a high current efficiency and not aggravating battery life.

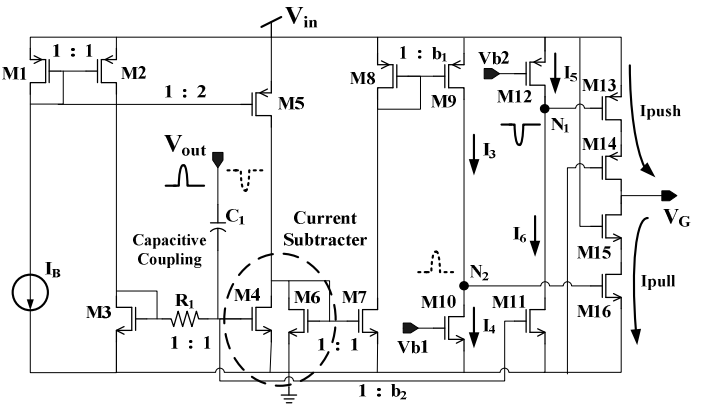
One important design issue is about carefully setting I_{AB} or aspect ratio β between the current-sense transistor and power MOSFET at different loads. Too small β will not gain dynamic biasing advantages; however, since M_2 is diode-connected and the input V_- is a stable reference voltage, too large β will introduce more feedback current I_{AB} to the input stage pushing V_B to a very low voltage especially when V_{OUT} is small, which may result in transistors in the current source of I_B and I_{AB} entering into linear region. If this unluckily happens at large load current, there exists no isolation between ground and bias voltage V_B. The ground noises will couple freely to the gate of input transistors, degrading performances of the amplifier. In this circuit, the largest load current is 100mA and the aspect ratio of I_{load}/I_{AB} is chosen as 10000/1, where the largest feedback current is approximately 10μA.

2.2 Dynamic Push-Pull SRE Circuit

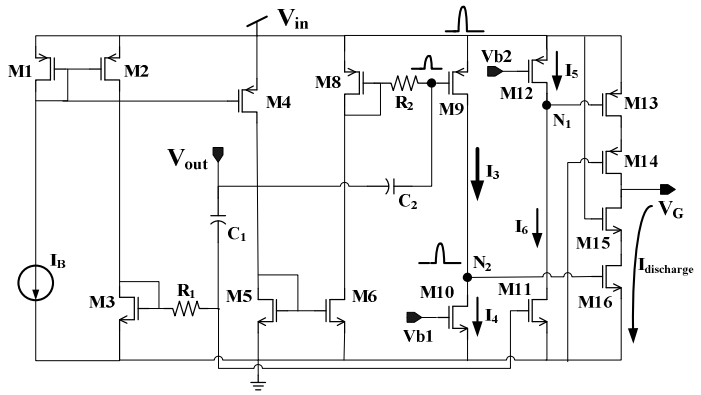
Unluckily, the adaptive biasing is activated only when the gate voltage of the power MOS (V_G) goes down (i.e., when the feedback is going to compensate an abrupt increment of load current). However, if the load current suddenly increases, an amount of time occurs before V_G is moved down and before the adaptive biasing is activated, which is determined by the bandwidth of the loop. This latency may strongly reduce effectiveness of the adaptive biasing. For example, when the load current steps down from heavy load to light load, the fast charging of the pass transistor gate enables small overshoot and fast recovery of the LDO output voltage. However, the biasing current of the amplifier is low at light load that leads to a large undershoot of the output voltage when the load current steps up from the minimum to the maximum in a very short time.

1) Principle of Operation: In order to get rid of the dependence on limited bandwidth and reduce output voltage spikes and recovery time further, a SR enhancement (SRE) circuit based on dynamic push-pull (DPP) techniques is implemented in parallel with the AB error amplifier to get a better regulated power supply. The SRE circuit only provides a dynamic current to charge or discharge gate capacitance C_{pass} of the power transistor during transient if large voltage spikes take place, and is completely turned off in the static state, dissipating small quiescent current. It should improve both loop-gain bandwidth and slew rate at the gate drive of power transistor, while maintaining high current efficiency in static state.

Normally, the SRE circuit consists of a sensing and driving circuit [21]–[23]. How to avoid a larger loading capacitance due to additional structures as well as high dynamic current at input stage in these existing methods is critical. For example, a current-detection SRE circuit detecting changes in the current signal at active load of the core amplifier is reported in [8]. The advantage is that it does not increase the loading of error amplifier.



(a)



(b)

Fig. 3. DPP SRE circuits with capacitive coupling (a) Proposed DPP techniques (b) DPP structure with two coupling capacitors

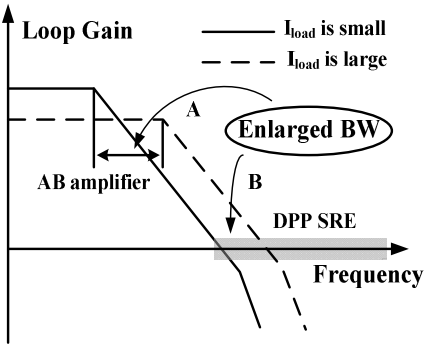


Fig. 4. Sketch map of improvements for the loop bandwidth

In the proposed structure shown in Fig. 3(a), the sensing circuit adopts a voltage detection method based on capacitive coupling. It senses rapid transient voltage changes at the output of the LDO and then changes current signal I_{M4} or I_{M11} to trigger a dynamic push-pull circuit for increasing the driving current momentarily. The basic circuit is a modification to current mirrors M_3-M_4 and M_3-M_{11}, where capacitor C_1 and resistor R_1 have been added to realize a high-pass filter. It provides a fast path to detect the output voltage spikes. As shown by the timing diagrams in Fig. 3(a), when the amplitude of V_{OUT} changes from low to high (ΔV) instantaneously (represented by the real line), the rapid voltage change couples to the gate of M_{11} directly due to the high-pass property of C_1. When C_1 is chosen to be much larger than C_{gs3}+ C_{gs4}+C_{gs11}, the gate voltage of M_{11} is dominated by the coupled signal from C_1 in this instant. Thus, V_{gs11} is changed momentarily and the extra current ΔI_6 can be found from [14]

$$\Delta I_6 \approx g_{m11}\Delta V = \sqrt{2b_2 I_B \mu_n C_{ox} \left(W/L\right)_{M11}}\,\Delta V \tag{3}$$

It is found that a larger aspect ratio of the current mirror helps to increase ΔI_6 for injecting more transient current, but at the penalty of increased quiescent current in steady state. Therefore, the size of M_{11} should be carefully designed to strike a balance between the above tradeoffs. This consideration is also applicable to transistor size design of M_4. When V_{OUT} changes from high to low (represented by the dotted line), the coupling effect generates a smaller I_{M4} and triggers the pull action. When V_{OUT} stays at a constant voltage in the steady state, C_1 is open-circuited, resulting in an auto shutdown of the current boosting circuit. Besides, this coupling effect is independent of the DC value of V_{OUT} due to the high-pass characteristic of C_1, so the proposed method is suitable for detecting any output voltage level, improving ICMR of the amplifier considerably.

The driving circuit is composed of transistors M_9-M_{16}. Based on the appropriate ratios of current mirror (b_1, b_2), M_9 and M_{10} (M_{11} and M_{12}) are designed such that if both transistors operate in the saturation region, their drain currents must meet the relationship $I_3<I_4$ ($I_5>I_6$). So M_{10} and M_{12} operate in the triode region such that voltages of node N_1 and N_2 are set to "1" and "0" to force transistors M_{13} and M_{16} to be turned off at steady state.

Once the load current decreases quickly and causes large output variations, the extra current ΔI_6 is generated to pull the voltage of node N_1 down. Then transistor M_{13} will then be heavily turned on to charge the gate capacitance of power transistor. When V_{OUT} is regulated back to its expected voltage in the steady state, I_6 decreases and the voltage of node N_1 is smoothly reset to "1" to turn transistor M_{13} off.

2) Sensitivity to Supply voltage: Similarly, the transistor M_{16} can be turned on by pulling the voltage of node N_2 high to discharge the gate capacitance during the negative slewing period. As shown in Fig. 3(b), the traditional method to increase a PMOS current I_3 momentarily is just by pulling down the gate voltage directly [14]. However, there exist some problems for this structure. First, additional high-pass filter devices (R_2 and C_2) are needed, occupying large chip area inevitably. Second, it is sensitive to supply voltage variations. This is because when a large coupling capacitor C_2 has been connected to the gate of M_9 in Fig. 3(b), the bandwidth of current mirror M_8-M_9 is degraded due to the largely increased capacitance at the gate.

As a result, the gate voltage V_{G9} cannot follow variations of the supply voltage in low-power design. For example, when V_{IN} increases fast, V_{GS9} may be enlarged instantaneously. I_3 is thus increased, having the potential risk to pull the node voltage V_{N2} high and turn on M_{16} falsely. An unwanted discharging current $I_{discharge}$, depending on the amplitude of ΔV_{IN}, flows to the gate of power MOS and tries to pull V_G down. So the output voltage of the LDO is increased and must be regulated by the negative feedback loop in a certain time. Moreover, if V_{IN} decreases rapidly, M_9 may be shut down to delay the pull function of SRE circuit, because only a small bias current is used here to pull V_{G9} low. The PSRR and line-transient performances are therefore degraded, which has a similar phenomenon in [14].

The simplest solution is with the help of an RC filter in line with the power supply to filter out fluctuations before they reach the SRE circuit. However, the high power losses and reduction in voltage headroom caused by this resistor when the SRE circuit is triggered would severely limit its size, pushing the pole to high frequencies. Another methodology is assisted by adding a cascode structure such as resistors into the PMOS bias current pair M_8-M_9, making the coupling circuit insensitive to supply voltage noise. However, this may reduce the transconductance at the coupling input port and the dynamic charging effect is weakened. The new idea proposed in this brief to avoid such problems is just by adopting current subtracter M_4-M_6 instead as shown in Fig. 3(a). After that optimization, only one coupling capacitor C_1 is needed leading to a smaller chip area. The main difference compared to using two coupling capacitors is that the circuit speed response for enabling charging action is degraded by additional two current mirrors (M_6-M_7 and M_8-M_9) and small bias current I_B. However, by making the sizes of these transistors small, the parasitic capacitances are set small and the time delay can be ignored. In addition, transistors M_{14} and M_{15} are used to prevent the noise of N_1 and N_2 from coupling to the gate of the power transistor when transistors M_{13} and M_{16} are turned on.

3) Optimal Sizing of Drive Transistors: The response time of the SRE circuit is determined by the time required to turn on or turn off drive transistors M_{13} and M_{16} when an output voltage spike ΔV is applied to the DPP SRE circuit. During the positive (negative) output slewing, transistor M_{12} (M_{10}) is in the saturation region. Therefore, the response time $t_{res,p}$ and $t_{res,n}$ of the SRE circuit for positive and negative slewing periods is approximately given by

$$t_{res,p} \approx \frac{\left(\left|V_{thp}\right| - \left|V_{ov,M12}\right|\right) C_{p1}}{g_{m11} \Delta V} \tag{4}$$

$$t_{res,n} \approx \frac{\left(V_{thn} - V_{ov,M10}\right) C_{p2}}{b_1 g_{m4} \Delta V} \tag{5}$$

where V_{ov} is the overdrive voltage of MOS transistor, C_{p1} (C_{p2}) is the parasitic capacitance at node N_1 (N_2). Equations (4) and (5) show that the response time increases with the value of C_{p1} and C_{p2}. Increasing the sizes of transistors M_{13} and M_{16} thus slows down response time of the SRE circuit.

On the other hand, larger size of drive transistors is critical for controlling the amount of dynamic currents to charge and discharge V_G, therefore affecting the maximum attainable slew rate. For example, assuming that M_{13} and M_{16} are in

saturation regions with constant dynamic current during the output slewing periods and the channel length modulation is neglected, the drive transistor size can then be demonstrated as

$$\left(\frac{W}{L}\right)_{M13} \approx \frac{2 \cdot SR_{+} \cdot C_{pass}}{u_p C_{ox}\left(V_{IN} - V_{ov,M11} - \left|V_{thp}\right|\right)^2} \tag{6}$$

$$\left(\frac{W}{L}\right)_{M16} \approx \frac{2 \cdot SR_{-} \cdot C_{pass}}{u_n C_{ox}\left(V_{IN} - \left|V_{ov,M9}\right| - V_{thn}\right)^2} \tag{7}$$

where SR_{+} and SR_{-} are the slew rate improvement achieved by DPP SRE circuit. One method to resolve the trade-off between speed response and SR is to enlarge g_{m4} and g_{m11} without increasing much power.

From the above analysis, it seems that the dynamic push-pull scheme adds a gain into the loop by the boosted current and can effectively enhance the transient response time for regulating the output voltage back to a stable voltage level, i.e., the circuit is used to enhance the slew rate of the error amplifier during the transient period. Because the loop-bandwidth is low-pass and limited while this feedforward path due to capacitive coupling is high-pass, the values of R_1 and C_1 can thus be selected by setting the corner frequency $(1/R_1C_1)$ a little lower than the GBW to extend the loop-bandwidth of the LDO and make sure the DPP SRE circuit only works for high frequency spikes.

Comparisons between the loop gains of the proposed LDO and circuit structure like [13] at different load conditions are shown in Fig. 4 to prove the superiority. Method A (adaptive biasing) enlarges the bandwidth at heavy load and method B (dynamic push-pull techniques) focuses on voltage variation at high frequency, all of which will lead to a faster transient response at low bias current.

3 Circuit Realization

Fig. 5 shows the schematic of the proposed LDO regulator, which consists of a PMOS power transistor M_o, a current-sensing circuit, a high slew-rate push-pull error amplifier, a SRE circuit and a reference buffer. The push-pull output stage constructed with transistors M_{13} and M_{20} facilitates the LDO regulator using only moderate size M_o to provide a wide range of load currents. In this circuit, to provide 100mA load current with 150mV dropout, the aspect ratio of $(W/L)_{Mo}$ is chosen to be 15000μm/0.35μm in a 0.35μm standard CMOS process where the threshold voltage $|V_{thp}|$ of M_o is about 0.66V.

The error amplifier is mainly constructed of two cross-coupled common-gate cells G_{mH} and G_{mL}. Here some transistors like M_2 and M_3 have been reused in both input stages of the cells. The typical bandwidth of a LDO with 100mA output capability is about 200kHz to 1MHz [1]–[3]. Assuming the corner frequency is set to be about

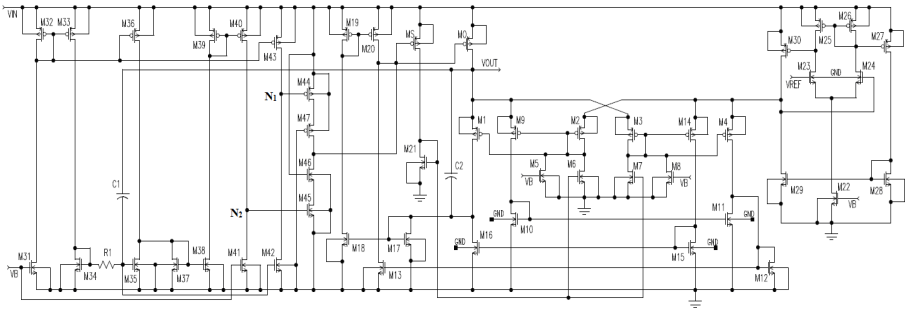


Fig. 5. The proposed ultra-fast capacitor-less LDO with a reference buffer

100kHz, the required passive components R_1 and C_1 are 3pF and 500kΩ respectively, where the accuracy is not important. Current mirrors M_{12}-M_{13} and M_{19}-M_{20} are used to realize a current-summation circuit. To ensure the amplifier has fast-transient responses and large voltage-gain, the channel lengths of all transistors except M_o are designed to be five times of the minimum feature size to guarantee that all the parasitic poles are at high frequency.

Since most of voltage references do not have output current driving ability [24], a voltage buffer without frequency compensation is introduced here to transfer the voltage V_{REF} to the inputs of the G_m cells. Because adaptive biasing is utilized in the circuit, the resulting bias current for the amplifier is increased at heavy load, which requires an enhanced driving current I_{drive} from the buffer. Therefore, the aspect ratio $(W/L)_{M30}$ should be designed to satisfy the maximum driving ability without using a large overdrive voltage, which must be always smaller than the dropout voltage at different loads. Otherwise, M_{30} may enter into linear region when the difference between V_{IN} and V_{OUT} is small. This will provide a low-resistance path where the supply noises can couple to inputs of the G_m cells, degrading PSRR greatly. Furthermore, the bandwidth of the buffer should be designed to satisfy the maximum bias current variation rate when the load current changes from light load to heavy load. If not it will cause large voltage droop at the output of the buffer, deteriorating transient responses.

As shown in Fig. 5, because the output of the LDO is connected to a low-resistance node such as the source terminals of M_1 and M_3 inside the G_{mH} cell, this sets the dominant pole p_1 locating at the gate of the power transistor and the output pole p_2 of the LDO to be non-dominant. As both drive transistors M_{44} and M_{45} are off in the LDO during the static state, there is almost no difference between the ac responses of the LDO with and without the SRE circuit. Here four parts mainly contribute to total output load capacitance C_{load} in this structure, including C_{db} of the power MOSFET, input capacitors C_{in} from G_m cells, coupling capacitor C_1 from DPP SRE circuit and the parasitic output capacitance C_{par} due to the metal lines for on-chip power distribution which is generally in the range of 10–100pF [9]. By using the circuit proposed above, more input transistors and capacitors are implanted at the output of the LDO compared to [13], C_{load} is therefore unluckily increased pushing p_2 to lower frequency, which may degrade phase margin of the feedback loop. This stability may be even worse when a large parasitic capacitance C_{par} and small I_{load} are applied [20].

In order to realize pole splitting under a wide range of I_{load} from several tens of milliamperes to several μA and occupy less silicon area, the active capacitor multiplier is adopted for Miller compensation [25]. Here, capacitor C_2 performs the multiplied-miller capacitor with current buffer. The overall equivalent miller capacitor C_c is equal to kC_2, where $k=(S_{18}/S_{17})\times(S_{20}/S_{19})$ and $S_i=(W/L)_i$ is the aspect ratio of the i-th transistor.

Assuming G_{m1} and R_{o1} are the equivalent first stage transconductance and output resistance of the LDO, g_{mo} and C_{pass} are the transconductance and gate capacitance of the power transistor, R_{out} is the overall output resistance, the frequency response can then be given by

$$p_1 = 1/\left[\left(C_{pass} + C_c g_{mo} R_{out}\right) R_{o1}\right] \tag{8}$$

$$p_2 = \left(g_{mo} + 1/R_{out}\right)/\left(C_{load} + C_{pass}\right) \propto \sqrt{I_{load}} \tag{9}$$

$$GBW = g_{mo}/\left[C_{pass}/\left(G_{m1}R_{out}\right) + C_c g_{mo}/G_{m1}\right] \propto \sqrt{I_{load}} \tag{10}$$

Here the input resistance $1/G_{m1}$ of the error amplifier mainly determines R_{out}. Because adaptive biasing is applied, poles and GBW are changed accordingly in different load conditions as shown in equations (9) and (10). In order to make sure a phase margin larger than 45°, p_2 should be larger than GBW to determine the total Miller capacitor C_c.

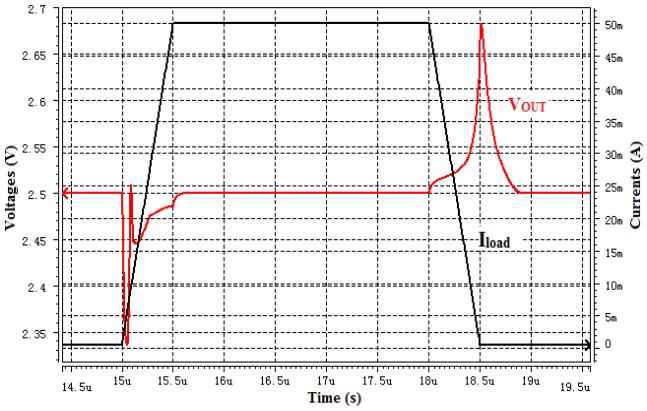
$$C_c > \frac{G_{m1}R_{out}}{1+g_{mo}R_{out}}\left(C_{load}+C_{pass}\right) - \frac{C_{pass}}{g_{mo}R_{out}} \simeq \frac{G_{m1}C_{load}}{g_{mo}} \tag{11}$$

The minimum load current for the LDO to ensure stability is 0.5mA. Normally, the parameter $g_{mo}R_{out}$ or g_{mo}/G_{m1} is set large enough to make this compensation achieved without using any large on-chip compensation capacitors. In this design, the required compensation capacitor C_2 is only 2.3pF. Area efficiency of such LDO regulator is thus maintained, which is particularly suitable for chip-level power management. Also the capacitor multiplier introduces a left-hand plane zero z_1 (g_{m17}/C_2) at a relatively high frequency, which can be designed near the output pole p_2 to add phase and optimize frequency compensation.

4 Experimental Results and Discussion

The proposed capacitor-less LDO has been implemented in standard 0.35μm CMOS technology. The circuit was designed to provide 2.5V output voltage at 100mA output current for input voltage greater than 2.65V.

Load transient behavior, which is mainly decided by SR and its bandwidth of the LDO, is simulated here at to evaluate the transient performance. Fig. 6 shows the load-transient responses with a 100pF off-chip output capacitor, which is used to



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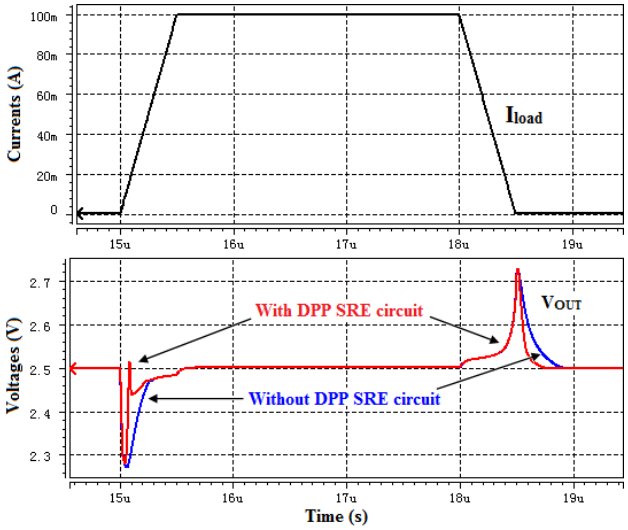
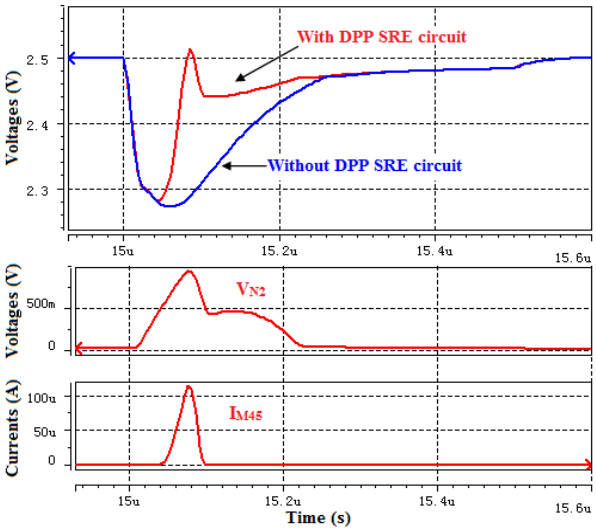


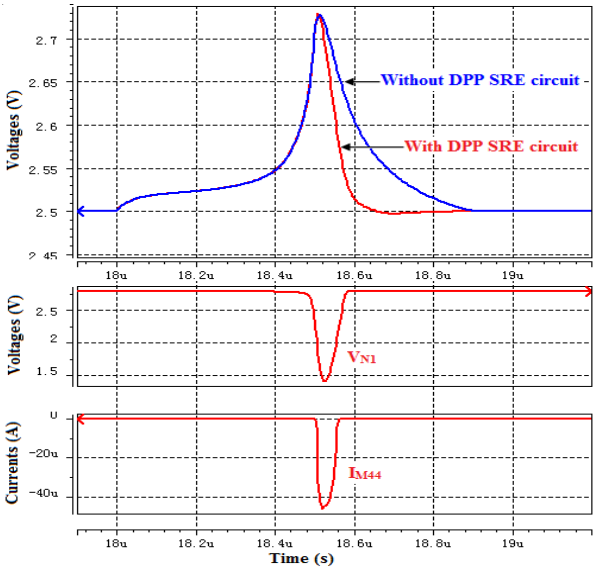
(b)

Fig. 6. Simulated load-transient responses with a 100pF off-chip output capacitor for different current changes (a) ΔI_{load}=50mA (b) ΔI_{load}=100mA

model the output-parasitic capacitance from the metal lines. In Fig. 6(a), I_{load} varies from 0.5mA to 50mA and V_{IN} is 2.8V, while the load current change is increased to 100mA in Fig. 6(b). The results show that the output voltage can be fully recovered within 0.7μs at a voltage spike less than 229mV. It can be also observed in Fig. 6(b) that with the use of DPP SRE circuit in the LDO, which only consumes 29.4% additional static current, significant improvement in transient responses can be achieved in low-power condition.



(a)

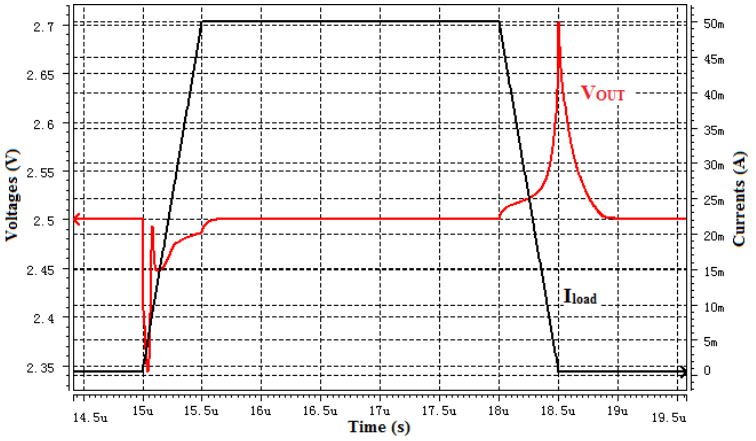


(b)

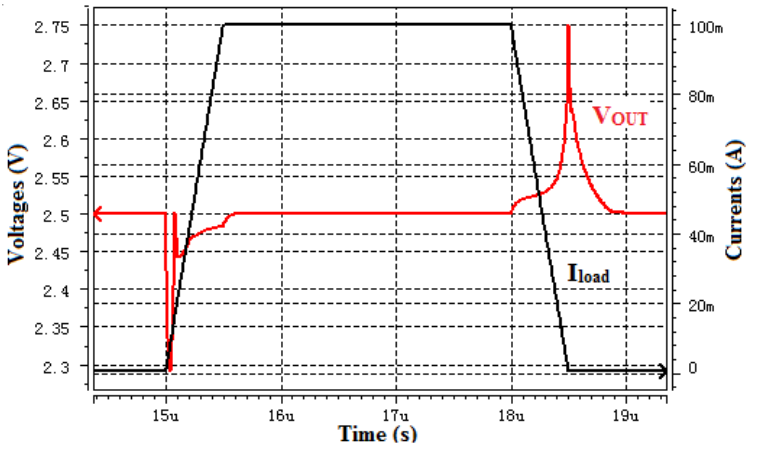
Fig. 7. Partial enlargement of the voltage spikes for a 100pF off-chip output capacitor and 100mA load current change (a) undershoot (b) overshoot

The working process and advantage of the DPP SRE circuit can be analyzed in detail in Fig. 7. For example, when the load current changes from the light load to heavy load, a large undershoot occurs at the output. The current comparator (M_{40}/M_{41}) takes effect to pull the node voltage V_{N2} high and turn on drive transistor M_{45} heavily. A dynamic current I_{M45} (more than 100μA) can be provided to reduce the

output-voltage excursion during transient. In addition, the pole located at the gate of the power transistor will be shifted to a higher frequency due to the turn on of drive transistor M_{45} during transient, thereby improving the bandwidth of the LDO. The settling time is therefore improved by about 2.9 times when a 100mA output-current change is applied. The phenomenon for the overshoot reduction is similar in Fig. 7(b).



(a)



(b)

Fig. 8. Simulated load-transient responses without an off-chip output capacitor for different current changes (a) ΔI_{load}=50mA (b) ΔI_{load}=100mA

The load-transient responses without an off-chip output capacitor are shown in Fig. 8. The current change ΔI_{load} are chosen as 50mA and 100mA again respectively. Measurement results show that the proposed capacitor-less LDO can be fully recovered within 0.8μs at a voltage spike less than 250mV.

From the simulation results shown above, it can be seen that the DPP SRE circuit aids in adjusting the power MOS in the transient response effectively to avoid large output spikes, where the voltage deviation and response time are much better than that in [13] even at a twice load current change. The sizes of driving transistors in SRE circuit have been optimized to avoid overcharging at the gate of M_o and good stability of the LDO regulator can be achieved.

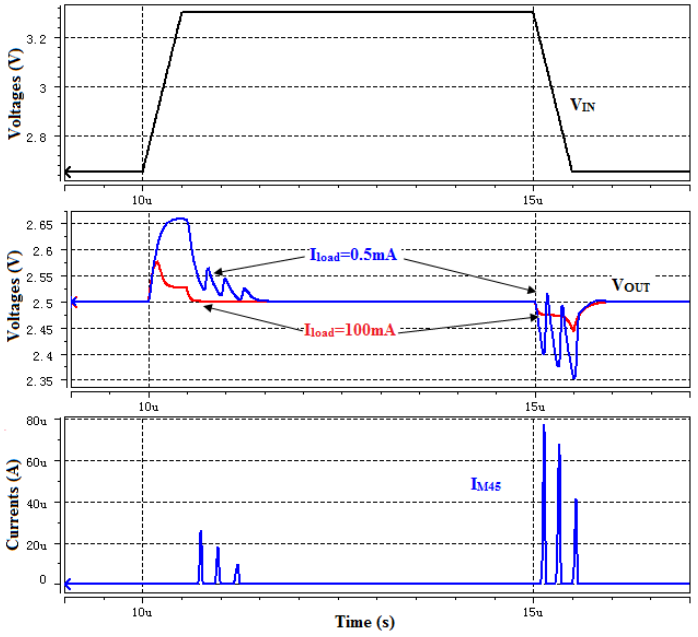


Fig. 9. Simulated line-transient response with a 100pF off-chip capacitor

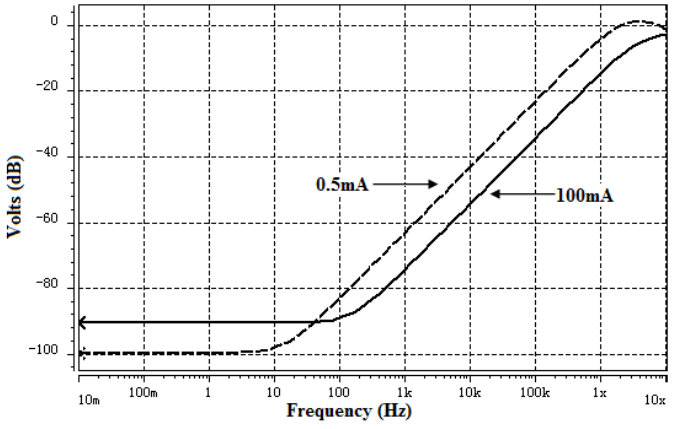


Fig. 10. Simulated PSRR versus frequency for I_{load}=0.5mA and I_{load}=100mA when V_{REF}=2.5V, V_{IN}=2.8V and C_{load}= 100pF

To prove the DPP SRE circuit is not sensitive to supply voltage variations because of a current subtracter introduced, the line-transient is therefore simulated. The line-transient response with a 100pF off-chip output capacitor is shown in Fig. 9, where V_{IN} varies from 2.65V to 3.3V. The result shows that the output voltage can be fully recovered within 1μs at a voltage spike less than 76mV when I_{load} is 100mA. No dynamic spurs and injected noise occur and the circuit works robustly. However, if the load current is small, the bandwidth of the LDO is decreased, which may introduce a larger voltage spike and trigger the pull function of the DPP SRE circuit in a certain time. Because Miller compensation is adopted to guarantee sufficient phase margin during transient as analyzed before, the small ringing can be attenuated quickly without affecting the transient performance. Finally, power-supply ripple rejection (PSRR) against different load currents is shown in Fig. 10. The proposed LDO can achieve about 74dB PSRR at 1kHz when I_{load}=100mA.

Table 1. Performance Comparison With Previous Published Work

	[9]	[13]	[14]	[20]	This Work
Technology(μm)	0.09	0.18	0.35	0.35	0.35
Input voltage V_{IN}(V)	1.2	1-1.8	0.95-1.4	3-4.2	2.65-3.3
Dropout voltage V_{DO}(mV)	300	100	200	200	150
Quiescent current I_Q(μA)	6000	1.2	43	65	10 (no load)
Output current I_{load}(mA)	100	50	100	50	100
Load regulation(mV/mA)	N/A	0.148	∼0.4	∼0.56	0.005
Line regulation(mV/V)	N/A	3.625	N/A	∼23	0.38
Settling time T_{settle}(μs)	0.00054	∼2.8	∼3	∼15	∼0.5
FOM(ns)	0.032	0.067	1.29	19.5	0.05

Table 1 shows performance comparison with some previously reported capacitor-less LDOs. A figure of merit (FOM=T_{settle}×I_Q/$I_{load(max)}$) used in [9] and [13] is adopted here to evaluate different current efficient designs for improving transient response. The response time T_{settle} (T_{settle}=C_{load}×ΔV_{OUT} /$I_{load,max}$) is found from C_{load} for a specified $I_{load,max}$ and ΔV_{OUT}. A lower FOM implies a better slewing performance, where the proposed regulator has the lowest FOM (0.05ns). This feature is very important and attractive to any high-density SoC applications.

5 Conclusion

This chapter presents an ultra-fast, capacitor-less LDO with an advanced common-gate error amplifier and DPP SRE circuit. Some low-power methods like adaptive biasing and capacitive coupling have been adopted to improve both ICMR and loop bandwidth of the error amplifier greatly, while maintaining the traditional advantages such as low quiescent current and small chip area. By applying them to a LDO with a power-efficient methodology, the accuracy and response speed are significantly enhanced. The experimental results confirm that overshoots and undershoots in load transient of the LDO are improved greatly as results from the loop-gain-bandwidth enhancement. The performances are especially encouraging in chip-level power management.

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