Reconfigurable Computing for High Performance Networking Applications

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It is now forecast that Terabit Ethernet will be needed in 2015. (A 1 Tb/s data rate means that the estimated memory capacity of a typical human could be transmitted in 24 seconds.) In this talk, Gordon Brebner will give an overview of research which demonstrates that Field Programmable Logic Array (FPGA) devices can be main processing components for 100-200 Gb/s networking, a main event horizon in 2010, and points the way to how techniques might scale (or not) towards a 1 Tb/s transmission rate by 2015. The highly configurable, and reconfigurable, characteristics of such devices make them a unique technology that fits with the requirements for extremely high performance and moreover for flexibility and programmability. Aside from discussing the physical technological properties, the talk will cover work on higher-level programming models that can make the technology more accessible to networking experts, as opposed to hardware/FPGA experts.

Gordon Brebner is a Distinguished Engineer at Xilinx, Inc., the worldwide leader in programmable logic solutions. He works in Xilinx Labs in San José, California, USA, leading an international group researching issues surrounding networked processing systems of the future. Prior to joining Xilinx in 2002, Gordon was the Professor of Computer Systems at the University of Edinburgh in the United Kingdom, directing the Institute for Computing Systems Architecture. He continues to be an Honorary Professor at the University of Edinburgh, is a Ph.D. advisor at Santa Clara University, and is a visiting lecturer at Stanford University. Professor Brebner has been researching in the field of programmable digital systems for over two decades, presenting regularly at, and assisting with the organization of, the major international conferences in the area. He has authored numerous papers and holds many patents.

A. Koch et al. (Eds.): ARC 2011, LNCS 6578, p. 1, 2011.