Design of Multifunction Vehicle Bus Controller

Zhongqi Li, Fengping Yang, and Qirong Xing

College of Electrical & Electronic Engineering, East China Jiaotong University, Nanchang, P.R.China
lzq0828@163.com

Abstract. The Train Communication Network (TCN) is widely used in high-speed train. However, its core technology - Multifunction Vehicle Bus Controller (MVBC) is owned by foreign companies, which limits the development of high-speed railway in China. Based on the principle of Multifunction Vehicle Bus(MVB), and analysis of real-time protocol and functions of bus controller to be achieved, this paper describes the design of MVBC which is divided into seven modules, Encoder, Decoder, Telegram Analysis Unit(TAU), Configuration Memory, Traffic Memory Controller(TMC), Arbitrator and Microprocessor Control Unit(MCU). And then it designs each module with VHDL in the integrated development environment of Quartus Ⅱ developed by Altera Company. A new MVBC is developed with FPGA. The test shows that it can take place of MVBC Application Specific Integrated Circuits (ASIC).

Keywords: TCN, MVB, MVBC, FPGA.

1 Introduction

The TCN bus was standardized in the Plenary Session of the IEC Technical Committee 9, Kyoto, Japan, October1999, which resulted to the IEC 61375 Standard. The IEEE Vehicular Society also standardized the TCN bus, which resulted to the IEEE 1473-T Standard. The main goal of the TCN is to set a single train equipment specification that is compliant with the requirements/needs of different railway service providers and to warrant the interconnection of any number of different vehicles/units from possibly different manufacturers in the same train.

MVB is one component of TCN. The MVB is the Vehicle Bus specified to connect standard equipment, located in the same vehicle, or in different vehicles in the TCN. The MVB can address up to 4095 devices, of which 256 are stations capable of participating in message communication. In order to allow these devices to communicate with each other, a common communication interface card is designed which is independent of the chosen physical layer and functions associated with each device. The MVBC is an ASIC chip which realizes the physical and major parts of the link layer protocol of the MVB.

2 System Description and Architecture

The MVB Controller contains the encoders/decoders and the logic to control the Traffic Memory, which decodes the incoming frames and addresses the Traffic Memory

D. Li, Y. Liu, and Y. Chen (Eds.): CCTA 2010, Part IV, IFIP AICT 347, pp. 177–183, 2011.

accordingly. This paper describes the design of MVBC which is divided into seven modules that is Encoder, Decoder, Telegram Analysis Unit(TAU), Configuration Memory, Traffic Memory Controller(TMC), Arbitrator and Microprocessor Control Unit(MCU). Fig 1 is MVBC architecture.

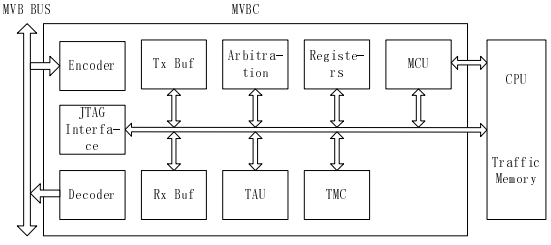

Fig. 1. MVBC architecture

Implementation steps of the controller function as follows, chip power, reset, configure the device address, models and other services, start work. When sending data, MCU reading the corresponding data from Traffic Memory(TM). write to send buffer, then MCU send instructions of send data to the encoder. When accepting data, the Manchester decoder receiving signals from the bus controller, upon decoding, verification and data is written in receive buffer, and notifies the main control unit. MCU read data from the receiving buffer, writes corresponding area of TM. MVBC communicate with the microprocessor through TM which uses dual-port RAM.

2.1 Encoder

Encoder engages in Manchester encoding of Master_Frame and Slave_Frame, and generation and sending CRC check sequence. Above-mentioned work is controlled by MCU. The specific tasks of the module are as follows: (1) The parallel data are extracted from the buffer, (2) The parallel input data transform into serial data suitable for MVB, (3) Add to delimiter for ready to send data, (4) According to the length of ready to send data, add one or more 8-bit CRC check_sequence. (5)Manchester encode for data to be send in order to improve communication quality.

Structure of encoder according to the above design of the task is as follows, Digital control unit, Parallel Convert Serial Unit, Frame Delimiter Unit, FIFO unit, Multi-selector unit, CRC Generation Unit, Manchester encode unit. The structure is shown in Fig 2.

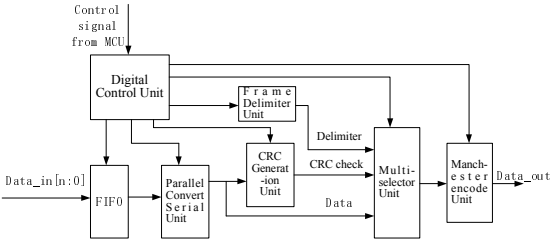

Fig. 2. Encoder architecture

Digital control unit plays a controlling role of the operation of the other. First Input First Output(FIFO) unit is the input data buffer. Frame delimiter unit is the role as follows; add to Start_Bit for frame, Start Delimiter of Master_Frame, Start Delimiter of Slave_Frame. Parallel Convert Serial Unit read data from buffer and convert parallel data to the serial data. Manchester encode unit encodes data on the communication. Outgoing data CRC check sequence generated by CRC generation unit. When the data output, Multi-selector unit selects the starting delimiter, outgoing data and the CRC check code.

2.2 Decoder

The main functions of the decoding module include Manchester decoding and error detection of received data, then decoded without error serial data convert to parallel data which stored in the buffer zone and supply of top applications. Decode is the anti-process of encode which will have decoded data encoded, it is also the original appearance of data. The task of error detection mainly includes the error detection of CRC check code, error of frame length and error of Manchester skipping, etc.

Decoder includes decoding control unit, the detection of start bit unit, delimiter detection unit, Manchester decode unit, Serial Convert Parallel Unit, FIFO unit, CRC check unit and the length check unit. The structure is shown in Fig 3.

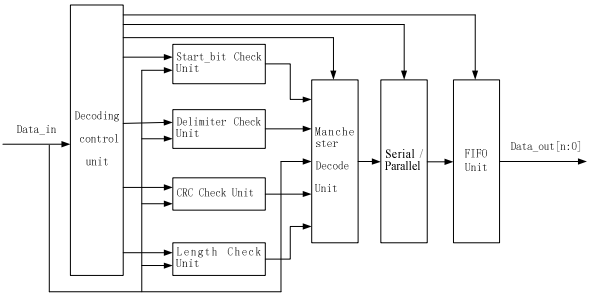

Fig. 3. Decoder architecture

2.3 Memory Configuration

Memory Configuration module read and write configuration registers of MVBC and CPU which consists of 27 8-bit configuration registers and 4 8-bit registers buffer which composed of PCS. The following memory is used in MVB communication, TM, TxBuffer, RxBuffer and InterRegister whose access mode include internal and external access and internal and internal access. Internal and external access include CPU←→TM, CPU←→InterRegister, RXBuf→TM, TM→TXBuf, TM→MFR. Internal and internal access include RXBuf→MFR, MFR→TXBuf.,Two sets of configuration register access mode is designed to achieve these two access functions which includes internal access and external access, so you can guarantee that two access patterns at the same time, and without conflicts and impact.

Internal access mode use a dedicated signal line to achieve an internal read-write access in which read access is through the direct connection method to achieve fast access, while the form of written interview by paragraph to visit it to each configuration register which is divided into paragraphs (up to 16), identify by paragraph address and data. So long as we know the corresponding data segment address and the segment can be achieved within the configuration register access.

In the external access mode, then use a common bus address to visit. As the external access is targeted TM or CPU, on the TM and the CPU access is controlled by TMC and ARB.

2.4 Telegram Analysis Unit

TAU is mainly responsible for the analysis of telegram. The received packet is passed to the control unit results MCU, then according to the feedback control unit to the corresponding treatment. There are eight kinds of situations. TAU is composed of timer and state machine. Fig 4 is TAU architecture.

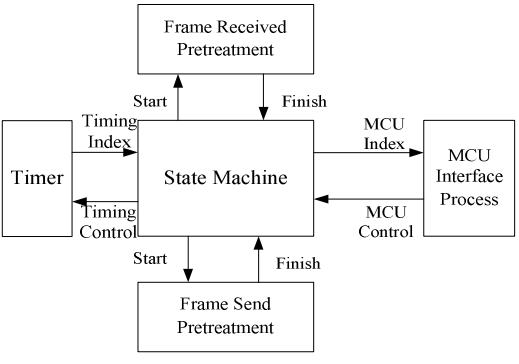

Fig. 4. TAU architecture

State machine is responsible for the analysis of the telegram and the corresponding control. Timer with the state machines perform a variety of timing tasks, while ensure the successful completion of state machines to switch among various states and the corresponding operation.

2.5 Traffic Memory Controller

TMC is composed of sink time manager、master state machine、word access state machine and selector. Master state machine controls all of TM and generates control sequences. Each word can be accessed by controlling word access state machine. When word being accessed completely, the word will automatically add an access counter, up access to all word. Word access state machine is formed by the five state, IDLE STATE, ACC_BEGIN STATE, WAIT STATE, W_TMRDY STATE and DATA_VALID STATE. Transition among states is shown in Fig 5.

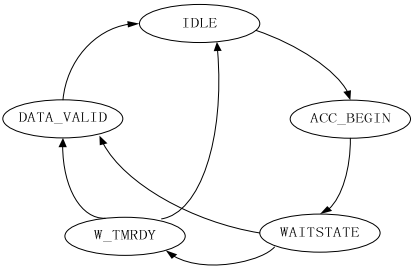

Fig. 5. Transition among states

2.6 Traffic Memory Controller

Arbitrator is used to solve the conflict when CPU and MVBC access TM at the same time, arbitrator at the same time allows only one access TM.

2.7 Microprocessor Control Unit

MCU is a core part of MVBC almost control all the other modules work, play a role in overall control. MCU is not directly involved in concrete action, but by controlling the other modules to complete the appropriate action treatment. MCU is composed of the distribution of Master frame, port pretreatment, port post-processing, Transport Data Unit, command processing unit. MCU architecture shown in Figure 6.

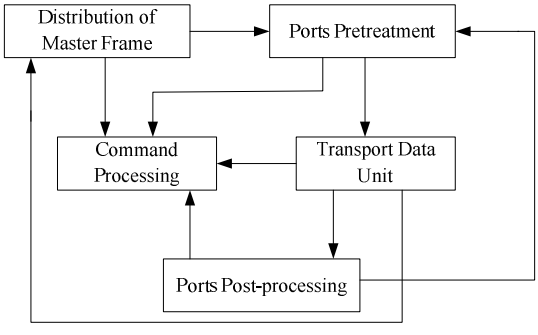

Fig. 6. MCU architecture

3 Simulation

Fig 7 and Fig 8 shows the simulation result of Master Frame of process data and Slave Frame of process data simulated in Quartus Ⅱ. In Fig.7, F_code is 0000 which means 16 bit process data. The corresponding response frame is 16-bit. The last 12 bit of master frame is Logical address of process data. Data_out is main frame of process data which includes a frame header, frame end, and CRC checksum. Send_end is high that means sending master frame of process data is over. The delimiter and checkout value is successfully added. The simulation result of Salve Frame is shown in Fig.8.

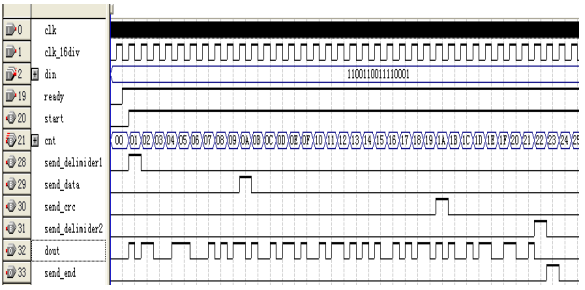

Fig. 7. Simulation of Master Frame of process data

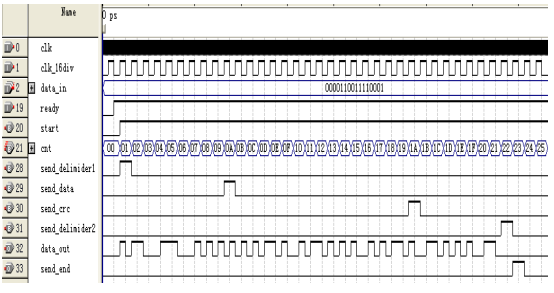

Fig. 8. Simulation of Salve Frame of process data

Fig 9 shows the simulation result of Master Frame of message data simulated in Quartus Ⅱ. In Fig.9, a Master Frame contained data is encoded.

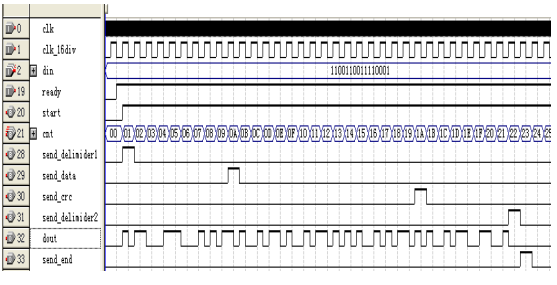

Fig. 9. Simulation of Master Frame of message data

4 Conclusions

The paper proposes a novel MVB design method using SOPC technology. The proposed MVB controller was successfully tested at a mixed MVB environment. It combines CPU and MVB controller into one single FPGA, so this method can save PCB space and reduce total power consumption. The availability of multi million-gate

FPGA devices and SOPC technology has opened the possibility to create complex single chip systems and can accelerate system performance remarkably.

With the SOPC technology, we have created a novel design and implementation method of the MVB controller. This method can great reduce the chip numbers and card size and power consumption relative to the traditional method. And the design is based on a soft IP core, so it can be easily integrated into other applications.

Acknowledgement

The work described in this paper has been supported by Foundation of JiangXi Educational Committee (GJJ09203).

References

[1] Electric Railway Equipment—Train bus—Part1: Train Communication Network, International Electro technical Commission (IEC), IEC 61375-1 Ed.01 (1999)
[2] SIEMENS Transportation Systems, MVB_Controller ASIC, MVBCS1, Data Sheet (October 2001)
[3] Zhang, S., Zhang, S., Huang, S.: CRC Check the FPGA to achieve parallel computation. Computer Technology and Development (2), 26–62 (2007)
[4] Cai, Y.: Multifunctional compartment bus controller (MVBC) Research and Design, Master's thesis. Southwest Jiaotong University, Chengdu (2005)
[5] Jin, S., Wang, J.: FPGA-based realization of CRC encoder. Modern Electronic Technology (24), 18–22 (2005)
[6] Jiang, W., et al.: Based on the VHDL language, multi-purpose vehicle bus encoder design and analysis. Railway Communications Signal Engineering (10), 9–12 (2008)
[7] Lin, F., Ren, Z., Liu, C.: Manchester coding technology based on FPGA design. Modern Electronic Technology (17), 55–59 (2007)