Second Workshop on Highly Parallel Processing on a Chip (HPPC 2008)

It is now noncontroversial to assume that explicit, general-purpose on-chip parallelism will play a much more prominent role in future computing systems, ranging from embedded and portable systems, through servers, to compute farms and high-performance systems. What is, on the other hand, currently completely open is how such systems will be organized from the architectural point of view, how parallelism shall be exposed to the programmer (and user), as well as the nature of the parallelism (general or special purpose) that can or will be made available.

The Workshop on Highly Parallel Processing on a Chip (HPPC) takes as premise that the drive for increased application performance, technological feasibility and technological and environmental constraints (for instance on power consumption) within the next 5 to 10 years will lead to chips with a significant number (read: more than four or eight) of general-purpose cores, and/or possibly an order of magnitude more special-purpose cores, quite likely complemented by new and/or different paradigms for on-chip communication and memory organization than the processors that are now on the market. These developments pose major challenges to architecture, language and compiler design, algorithms, and application developments, in order to fully (or acceptably) exploit the raw, provided compute power. The HPPC workshop aims to be a forum for discussion of such fundamental issues. It is open to all aspects of existing and emerging, envisaged and imagined multi-core (by which is meant: many-core) chips with a *significant amount of parallelism*, especially to considerations on novel paradigms and models and the related architectural and linguistic support. To be able to relate to the parallel processing community at large, which we consider essential, the workshop is organized in conjunction with Euro-Par, the main European (but international) conference on all aspects of parallel processing.

For HPPC 2008, the second installment of the workshop, 6 papers were selected for presentation and subsequent publication out of the 20 submissions received in response to the call for papers that was launched early in 2008. The submitted papers were all relevant to the workshop themes, some more than others, and due to the limited time for the workshop (an extended half-day event), only about 30% of the submissions could be accepted. The workshop organizers thank all contributing authors, and hope that they will also find it worthwhile to submit contributions next year. All contributions received *four* reviews by members of the Program Committee, who are likewise all thanked for the time and expertise they put into the reviewing work, and for getting it done within the rather strict time limit. The final decision on acceptance was made by the Program Chairs based on the recommendations from the Program Committee.

The Euro-Par 2008 workshop day was lively and well-organized, and the HPPC workshop had a cumulative attendance of more than 40. In addition to the six contributed talks, the workshop had two longer, invited talks by Gianfranco

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Bilardi (on "Models for Parallel and Hierarchical On-Chip Computation") and Chris Jesshope (on "Building a Concurrency and Resource Allocation Model into a Processor's ISA"). The HPPC 2008 workshop organizers thank all attendees, who contributed much to the workshop with questions, comments and discussion, and hope they found something of interest in the workshop, too. We also thank the Euro-Par organization for creating the opportunity to arrange the HPPC workshop in conjunction with the Euro-Par conference, and of course all Euro-Par 2008 organizers for their help and (excellent) support both before and during the workshop. Our sponsors VTT, NEC Laboratories Europe and Euro-Par 2008 are warmly thanked for the financial support that made it possible to invite Gianfranco Bilardi and Chris Jesshope, both of whom we sincerely thank for accepting our invitation to speak and for their excellent talks.

These proceedings include the final versions of the presented HPPC papers (as a matter of principle, accepted papers not presented at the workshop are not included in the proceedings), taking the feedback from reviewers and workshop audience into account. In addition to the reviews by the Program Committee prior to selection, an extra, post-workshop (blind) "*reading*" of each presented paper by one of the other presenters was introduced with the aim of getting fresh, uninhibited high-level feedback for the authors to use at their discretion in preparing their final version (no papers would have been rejected at this stage – bar major flaws). This idea will be continued for HPPC 2009.

The contributed papers are printed in the order they were presented at the workshop. The abstracts of the two invited talks by Gianfranco Bilardi and Chris Jesshope have also been included in the proceedings. Thematically the contributed papers cover aspects of language and algorithms support for an actual, well-known, heterogeneous multi-core processor ("Optimized Pipelined Parallel Merge Sort on the the Cell BE" by Keller and Kessler, and "Compile-Time and Run-Time Issues in an Auto-parallelization System for the Cell BE Processor" by Donaldson, Keir and Lokhmotov), general, run-time support for heterogeneous multi-cores ("A Unified Runtime System for Heterogeneous Multi-core Architectures" by Augonnet and Namyst), improvements of software implementations of the transactional memory programming model ("Adaptive Read Validation in Time-Based Software Transactional Memory" by Atoofian, Baniasadi and Coady), high-level, general-purpose, programming support tools ("Towards an Intelligent Environment for Programming Multi-core Computing Systems" by Pllana et al.), as well as considerations on power-constrained limits to scaling of multi-cores ("(When) Will CMPs Hit the Power Wall?" by Meenderinck and Juurlink). The last mentioned paper, very much aligned with the premise of the HPPC workshop, conjectures chip-multiprocessors with 999 cores by 2022.

The HPPC workshop is planned to be organized again in conjunction with Euro-Par 2009.

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