

HPPC 2007: Workshop on Highly Parallel Processing on a Chip (Foreword)

Technological developments are bringing parallel computing back into the limelight after some years of absence from the stage of mainstream computing and computer science between the early 1990 and early 2000s. The driving forces behind this return are mainly technological: increasing transistor densities along with hot chips, leaky transistors, and slow wires – coupled with the infeasibility of extracting significantly more ILP at execution time – make it unlikely that the increase in single processor performance can continue the exponential growth that has been sustained over the last 30 years. To satisfy the needs for application performance, major processor manufacturers are instead counting on doubling the number of processor cores per chip every second year, in accordance with the original formulation of Moore’s law. We are therefore on the brink of entering a new era of highly parallel processing on a chip. However, many fundamental unresolved hardware and software issues remain that may make the transition slower and more painful than is optimistically expected from many sides. Among the most important issues are convergence on an abstract architecture, programming model, and language to easily and efficiently realize the performance potential inherent in the technological developments.

The *Workshop on Highly Parallel Processing on a Chip* (HPPC) aims to be a forum for discussing such fundamental issues. It is open to all aspects of existing and emerging/envisaged multi-core (by which is meant: many-core) processors with a *significant amount of parallelism*, especially to considerations on novel paradigms and models and the related architectural and linguistic support. To be able to relate to the parallel processing community at large, which we consider essential, the workshop has been organized in conjunction with EuroPar, the main European (but international) conference on all aspects of parallel processing.

The call for papers for the HPPC workshop was launched early in the year 2007, and by the submission deadline we had received 20 submissions, which were of good quality and generally relevant to the theme of the workshop. The papers were swiftly and expertly reviewed by the Program Committee, most of them receiving four qualified reviews. The Program Chairs thank the Program Committee for the time and expertise they put into the reviewing work, and for getting it all done within the rather strict time limit. A final decision on acceptance was made by the Program Chairs based on the recommendations from the Program Committee. Being a(n extended) half-day event, there was room for accepting only six of the contributions, resulting in an acceptance ratio of about 30%. Five of the six accepted contributions were presented at the workshop (the paper not presented is as a matter of principle not included in these proceedings), together with two forward-looking invited talks by Uzi

Vishkin and Thomas Sterling on realizing a PRAM-on-a-chip vision and societies of cores and their computing culture.

These post-workshop proceedings include the final versions of the presented HPPC papers, taking the feedback from reviewers and workshop audience into account. In addition, the extended abstracts of the two invited talks by Uzi Vishkin and Thomas Sterling have also been included in the proceedings.

The Program Chairs sincerely thank the Euro-Par organization for providing the opportunity to arrange the HPPC workshop in conjunction with the Euro-Par 2007 conference. We also warmly thank our sponsors VTT and Euro-Par for financial support, which made it possible to invite Uzi Vishkin and Thomas Sterling, both of whom we also sincerely thank for accepting our invitation to come and speak. Finally, we thank all attendees at the workshop, who contributed to a lively day, and hope they too found something of interest in the workshop. Based on the mostly positive feedback, the Program Chairs and organizers plan to continue the HPPC workshop in conjunction with Euro-Par 2008.

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