A Framework for Hardware-in-the-Loop Testing of an Integrated Architecture

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Abstract. In this paper we present a distributed Hardware-in-the-Loop (HiL) simulation approach that supports the verification and validation activities in an integrated architecture as recently developed in DECOS (Dependable Embedded COmponents and Systems), an integrated project within the Sixth Framework Programme of the European Commission. Focusing on the interconnection between the simulated environment and the Integrated System Under Test (ISUT), our approach involves the concept of a Smart Virtual Transducer (SVT) that replaces the physical transducers of the ISUT without a probe effect on the ISUT. Our approach enables a complexity reduction for setting up an HiL simulation and supports a well-designed scalable interface to an integrated architecture. Furthermore, we support non-intrusive, deterministic interaction between the environment simulation system and the ISUT in order to guarantee reproducible test-runs. We show an exemplary application of the proposed concept by tailoring the generic components of the proposed simulation approach to an automotive park assistant system.

1 Introduction

The increasing number of electronic functions in future automobiles requires a change from the traditional "one function – one Electronic Control Unit (ECU)" concept to integrated architectures that support bundling several functions in one ECU. Such an *integrated system architecture* must provide means to handle the complexity of distributed applications while supporting efficient integration of functions into the shared hardware.

An example for an integrated system architecture is the DECOS Integrated Architecture [1], which builds upon the validated architectural services of a time-triggered core architecture. A distributed time-triggered computer system provides a physical network as a shared resource for the communication activities of more than one application subsystem. Other integrated architectures are AUTOSAR [2] and IMA [3].

Integrated architectures pose also a challenge to the HiL test procedure, a standard method for testing of an embedded controller before its deployment [4].

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HiL simulation is a technique where parts of a real system are replaced by a simulation, i. e., a mathematical model of these real system parts [5]. HiL simulation offers increased realism of the simulation because access to hardware features is provided that would not be available in a pure software simulation. In an integrated system, applying the HiL test procedure requires finding adequate interfaces between the simulator and the ISUT.

In this paper we present a distributed HiL simulation approach for the DECOS Integrated Architecture. The interaction between the simulated environment and the ISUT involves the concept of an SVT [6] that replaces the physical transducers of the ISUT without a probe effect on the ISUT. Thus, an ISUT as part of an integrated architecture can be connected to the HiL simulator in a non-intrusive way. Each SVT communicates with other components of a distributed environment simulator via a standardized time-triggered digital interface. Furthermore, an SVT emulates a transducer-specific interface. The proposed concept enables a complexity reduction for setting up a HiL simulation and supports a well-designed scalable interface to an integrated architecture.

The rest of the paper is structured as follows: Section 2 reviews related work in the area of HiL simulation. Section 3 describes structure and features of the integrated system architecture that is used in our approach. Section 4 elaborates on the architecture of the environmental simulation system and discusses the implications on reproducibility of simulation results. We present a case study based on an exemplary prototype application in Section 5. The paper is concluded in Section 6.

2 Related Work

HiL simulation involves physical hardware components, i. e., nodes, of a real-time system. Hence, HiL simulation requires the construction of an environment simulator in order to emulate the environment of these nodes [7]. In case only a subset of nodes of a distributed real-time system exists, non-existing nodes must be simulated by a cluster simulator as discussed in [8,9,10].

HiL simulators are constructed for a wide range of different applications. For instance in [11], real-time HiL simulation of vehicle and mobile robots is proposed to avoid extensive formal analysis of these systems. In the traffic control domain, system integrators are confronted with frequent changes of signal timing plans implemented in traffic controllers. These signal timing plans are provided by sub-suppliers as closed Intellectual Property (IP) software modules. Hence, HiL simulation is proposed in order to fine-tune these signal timing plans while at the same time protecting the IP of the individual sub-suppliers [12].

Commercially available HiL simulation systems range from simple simulators that target at testing a single ECU to complex simulators that are capable of testing large distributed real-time systems. *DSP Builder* [13] by Altera[1] and *Tanto2 Test* by Hitex[2] are examples for simple HiL simulators, where a single

[1] http://www.altera.com
[2] http://www.hitex.de

hardware target (i. e., an FPGA, or a single ECU) is directly connected to a development PC that executes an environment simulation.

Several vendors offer solutions for more complex HiL simulators. Regarding such complex HiL simulators, we can basically distinguish between monolithic and distributed HiL simulators.

A modular, component-based, monolithic HiL simulator, uses a single device that is configured to offer all required interfaces for a particular SUT. Monolitic HiL simulators are offered for instance by dSpace[3] (*Simulator Mid-Size, Simulator Full-Size*), The Mathworks[4] (*xPC Target*[14]), National Instruments[5] (*LabVIEW*), and Pi Technology[6] (*Pi Autosim*). These simulator products can be equipped with a range of modular I/O boards and processor boards in order to be tailored to a particular HiL simulation system. I/O hardware solutions include analog and digital I/O, CAN, PWM, dynamic signals, motion control, image acquisition as well as FPGA modules.

In contrast to a monolitic HiL simulator, a distributed HiL simulator consists of several interacting nodes that are capable of executing a distributed simulation model. Each of these nodes can be equipped with application-specific I/O hardware. Distributed HiL simulators are provided by Applied Dynamics International (ADI)[7] (*ADI rtX simulator*), Opal-RT[8] (*RT-LAB*), and RTDS Technologies[9] (*RTDS Simulator*). These distributed simulators interact either by the exchange of data that is visible at the interfaces of the SUT (*emulated electronic interfaces*), or by the exchange of data that is part of the simulation model and that is not visible at the SUT's interfaces (*virtual interfaces*) [15]. Communication via the virtual interfaces, i. e., interaction between different nodes of a distributed simulator is either realized by the implementation of an event-triggered protocol (e. g., Ethernet, SCRAMNet, FireWire, or INFINIBAND) or by a common communication backplane as for the RTDS Simulator, that links all processing nodes in parallel.

Although all HiL simulators are designed for real-time execution of a simulation model, the existing solutions lack a scalable approach for deterministic interaction between HiL simulator components. Moreover, none of the existing solutions target at HiL simulation in an integrated architecture.

3 Integrated System

Many large applications (e. g., in the automotive or aerospace domain) consist of a number of nearly independent application systems. We call such an application subsystem a Distributed Application Subsystem (DAS). A DAS provides a major part of the overall application and is composed of smaller functional elements

[3] http://www.dspace.com
[4] http://www.mathworks.com
[5] http://www.ni.com
[6] http://www.pitechnology.com
[7] http://www.adi.com
[8] http://www.opal-rt.com
[9] http://www.rtds.com

called *jobs*. In the automotive domain, the powertrain subsystem, the comfort subsystem, and the multimedia subsystem are examples for DASs. Examples of DASs in a present-day avionic application are the cabin pressurization system, the fly-by-wire system, and the in-flight entertainment system.

The proposed framework for HiL simulation is designed for integrated architectures, i. e., a single distributed computer system serves as the execution platform for multiple DASs. Each node computer of the distributed computer system contains jobs of one or more DASs (cf. Figure 1). Likewise, the communication network that interconnects the node computers serves the transport of messages between jobs of more than one DAS.

In the following, we will discuss the structural elements of the DECOS architecture (i. e., network, nodes, environment), because this system architecture will be used for the construction of the framework for HiL simulation.

3.1 Communication Network

The communication network of the integrated architecture executes a time-triggered protocol (e. g., TTP [16], FlexRay [17]). The rationale behind choosing a time-triggered communication protocol is the suitability for ultra-dependable systems [18]. Time-triggered communication protocols are characterized by a guaranteed message transport with low jitter, error containment between node computers, and a fault-tolerant distributed global clock service.

3.2 Node Computers

A node computer provides an execution environment for multiple collocated jobs of one or more DASs as shown in Figure 1. Each job implements a part of the

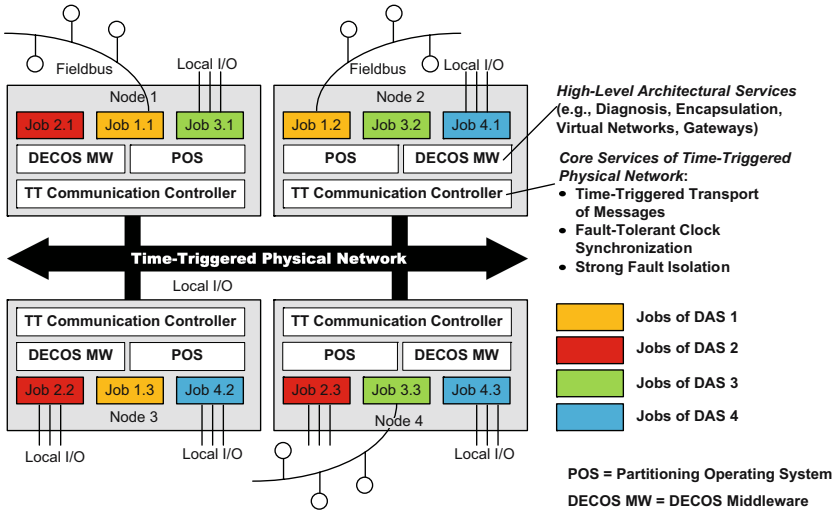

Fig. 1. Distributed System in the DECOS System Architecture

application functionality and is within the responsibility of a single organizational entity (e. g., a specific supplier).

The allocation of computational resources (e. g., memory, CPU time) to jobs occurs using a partitioning operating system with support for fault isolation and modular certification [19,20]. The partitioning operating system implements mechanisms for spatial and temporal partitioning in order to encapsulate the individual jobs. The scheduling of jobs needs to ensure that a timing failure of a job, such as a worst-case execution time violation, does not affect the CPU time available to other jobs. In analogy, the spatial partitioning mechanisms of the partitioning operating system enforce memory protection between jobs (e. g., with a memory management unit).

The interaction with other jobs occurs through the services provided by the DECOS middleware. The DECOS middleware offers high-level architectural services, which serve as a baseline for the development of applications. These services constitute the interface for the jobs to the underlying platform. Among the high-level services are gateway services, virtual network services, encapsulation services, and error detection services. On top of the time-triggered physical network, different kinds of virtual networks are established and each type of virtual network can exhibit multiple instantiations. Gateway services selectively redirect messages between virtual networks and resolve differences with respect to operational properties and naming. The encapsulation services control the visibility of exchanged messages and ensure spatial and temporal partitioning for virtual networks in order to obtain error containment.

Below the DECOS middleware, each node computer in Figure 1 contains the communication controller. The communication controller executes a time-triggered communication protocol as required for accessing the network. It provides so-called core architectural services (i. e., time-triggered transport of messages, fault-tolerant clock synchronization, strong fault isolation), which are used as the basis for the implementation of the high-level architectural services in the DECOS middleware.

The rationale for distinguishing between core architectural services and high-level architectural services is the ability to exploit existing time-triggered communication protocols for the construction of an integrated architecture. For example, it has been demonstrated by formal analysis [21] and experiments [22] that the Time-Triggered Protocol (TTP) is appropriate for the implementation of applications in the highest criticality class in the aerospace domain according to RTCA DO-178 B Level A.

3.3 Input/Output

In order to perform integration tests that involve the interaction between a given distributed computer system and its environment, the framework needs to simulate the physical surroundings of the computer system, i. e., the controlled object(s) and the operator. In a real-world system, the interaction between the computer system and the environment occurs via transducers, i. e., sensors and actuators. These transducers can either be connected directly or interfaced via

a fieldbus. The latter approach simplifies the installation from a logical and a physical point of view and is extendable but might introduce higher cost and increased latency of sensory information and actuator control values.

4 Environmental Simulation

4.1 Simulator Architecture

HiL simulation of an ISUT involves a simulation of the environment of this ISUT by means of an environment simulator. The environment simulator is linked to the ISUT via the ISUTs Controlled Object Interface (COI) [23] which can either be a standardized digital transducer interface or an arbitrary transducer-specific interface (e. g., an analog interface).

In the following we introduce a development approach with generic components that can be tailored to establish the coupling between an HiL simulator and a specific ISUT. Hence, we separate between those components that emulate the COI, e. g., via a 4-15mA interface, a fieldbus, or direct I/O, and those components that are used to execute part of a distributed simulation model but do not directly interact with the ISUT.

Following this separation, our HiL simulation framework involves a distributed environment simulator consisting of a set of *Frontend Simulation Components (FSCs)* that control the physical interaction between the environment simulation and the ISUT, as well as a set of *Backend Simulation Components (BSCs)* that are used to execute (part of) the environment simulation model. Additionally, a time-sync master component is employed in the HiL simulation framework. The time-sync master component is part of the environment simulator, i. e., it triggers the individual FSCs and BSCs according to a pre-defined schedule. Furthermore, the time-sync master is a (passive) member of the ISUT, i. e., it

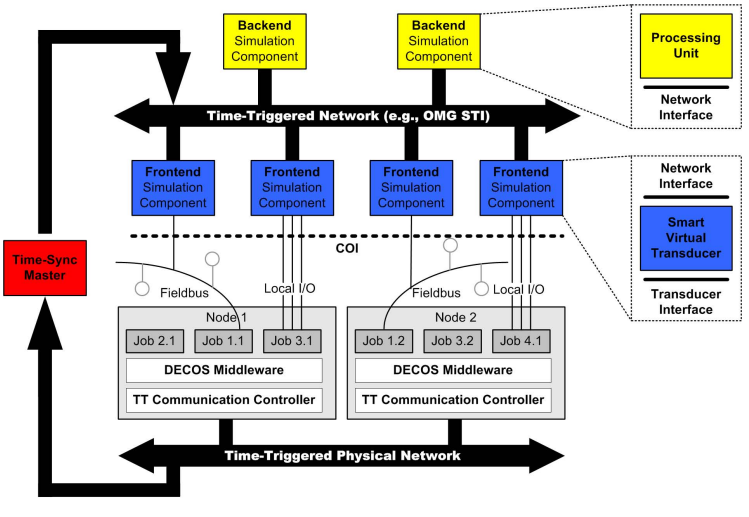

Fig. 2. HiL Simulation with an Integrated System

synchronizes its time-base with the time-base of the ISUT. Hence, the time-sync master establishes synchronism between the ISUT and the environment simulator without a probe effect with respect to the ISUTs execution.

As depicted in figure 2, the interaction of nodes of an ISUT with their environment is realized via an arbitrary transducer interface including value/time-depen dent analog and/or digital direct I/O as well as standardized fieldbus interfaces. An FSC connects to nodes of the integrated system for the purpose of interacting with these nodes via a particular transducer interface. FSCs and BSCs collectively execute the distributed simulation model of the environment of the ISUT.

An FSC requires updates of simulation values that are provided by one or several BSCs. Based on these simulation values, the FSC determines the I/O signal that is to be provided to the ISUT. Both the control logic that calculates the required I/O signal based on the simulation values and the physical wiring are part of the FSC. Thus, a change in the interface specification of the ISUT directly affects the FSC, but not necessarily the BSC as long as the FSCs can be provided with simulation values in time.

The availability of separate FSCs in an HiL simulation is particularly advantageous when it comes to incremental testing of an integrated system. Starting with a single node, a stepwise inclusion of jobs of the integrated system in the HiL simulation is required. At each step, the environment model of the real-time system is simulated (by BSCs) and the coupling between this simulation and the actual ISUT is established with FSCs. With separate FSCs it is possible to scale the HiL simulation from a small ISUT (e. g., a single node with only one job) up to a complete integrated system by adding additional FSCs as required.

FSCs of the environment simulator are realized by SVTs (cf. Figure 3). An SVT implements two interfaces – a standardized digital interface to a time-triggered transducer network (e. g., the Smart Transducer Interface of the Object Management Group [24]) and a transducer-specific interface. The digital interface is used to interact with the BSCs and with other SVTs (i. e., FSCs). The transducer-specific interface resembles the interface of a sensor or actuator element for coupling the SVT with direct I/O of the ISUT. Furthermore, an SVT can implement a certain fieldbus interface. In that case, the SVT would act as a gateway between the environment simulator and a fieldbus of the ISUT.

An SVT consists of a processor core, memory, a UART, as well as the digital and analog I/O necessary to emulate a specific transducer of the ISUT. The

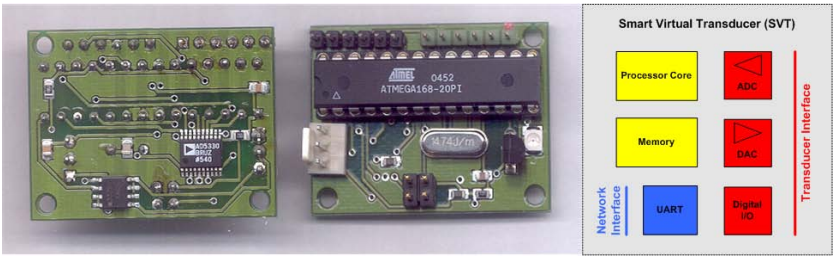

Fig. 3. Smart Virtual Transducer (SVT)

prototype given in figure 3 includes an Atmel ATMega168 microcontroller and an Analog Devices 8-Bit DA converter (AD5330).

4.2 Reproducibility of Simulation Results

Deterministic interaction between the environment simulator (i. e., network of FSCs and BSCs) and the respective ISUT is important in order to guarantee reproducible results of an HiL simulation run. Thereby, deterministic interaction relates to the functional (i. e., message value or signal size) and the temporal domain (i. e., instant of interaction).

In order to achieve reproducible results in our proposed architecture, the following requirements have to be fulfilled:

1. The HiL simulator must share a common time base with the ISUT and have *a priori* knowledge about the time when a sensor is read or an actuator is set by the ISUT.
2. The values exchanged across interfaces between HiL simulator and ISUT must be deterministic.
3. The ISUT and the HiL simulator may not exhibit intrinsic sources of indeterminism, e. g., by suffering from race conditions.

The proposed architecture can satisfy the first requirement by sharing its existing global timebase with the HiL simulator. Furthermore, the DECOS architecture supports a time-triggered action model the allows the prediction of the instants of accessing a sensor's or actuator's value.

The second requirement depends on the employed interfaces. While the digitalization of a pure analog value, e. g., by an ADC, always constitutes a possible source of indeterminism, a DAC – ADC system may behave deterministically, when (i) there is no sampling while the current value is changing to a new one and (ii) each value generated by the DAC can be interpreted by the ADC in a non-ambiguous way. (i) is already solved by the synchronization mechanisms and the temporal determinism of our architecture while (ii) in general requires a careful design of the analog path. For sensor types with only few detection results, e. g., a binary on/off detector, (ii) can be easily fulfilled.

Regarding the HiL simulator, we can establish deterministic behavior due to the usage of a time-triggered communication and execution scheme. Deterministic construction of the ISUT lies outside the sphere of control of the HiL simulator and requires a deterministic architecture. Our proposed case study builds on a time-triggered architecture that avoids sources of indeterminism by design and thus fully satisfies the third requirement.

5 Case Study

5.1 Exemplary Application Using the Integrated Architecture

The case study used to exemplify the HiL simulation environment includes two automotive DASs (which are part of a larger automotive electronic system):

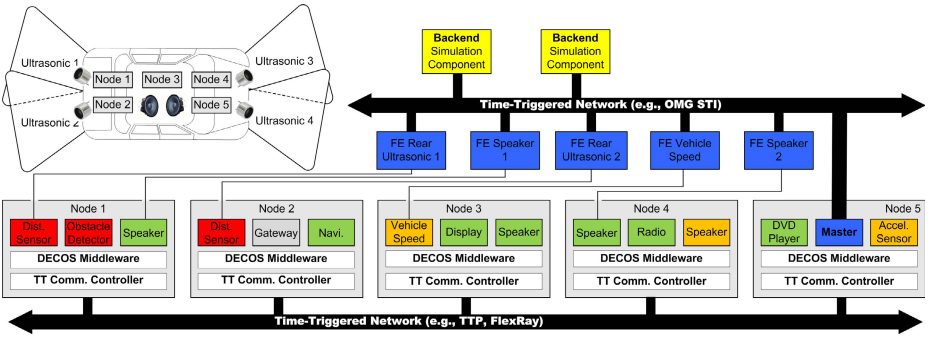

Fig. 4. Exemplary Integrated System with Environmental Simulation

– **Multimedia DAS.** Today's luxury cars contain multimedia functionality such as DVD players, high-end audio systems, and GPS navigation systems. In addition, voice control and hands-free speaker phones relieve the driver of concentrating on multimedia devices instead of traffic.
– **Park assist DAS.** This DAS implements a parking aid with ultra-sonic sensors. In case a threshold for a minimum distance is exceeded, the DAS produces an acoustic alarm signal. Therefore, the park assist DAS encompasses four jobs reading inputs from ultra-sonic distance sensors. In addition, the DAS contains an obstacle detector job, which reads the distance measurements from the four other jobs and determines whether an alarm signal should be produced. In this case, the acoustic alarm signal is transferred via a gateway to the speaker jobs of the multimedia DAS.

Figure 4 depicts a possible realization of these DASs using the DECOS architecture. Each node computer hosts multiple jobs, which can belong to different DASs (such as the multimedia or park assist DAS).

5.2 Exemplary Environmental Simulation

In the scope of the case study we exemplarily focused on two kinds of transducers, namely ultra-sonic sensors for distance measurement of the park assist DAS and loudspeakers of the multimedia DAS. Hence, the interaction between the environment simulation and the integrated system (i. e., the ISUT) across the COI involves SVTs that emulate the behavior of an ultra-sonic sensor as well as SVTs that capture and process the signals provided by the audio system jobs of the ISUT.

As depicted in figure 4, the setup of the environment simulation system additionally involves an FSC that receives the actual vehicle speed from the ISUT (i. e., *FE vehicle speed*) and a master node that controls the operation of the involved SVTs (i. e., *Master*) and that synchronizes the time-base of the environment simulation to the time-base of the ISUT.

Within the prototypical realization of the environment simulation system, we use TTP/A [25] to interconnect the deployed SVTs. The time-triggered field-

bus protocol TTP/A is an implementation of the OMG ST interface standard, including the time-triggered transport service. TTP/A is a round-based master slave protocol where multiple nodes of a TTP/A cluster arbitrate a shared bus according to a *time division multiple access (TDMA)* scheme.

In the current implementation we prototypically realized an SVT with a simplified interaction pattern that consists of digital samples for acoustic pressure. This SVT can be used to emulate a loudspeaker of the multimedia DAS. For the ultra-sonic sensors we realized SVTs that emulate a Polaroid 6500 series sonar ranging transducer [26].

6 Conclusion

In this paper we outlined a distributed HiL simulator that consists of FSCs and BSCs that are interlinked by a standardized digital transducer interface, e. g., the OMG STI. For the realization of the FSCs we propose to use SVTs that replace the physical transducers of the ISUT.

Besides showing an exemplary application of the proposed concept in the automotive domain, we discussed the prerequisites to achieve reproducible results in our proposed architecture.

Our approach supports the verification and validation activities in an integrated architecture, e. g., DECOS, IMA, AUTOSAR and supports deterministic interaction between an HiL simulator and an ISUT in order to guarantee reproducible test results. Moreover, this approach offers the possibility to test an integrated system at the physical interface. Hence, it is possible to perform non-intrusive (black box) tests which is particularly important for an integrated system where different vendors provide closed IP software or hardware/software components.

Acknowledgments

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