Automatic Problem Understanding
from Circuit Schematics

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Abstract. This paper presents an algorithm for understanding problems from circuit schematics in exercise problems in physics at secondary school. This paper models the problem understanding as a problem of extracting a set of relations that can be used to solve problems with enough information. The challenges lie in not only analyzing the circuit schematics but also extracting the proper relations for a given exercise problem. To face these challenges a novel approach is proposed to detect circuit nodes with their current flows to extract the current equations for nodes. And the other novel approach is proposed to extract voltage equations of independent loops. The proposed approach was tested with a dataset collected from the text books and the exam papers for the students at secondary schools. Experimental results show that the effect of recognition and analysis we designed delivers promising result, and our approach can be adapted to more complex electrical circuit analysis.

Keywords: Circuit schematic · Symbols recognition · Problem understanding
Extract equations

1 Introduction

The analysis and understanding of circuit schematic is the necessary way to solve circuit problems for secondary school students, but it is a challenge for machine to not only analyze the circuit schematics but also extract the proper relations for a given circuit problem. To face this challenge, this paper proposes to extract enough information for problem understanding by using circuit schematic diagram analysis. In general, a circuit problem is provided as a text in natural language together with circuit schematic, and a correct answer must be provided, typically in the form of an answering list with circuit equations, reasoning processes and answers. Equations are often extracted from the analysis of circuit schematic, such as voltage and current relationship (shorted for VCR) is extracted from the identification of resistance components, node current equations can be obtained by analyzing nodes together with their current flows and so on.

The task of circuit schematic analysis has received growing interest in recent years [1, 2]. One of the more interesting phenomenon of this research is that it combines visual question answering, web-based learning and intelligent tutoring system [4–6]. Symbolic analysis of linear circuit networks is the backbone of the design of electronic and systems [3]. The main task of this method is to obtain several algebraic expressions for corresponding specified circuit network functions. What's more, for the correctness of algebraic expressions, the validation method of symbolic expressions using both sets of control variables simultaneously was presented in [1]. However, this method is useful for linear networks, but for more complex networks (i.e., complicated circuit) it needs further optimization. Web-based approach [4] is another type of circuit analysis method that it stored a set of previously derived expressions into a database, and when an input is coming, the method will compare it with stored expressions. Whereas if the input is creative or unusual that several different solution paths could be exist, then obtaining a set of required equations from the database is a time-consuming work.

Another approach is based upon the introduction of a set of new variables (symbols) [5, 6]. By introducing appropriate nodes and loops, either a set of node voltages or a suitable set of loop currents can be used for forming Kirchhoff's voltage laws equations or Kirchhoff's current laws equations. But one of the challenge is that how to get the appropriate circuit nodes with the directions of current flows all around themselves automatically by machine, such as the node 1 and its current flows (I_2, I_4, I_5) in Fig. 1(a), and the other challenge is how to obtain independent loops, such as m1, m2 and m3 in Fig. 1(a).
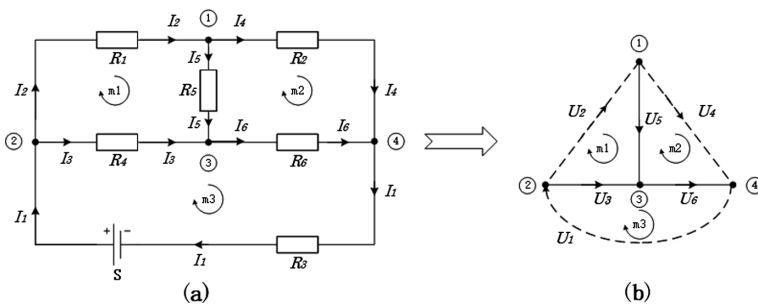

Fig. 1. Circuit schematic example

In this paper, a novel approach is presented to extract symbolic equations automatically by detecting circuit elements (i.e., components, nodes). The recognition of circuit elements by machine is the basic work for our approach. In order to detect the nodes with their current flows, the algorithm of node detection, LSD [10, 13] and the method of connectivity traversal will be orderly used. In the respect of extracting voltage equations of independent loops, a novel approach of simplifying the system of whole loop voltage's homogeneous linear equations is proposed. It is then show how this can be achieved to cover all circuit schematic and forming circuit equations corresponding to the physical quantities.

The remaining sections of this paper are organized as follows. In the following section, the analytical approach for circuit schematic is explained in detail. Section 3 deals with the elements recognition of circuit schematic by using image processing methods. In Sect. 4, detailed understanding procedure of circuit schematic is demonstrated with an auto-identifying algorithm. In Sect. 5, results of an actual test experiments are shown and discussed. Finally, in Sect. 6, conclusions are presented.

2 Analytical Approach of Circuit Schematic

The analytical approach focus on the recognition and analysis of circuit schematic. The section of circuit schematic recognition is to identify the elements of circuit schematic (i.e., components, nodes and so on), and the circuit schematic analysis section is used to obtain equations by analyzing two types of constraints (i.e., topology constraint and component constraint). The answers of circuit schematic problem are quantified by solving two kinds of simultaneous equations.

2.1 The Recognition of Circuit Elements

As soon as the circuit schematic is loaded into the system, three kings of fundamental recognition for circuit elements will be executed through a series of circuit schematic recognition algorithms: the tesseract OCR engine [12] is used to locate and recognize the characters and numbers of circuit labels, the approach of SVM [7, 11] is used to recognize circuit components, the approach of improved line segment detector (short for LSD) algorithm and nodes detection algorithm are used to obtain circuit nodes with their current flows. Then, a set of circuit labels, components (i.e., resistor, light, ammeter, voltmeter and so on) and nodes are identified. For each element symbol, the required properties are stored in a table.

2.2 Two Kinds of Constraints

The running state of circuit is determined by the components of circuit and the interconnection of each component. To summarize the analysis content of circuit schematic, two types of constraints should be understood clearly.

Component Constraint
Component constraint is determined by the nature of circuit elements, i.e. resistance, capacitor, inductance and power supply, so getting the properties of these four elements is the basis of circuit analysis. Besides, voltmeter and ammeter are tools for auxiliary measurement, and some appliances are the deformation of circuit elements, such as the light bulb is a resistive load. As is known to all, current, voltage and power are the basic quantities of physics analysis, however, power is the product of voltage and current. So, the essential thing for the single circuit element is to master the voltage and current relationship (short for VCR). With component constraint, VCR equations will be obtained by Ohm's law or other variant of Ohm's law.

Topology Constraint

Topology constraint is determined by the structure of circuit schematic and Kirchhoff's law is used to analyze the operation law of electricity in the circuit structure. Kirchhoff's current law (short for KCL) implies that: The algebraic sum of currents in a network of conductors meeting at a point is zero. Recalling that current is a signed (positive or negative) quantity reflecting direction towards or away from a node, this principle can be stated as: $\sum_{k=1}^{n} I_k = 0$.

Here, n is the total number of branches with currents flowing towards or away from the node. For example, the circuit node 1 and its current flows (I_2, I_4, I_5) is shown in Fig. 1(a), and the equation $I_2 - I_4 - I_5 = 0$ will be written by KCL.

Kirchhoff's voltage law (short for KVL) implies that: The directed sum of the electrical potential differences (voltage) around any closed network is zero, and it can be described as: $\sum_{k=1}^{n} V_k = 0$.

Here, n is the total number of voltages measured. For example, the circuit loop (mesh) m1 and its specified direction is shown in Fig. 1(b), and the equation $U_2 + U_5 - U_3 = 0$ will be written by KVL.

By analyzing topology constraint, two sets of equations will be obtained by KCL and KVL.

2.3   The Procedure of Analysis for Circuit Schematic

In general, the behavior of a circuit network is often governed by three sets of equations: VCR equations, KCL equations and KVL equations. Because of the topology constraint of KCL and KVL is adopted in the analysis of circuit nodes and loops, and the component constraint has been well embedded in the VCR theorems such as Ohm's law, so we only consider the circuit elements (i.e. Resistance and power supply), independent nodes and independent loops of a circuit schematic. The overall implementation procedure of analytical approach for circuit schematic are summarized as follows.

Procedure I: Analytical Approach of Circuit Schematic

Input: a physics problem text with corresponding circuit schematic.
Output: the recognition and analysis process for circuit schematic.
Step 1: circuit symbols recognition and screening of circuit components for VCR equations.
Step 2: circuit branch lines detection and circuit nodes detection.
Step 3: connectivity traversal based on circuit nodes to judge and set the reference directions of branch currents and detour directions of independent loops.
Step 4: independent nodes detection and extract node current equations by KCL.
Step 5: independent loops detection and extract loop voltage equations by KVL.

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3   Circuit Schematic Recognition

3.1   The Recognition of Circuit Components

Circuit components are the basic elements of circuit schematic, whose properties contain more information on circuit understanding (i.e., current, voltage or VCR information). The goal of the detection algorithm is to recognize the components and line-linking in a circuit schematic. In particular, this algorithm strives to obtain VCR equations by analyzing circuit schematic in a digital document, which includes textual question stems and circuit schematics. Through the preprocessing, content representations (i.e., PDF images and circuit schematics) are rapidly extracted from a given digital document by using method [8, 14]. In addition, a segmentation process approach [15] is implemented to separate the textual and non-textual components in a diagram and circuit region is located by a convex bounding operation of non-text classes. In the framework, the textual and circuit schematic content of a document will be processed by our algorithms.

Circuit Labels Recognition

There are two kinds of circuit labels: the label outside the component (i.e., the label "R_1" and "S" in Fig. 1(a)) and the label inside the component (i.e., the label "A" of an ammeter) which is a part of the component. Initially, both circuit labels will be located and recognized by our method and the recognized labels inside the component is needed to populate back to the diagram.

First, the tesseract OCR engine [12] is adopted to locate and recognize the characters and numbers of circuit labels. Only clusters have a structure of "C", "Cn" and "Cnn" will be accepted as a valid label, in which "C" stands for character and "n" for number. Recording all the candidate labels and their locations in a table named T_{label}. Second, characters and number belonging to voltmeter, ammeter and motor are pushed back to the diagram, i.e. the character of "V" and "A" will be drawn back to diagram and they still in T_{label} as an accepted label. Besides, in order to avoid destroying the original image feature of circuit, we calculate a bounding rectangle for each of them and copy the pixel value of each rectangle from the source figure to the circuit schematic, instead of redrawing these characters.

Components Recognition

There are more than thirteen types of circuit components in physics at secondary school, and six most commonly used components are chosen as the target of recognition. What's more, a classification approach SVM was used to recognize the components of circuit schematic.

Component symbols segmentation is an important work that seriously affect the accuracy of recognition. In a circuit schematic, symbols are usually presented between two collinear segments. Based on this regularity, the gaps between two collinear segments are collected and the bounding rectangles G are calculated, and then removing blank rectangles in G which contain no symbols by contours analyzing. The process of symbols location and recognition are shown in Fig. 2.

Due to battery(s) symbol contains two or more separate connective component (i.e., Fig. 2(a)), a joint model is used for accurate battery symbols segmentation. In this
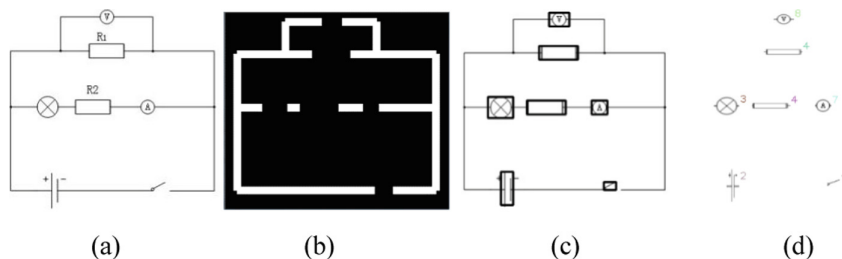
Fig. 2. Symbols location and recognition. (a) Input image (b) Overstriking mask of segment gaps (c) Bounding box on contours (d) Recognition results

model, we analyze the connectivity of each set of online segments and generate a default bounding box between two online segments. Then a combination operating is implemented on results of contour segmentation on gaps and all default boxes. The final segmentation results are shown in Fig. 2(c).

The corresponding sub-figure defined by box r in Fig. 2(c) is considered as a candidate circuit symbols and is resized to 32 * 32. Then the sub-figure is reshaped to a size of 1 * 1024 row vector which is used as the input of SVM classifier for training and prediction. A recognized sub-figure located by r is defined as a 3-element row vector *symbol* stored in a vector S:

$$symbol = (typeID, label, r)$$

Where, *label* is the corresponding label found in T_{label} according to the position correlation, *TypeID* denotes the symbol type obtained by SVM prediction. The final components recognition results are shown in Fig. 2(d).

3.2   Node Detection Algorithm of Circuit Schematic

According to KCL, choosing an arbitrary circuit node, the sum of currents flowing into the node is equal to the sum of currents flowing out of the node or equivalently, so the goal of this section is to detect the whole nodes of a circuit schematic. As soon as the circuit nodes are detected, a set of KCL equations for each nodes is obtained. In this subsection, we briefly describe the branch lines detection and nodes detection in a circuit schematic.

Branch Lines Detection
The main work in this section is to detect the short lines from circuit diagram. Symbols are connected by vertical and horizontal short lines, while some short lines are part of symbols. In reality, only connecting lines are remained by the approach of detection, which is based on LSD [10, 13]. Salient segments are removed and short segments are merged to amend the defects by a set of optimization processes.

There are three possible defects in the lines detected from a diagram by applying LSD algorithm: (1) a visually line segment may be detected as a series of unconnected parallel short ones, (2) a line in the figure is detected as some disconnected short

segments, (3) the start or end points of a sub-circuit and the turning points of two connective segments cannot be accurately detected. The following sub steps are used to amend the defects.

To solve these problems, a set of optimization processes is performed. For each segment, we first find out all co-line segments as a segment group, then remove those segments far away from others and finally merge the remained segments into a new longer one. The distance between endpoints of two different segments is used for segments grouping. For example, in stage of grouping, put seed segment l_{vi} selected from L_v into a new group G_{vi}, add all co-line segments l_{vj} into G_{vi} if $dist(l_{vi}, l_{vj}) < \tau_v$, and remove l_{vj} from L_v. Where, τ_v is a pre-specified distance tolerance, $dist(l_{vi}, l_{vj})$ is the Euler distance. In stage of short segments merging, pair (l_{vi}, l_{vj}) is replaced by a new segment l'_{vi} when $co(l_{vi}, l_{vj}) > \delta_v$, where $co(\ ,\ )$ is the overlapping ratio on Y axis of (l_{vi}, l_{vj}), δ_v is a pre-specified tolerance. Put l'_{vi} into L'_v. Same strategies are used to merge short segments in L_h into L'_h.

On phase of gap detection, adjacency collinear segments are merged, and gaps between two collinear segments are detected. The graph in the bounding area of each gap is probably a circuit component symbol. Pairs of parallel segments which are part of the resistor and the battery may also be detected in clusters L'_v and L'_h. These pairs are removed before the operation of segments merging and gap detecting.

Circuit Nodes Detection

In the circuit topology, fork nodes denote the starting and ending of a parallel connection. Degree analyzing is applied to identify fork nodes from all intersection nodes in this step. Before degree analyzing, circuit will be converted to a connected graph $G_{connected}$ by combination of the position of row symbols vector S and segments clusters L'_v and L'_h.

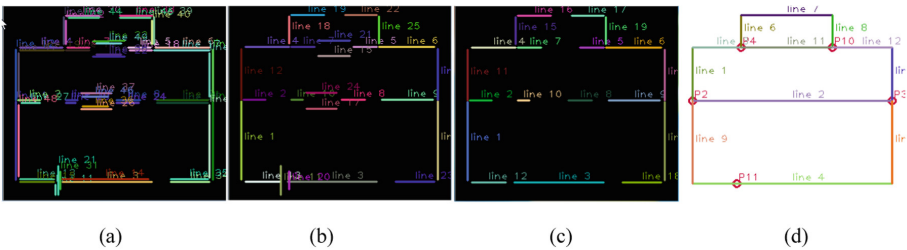(a)   (b)   (c)   (d)

Fig. 3. Branch lines and nodes detection. (a) Segments detection (b) Sallient segments removing (c) Resistor and power symbol location (d) Recognize circuit structure and fork nodes

Two types of intersection nodes, including turning node and fork node, exist in the circuit. Degree analyzing is implemented in this step to identify fork node. The degree of a node d is defined by the number of segments connected. For each intersection node $n_i (1 \leq i \leq N)$, count the numbers of adjacency segments $degree(n_i)$. If $degree(n_i) \geq 3$, then node n_i is marked as a fork node. The battery position in the diagram is treated as the start and end point of the circuit, which is marked a fork node n_0. The process of branch lines and nodes detection is shown in Fig. 3.

4 Circuit Schematic Analysis

After the segmentation and connection analyzing, symbols are recognized (Fig. 2(d)) and fork nodes are obtained (Fig. 3(d)). In this section, the extraction method of independent node current equations and independent loop voltage equations based on circuit schematic diagram analysis is proposed. Before the extraction, a node connection traversal algorithm is introduced to find the available paths among fork nodes and to get the directions such as current directions and voltage directions all around fork nodes.

4.1 Connectivity Traversal Based on Circuit Nodes

Connection traversal described in this section is a special kind traversal which uses depth first algorithm for traversing and searching a max length connective path in the connected graph $G_{connected}$ in the first main path searching phase followed by a shortest path traversal in the sub path searching phase. Before vertex traversing, the connective segments between two adjacency fork nodes are linked and marked as an edge of the circuit graph.

Different with traditional DFS in graph theory, not all nodes are visited in one traversal path and some special strategies are defined as follows:

Strategy 1. The main path start from n_0 and end with n_0.
Strategy 2. The main path contains the maximum number of fork nodes.
Strategy 3. No repeated nodes in main path.
Strategy 4. No repeated edges in main path.
Strategy 5. The beginning and end nodes of each sub path are from the main path or sub path traversed.

For each adjacency fork node pair (n_i, n_j), $0 \leq i \neq j \leq N$, the edge from n_i to n_j is marked as $s_i = \{l_p\}$, where l_p is the segments between n_i and n_j.

The algorithm begins with vertex n_0, it then iteratively transitions from the current vertex to an adjacent, unvisited vertex, until it can no longer find an unexplored vertex to transition to from its current location. Then, the algorithm backtracks along previously visited vertices, until it finds a vertex connected to yet more uncharted territory. It will then proceed down the new path as it had before, backtracking as it encounters dead-ends, and ending only when the algorithm has backtracked past the vertex n_0 from the very first step.

Then, a sub path m_{i+1} is defined as a shortest path walking along the unvisited edges between each pair of visited node in the path set $M = \{m_0, \cdots, m_i\}$. The searching starts from m_0, for each node n_k in m_0, find the shortest sub path starting with n_k and put it to M. Do searching process for each path in M until these is no new path can be found.

4.2 Independent Node Identification

A well-known fundamental set of independent loop currents may be obtained by considering an arbitrary spanning tree and linking in each of the remaining edges

(branches) of the circuit's graph [1]. If each circuit node is identified by a specific circuit symbol, any node current equations in the circuit schematic can be obtain by the topology constraint of KCL. This is a general method to form node current equations, but the problem is how to get independent nodes with their equations.
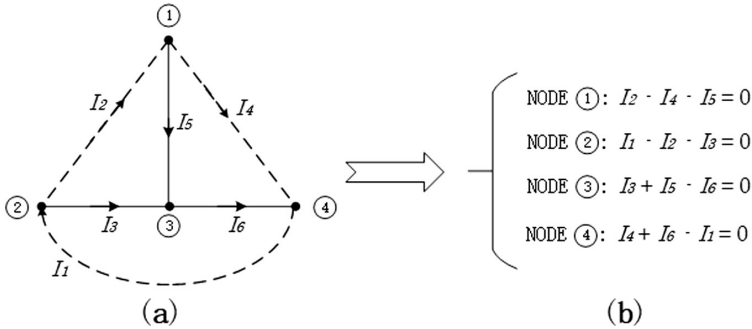

Fig. 4. Circuit nodes analysis

In order to clarify the analysis of circuit nodes, the simplified circuit schematic in Fig. 4 is used. The six branches describing the connection of the circuit are associated with four circuit nodes in Fig. 4(a). For the currents, a straightforward choice is to choose an arbitrary node as a reference and to analyze the current flows all around this node. Any node current equations in the network can be obtained by KCL as shown in Fig. 4(b). However, the four node current equations in the example are obviously linear dependent because of anyone equation can be derived by other three equations. In the process of solving, independent nodes or linear independent equations are required, so the method is simply remove any circuit node with its current equation.

4.3   Independent Circuit Loops Detection

For the voltages, an effective way is to find circuit loops that corresponding loop voltage equations can be written by KVL in topology constraint. In the process of connectivity traversal based on circuit nodes, the whole circuit loops can automatically be detected with voltage directions. Then, any different voltages in the circuit network will be involved by the relation of circuit loop voltages.

The proposed approach can be demonstrated through an example. The structure of circuit schematic Fig. 1(a) is shown in Fig. 5(a) and is asked to extract loop voltage equations. With connectivity traversal for circuit schematic, seven circuit loops were detected in Fig. 5(b). Corresponding to these loops, seven loop voltage equations can be obtained by KVL. It may prove to be more elegant to extract loop voltage equations, but some dependent loops were also extracted such as LOOP 6 contained LOOP 5 and LOOP 7 in Fig. 5(b). If linear dependent equations are present in equations group, the process of solving equations may drop into an endless loop. So a method of extracting independent loops by simplifying the system of homogeneous linear equations is proposed in Fig. 6.
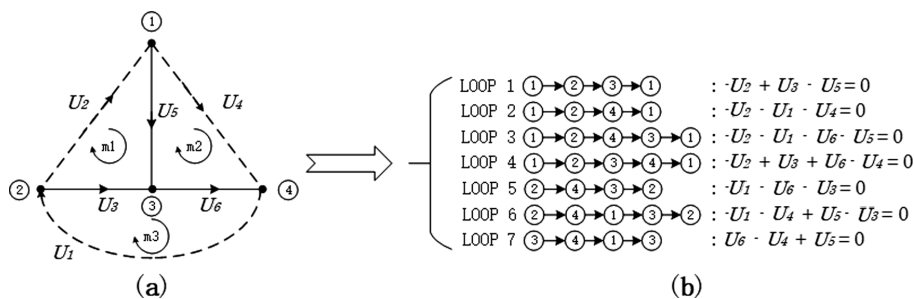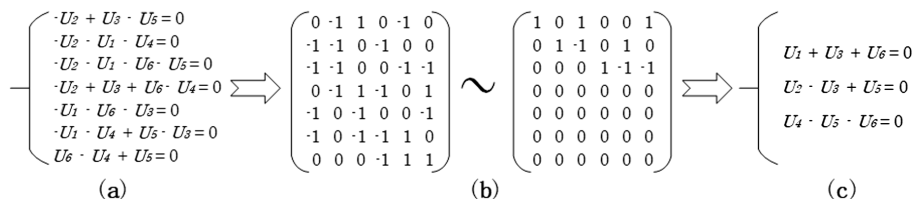
Fig. 5. Circuit loops analysis

Fig. 6. Independent circuit loops detection

A set of homogeneous linear equations is shown in Fig. 6(a), and the target is to extract independent loops such as m_1, m_2 and m_3 in Fig. 5(a). Our work is to extract the coefficients of the set of homogeneous linear equations that forming a coefficient matrix, and then simplifying the coefficient matrix to the simplest, which is shown in Fig. 6(b). Through simplification, the independent loops can be detected and the voltage equations of independent loops can also be written in Fig. 6(c).

5   Experiments

5.1   Experiment Setup

Dataset: The dataset contains 145 circuit schematics in physics at secondary school, which were collected from the textbook of secondary school and the academic test for the junior high school students. There are six kinds of components such as resistor, slide resistor, light, ammeter, voltmeter and power supply in circuit schematic will be recognized by our approach. The statistics of these components in dataset are shown in Table 1.

Table 1.   Statistics on the dataset of experiment

	#CS	#R	#SR	#L	#A	#V	#S
Total	145	180	67	138	96	76	145

Note: **#CS** = Circuit schematic,
#R = Resistor, **#SR** = Slide resistor,
#L = Light, **#A** = Ammeter, **#V** = Voltmeter,
#S = Power supply.

5.2   Experimental Results

To test the generality and practicability of our approach, we have made experiments on the prepared dataset and part of the results are shown in Table 2.

Table 2.   Part of experimental results

No.	1	2	3	460	3100	3740	3750	3820	3890	3930
N_s	7	6	6	6	6	6	5	6	6	5
N_f	5	2	2	5	5	4	2	2	4	2
T	85.45	97.97	81.8	53.08	69.19	57.28	59.81	86.42	61.45	67.52

N_s: the number of symbols recognized, N_f: the number of fork node calculated, T: processing time (ms).

Table 2 shows a part of our experimental results. More circuit schematics and corresponding results are available in http://pan.baidu.com/s/1kUKwcV9. In the experiment, our approach in the identification of circuit symbols has got a good performance that almost all the results are correct. The method of circuit node detection is also meet the design requirements. At the same time, we count the time of processing in Table 2 that indicates our approach is a time-saving work.

6   Conclusions

This paper has presented an algorithm for understanding the physics problems at secondary school by extracting the relations from circuit schematics. The algorithm first recognizes the circuit schematics, and then it extracts an enough set of relations. The main contributions of the paper are multiple. The first one is that it proposes the concept of independent node and the method to identity this type of nodes form a given circuit schematics. The second one is that it proposes the concept of independent loop and the method to identity this type of loops from a given circuit schematics. The third one is that it shows that the set of relations extracted from independent nodes and independent loops from a given circuit schematics are enough for solving the given problem. The experimental results show that the proposed algorithm is very promising in solving the concerning type of exercise problems.

Two of more jobs can be done in the future based on the results of this paper. We first can study how to use the deep learning algorithm to extract relations. Then we can do research on extracting relations from more complex circuit schematics.

References

1. Weyten, L., Rombouts, P., Catteau, B., De Bock, M.: Validation of symbolic expressions in circuit analysis e-learning. IEEE Trans. Educ. **54**, 564–568 (2011)
2. Ozogul, G., Johnson, A.M., Moreno, R., Reisslein, M.: Technological literacy learning with cumulative and stepwise integration of equations into electrical circuit diagrams. IEEE Trans. Educ. **55**, 480–487 (2012)
3. Huelsman, L.P.: Symbolic analysis-a tool for teaching undergraduate circuit theory. IEEE Trans. Educ. **39**, 243–250 (1996)
4. Weyten, L., Rombouts, P., De Maeyer, J.: Web-based trainer for electrical circuit analysis. IEEE Trans. Educ. **52**, 185–189 (2009)
5. Reisslein, J., Johnson, A.M., Reisslein, M.: Color coding of circuit quantities in introductory circuit analysis instruction. IEEE Trans. Educ. **58**, 7–14 (2015)
6. Johnson, A.M., Butcher, K.R., Ozogul, G., Reisslein, M.: Introductory circuit analysis learning from abstract and contextualized circuit representations: effects of diagram labels. IEEE Trans. Educ. **57**, 160–168 (2014)
7. Chang, C.-C., Lin, C.-J.: LIBSVM: a library for support vector machines. ACM Trans. Intell. Syst. Technol. (TIST), **2**, 27 (2011)
8. Chiu, P., Chen, F., Denoue, L.: Picture detection in document page images. In: Proceedings of the 10th ACM Symposium on Document Engineering, pp. 211–214. ACM (2010)
9. Mandal, P.D.S., Bhowmick, P., Chanda, B.: Topological simplification of electrical circuits by super-component analysis. In: 2015 13th International Conference on Document Analysis and Recognition (ICDAR), pp. 211–215. IEEE (2015)
10. Von Gioi, R.G., Jakubowicz, J., Morel, J.-M., Randall, G.: LSD: a fast line segment detector with a false detection control. IEEE Trans. Pattern Anal. Mach. Intell. **32**, 722–732 (2010)
11. Schölkopf, B., Smola, A.J., Williamson, R.C., Bartlett, P.L.: New support vector algorithms. Neural Comput. **12**, 1207–1245 (2000)
12. Smith, R.: An overview of the tesseract OCR engine. In: 2007 Ninth International Conference on Document Analysis and Recognition, ICDAR 2007, pp. 629–633. IEEE (2007)
13. Wang, H.-Y., Pan, D.-L., Xia, D.-S.: A fast algorithm for two-dimensional Otsu adaptive threshold algorithm. Acta Automatica Sinica **33**, 968–971 (2007)
14. Xu, C., Tang, Z., Tao, X., Shi, C.: Graphic composite segmentation for PDF documents with complex layouts. In: Proceedings of SPIE Document Recognition and Retrieval XX, p. 8658 (2013)
15. Zirari, F., Ennaji, A., Nicolas, S., Mammass, D.: A simple text/graphic separation method for document image segmentation. In: 2013 ACS International Conference on Computer Systems and Applications (AICCSA), pp. 1–4. IEEE (2013)