Chapter 15
Conclusions

Several stages of decoupling capacitors are typically placed across the power and ground lines to bypass inductive interconnect. Decoupling capacitors are the focus of Part III. While effective for reducing the high frequency impedance of power distribution system, decoupling capacitors are only useful within a certain frequency range due to inherent parasitic resistances and inductances.

The efficient placement of decoupling capacitors is described in this part. Traditionally, decoupling capacitors have been placed within the available on-chip area. This approach, however, is not effective. Decoupling capacitors need to be placed within a specific distance from the current source to allow the charge to be efficiently transferred from the power supply to the decoupling capacitor, and within a specific distance from the load to achieve efficient charge transfer from the decoupling capacitor to the load. Based on these distances (or radii), the efficient placement of decoupling capacitor is described in Part III.

The power delivery system can be further enhanced by distributing the decoupling capacitors, starting from a large decoupling capacitor placed far from the load and ending with small distributed decoupling capacitors placed close to the load. Signal integrity is also greatly enhanced by utilizing this methodology. Additionally, the co-design of the distributed on-chip power supplies and decoupling capacitors is described in Part III, supporting the simultaneous placement of decoupling capacitors with the on-chip power supplies. These power supplies can be placed in close proximity to the load, since the size of these power supplies is relatively small.

These methodologies are described for different systems under a variety of constraints, exhibiting both computational efficiency and accuracy. The important issue of efficiently placing on-chip decoupling capacitors is the primary topic of this part.

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