

# Development of a Simulink Model of a Saturated Cores Superconducting Fault Current Limiter

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**Abstract.** Superconducting fault current limiters are considered as emerging devices for the advent of modern power grids. Those limiters as well as other electric power grid applications have been developed in the last years in order to support the increased penetration of dispersed generation. The development of such limiters requires new design tools that allows to simulate those devices in electrical power grids with different voltage ratings and characteristics. This work presents a methodology to simulate the behaviour of saturated core type limiters based on its characteristic curves. A prototype is tested to obtain its characteristic and then the methodology is implemented in Simulink. The simulation carried out by the proposed methodology is compared with a real test.

**Keywords:** Fault current limiters · Saturated-core fault current limiters · Modern power grids · Smart grids · Short-circuit currents · Superconductivity

## 1 Introduction

Superconducting Fault Current Limiters (SFCL) have been considering as emerging and attractive devices enabling an increased integration of distributed generation sources in modern power grids, due to their ability to limit fault currents and thus helping to mitigate several operation problems that such grids can experience [1].

Amongst all different topologies of inductive SFCL, the saturated cores topology [2], originally proposed in [3], involves the use of highly saturated iron cores that can be achieved by a high DC current flowing in a high temperature superconducting (HTS) coil. When the line current exceeds normal operation limits, e.g. due to a fault, the inductance increases abruptly, limiting the current through an inductive voltage drop. In this situation, the cores of the limiter alternate between saturated and unsaturated states.

In the last years, several projects were carried out using this topology. Zenergy Power Company operated a 15 kV three-phase limiter in the Southern California

Edison substation and an 11 kV in CE Electric UK substation [4]. Other company, InnoPower, developed a 35 kV/ 90 MVA device [5]. InnoPower has also been testing a 220 kV/300 MVA [6].

Finite elements method (FEM) software packages are often used to simulate the performance of these devices [7]. However, simulating a SFCL with FEM software can take a considerable amount of time, from several hours to days or weeks, even when considering simple devices in very simple grids.

In order to reduce the simulation time and to simulate those devices in more complex grids, a numerical method that can be applied to perform fast dynamic simulations of saturated cores SFCL is proposed in this work and is implemented in Matlab/Simulink. This methodology is based on the relationship between the linked flux with the primary of the device  $\psi_{FCL}$  and the line current  $i_{line}$ . The dynamic behaviour of the SFCL is thus simulated based on this  $\psi_{FCL}$ - $i_{line}$  characteristic. This is an extension of the methodology proposed for transformer type SFCL [8–10] and presented in [11] for saturated cores SFCL.

This work also constitutes one of several studies that needs to be addressed in order to answer the following research question:

*Are there development methodologies and simulation tools of Saturated Cores Fault Current Limiters, allowing analysing its performance in power grids with different degrees of complexity, and thus contributing to sustained advent of technologies based on superconducting materials?*

Integration of SFCL devices in power grids depends also on developing tools to simulate them under different conditions, such as PSCAD or others. This work provides a contribution for such developments.

## 2 Contribution for Technological Innovation for Cloud-Based Engineering Systems

Electric energy demand has grown yearly, which means that there is a significant increase in the penetration of distributed generation (DG) to satisfy this increase in demand. To make a grid “smart” is essential to manage the future power grids especially from the usage of networked power devices. Smart Grids (SG) offer deep monitoring and controls of the grid but needs advanced analytics to analyse, to process and to storage the considerably big amount of data for safety efficient and reliable operational decisions. In order to project an efficient and scalable SG, solutions and services based on Cloud Computing must be incorporated [12].

In the energy domain, fail-safe power grids are foreseen, ensuring safety and power quality, supporting the coexistence of central and distributed generation, energy storage and bidirectional energy flow. SFCL exhibits several features that make them attractive in protecting network equipment as well as allowing improving network availability, contributing to assure fail-safe grids and thus robust and efficient SG [13].

### 3 Proposed Methodology Based on SFCL Characteristic

The proposed methodology is based on the magnetic characteristic of the limiter which relates line current  $i_{line}$  and linked flux with the primary  $\psi_{FCL}$ . This characteristic is able to describe the electromagnetic behaviour of the limiter. Equation 1 shows the developed voltage drop at the terminals of the SFCL that is directly related with the SFCL characteristic.

$$u_{SFCL}(t) = r_{SFCL} \cdot i_{line}(t) + \frac{d\psi_{SFCL}(t)}{dt} = r_{SFCL} \cdot i_{line}(t) + \frac{d\psi_{SFCL}(t)}{di} \cdot \frac{di_{line}(t)}{dt} \tag{1}$$

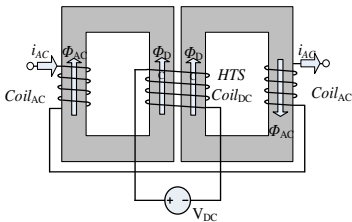
Knowing the characteristic of the SFCL, it is possible to develop an adequate computational model for power system simulation software (such as PSCAD or SimPowerSystems/Simulink), that do not rely on knowledge of circuit equations, which is practically unfeasible.

The first step of the methodology consists of determining the magnetic characteristic of the limiter  $\psi_{FCL}$ - $i_{line}$ . This characteristic may be determined by real tests. Using the characteristic obtained it is possible to implement the SFCL in Simulink, as a variable inductance. Thus, the limiter may be simulated in grids with different complexities and faster than recurring to FEM software.

#### 3.1 Operation Principle of the Saturated Cores Fault Current Limiter

Several different geometries of this type of SFCL have been proposed. However the operation principle of the limiter remain the same [3]. Fig. 1 shows the basic elements of single-phase saturated cores SFCL.

Under normal operation, AC current in the AC coils creates a magnetic flux that is lower than the DC bias flux, remaining the iron cores highly saturated and making the impedance of the limiter negligible. However, when a fault occurs, the AC current increases abruptly, leading the cores out of magnetic saturation alternately. The line impedance is increased and the fault current is limited.



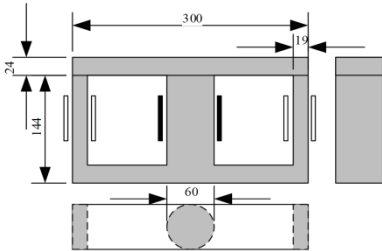
**Fig. 1.** Single-phase saturated cores SFCL conceptual diagram. It is composed of a HTS DC coil embracing the cores and two conventional AC coils connected in series with the line under protection wound on the outer limbs.

## 4 Experimental Test to Determination of the Characteristic of the SFCL

In order to determine the characteristic of the limiter, experimental measurements were carried out.

### 4.1 Topology of the Limiter and Experimental Apparatus

Fig. 2 shows the dimensions of the laboratory scale limiter used to develop the presented methodology. The core used for the tests was an EI iron core (instead of two separated cores). The AC coils are placed on the outer limbs and the DC biasing coil is placed in the inner limb (which has round cross section) of the core. The magnetic core provides closed magnetic paths for each outer limb. Therefore to assure that both outer limbs are driven into deep saturation, their cross sections must be less than 50% of the inner limb core section. In the present case, the outer limbs cross section are 40% of the inner limb cross section.



**Fig. 2.** Dimensions of the iron core of the limiter. All dimensions are in millimetres.

The test circuit comprises a voltage source  $u_g$ , a line resistor  $R_{Line}$ , a load  $R_{Load}$ , a circuit breaker  $S_f$  (used to simulate faults) and the SFCL. The AC coils are made of copper wire with  $1.3 \text{ mm}^2$  cross section, 100 turns each. A 60 turns DC coil is built from 4 mm-wide first generation superconducting tape. Table 1 shows the parameters of the test grid. More detailed information can be found in [11].

The core must be highly saturated in order to make the impedance of the limiter negligible in normal operation and, at the same time, can not be saturated too deeply since it can go out the saturation, limiting the fault current. Thus, it is necessary to choose an adequate magneto motive force (MMF) value ensuring that all limbs of the core are saturated. Therefore, 35 A were chosen as DC current, corresponding to a MMF of 2100 A·turn.

**Table 1.** Characteristics of the test grid

Grid	Description	Value
$u_g$ (V)	Voltage source	100
$f$ (Hz)	Frequency of the electrical grid	50
$R_{Line}$ ( $\Omega$ )	Line resistance	1
$R_{Load}$ ( $\Omega$ )	Load resistance	20
$I_{DC}$ (A)	DC bias current	35

## 4.2 Determination of the Characteristic of the SFCL

A test was carried out considering the parameters shown in Table 1. A fault was applied on the test circuit and data was acquired with a data acquisition board to a computer.

Fig. 3 shows the individual characteristic  $\psi_{FCL}-i_{line}$ , associated to each AC coil and the equivalent characteristic of the limiter, obtained by combining the previous ones. When line current is low,  $d\psi_{FCL}/di_{line}$  is also low, thus the line current flows with any limitation. In fault condition, a high  $d\psi_{FCL}/di_{line}$  is reached and an inductive voltage drop at the terminals of the limiter limits the line current.

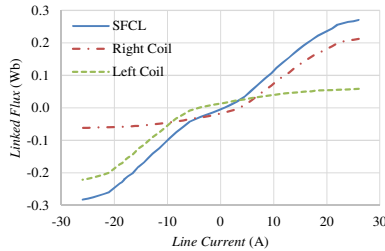


Fig. 3. Measured  $\psi_{FCL}-i_{line}$  characteristic of each AC coil and calculated SFCL characteristic

## 5 Simulation of the FCL by the Developed Methodology

The presented methodology is based on the measured characteristic of the SFCL. A Simulink model of the SFCL was built based on its characteristic.

### 5.1 Model for the Dynamic Simulation of SFCL

To simulate the SFCL in Simulink was necessary to build a model that describes the SFCL behaviour according to Equation 1. The model may be built with a dependent current source that imposes a specific current in the line depending on the characteristic of the SFCL. The characteristic of the SFCL is function of linked flux and line current, thus if the linked flux is known the current that the SFCL should impose is also known. Equation 2 shows how the linked flux may be calculated, by the integration of the voltage drop over the SFCL  $u_{FCL}$ , and subtraction of the resistive voltage drop over the SFCL  $r_{FCL} \cdot i_{line}$ . Fig. 4 shows the model in Simulink. The model is composed of a set of blocks that compute the linked flux according to Equation 2, a lookup table block (so-called Psi-i) that computes the current according to the linked flux with the primary of the SFCL, and a dependent current source block (so-called Inject SFCL current) which provides the current in the line.

$$u_{FCL}(t) = r_{FCL} \cdot i_{line}(t) + \frac{d\psi_{FCL}(t)}{dt} \Leftrightarrow \frac{d\psi_{FCL}(t)}{dt} = u_{FCL}(t) - r_{FCL} \cdot i_{line}(t) \Leftrightarrow \quad (2)$$

$$\Leftrightarrow \psi_{FCL}(t) = \int (u_{FCL}(t) - r_{FCL} \cdot i_{line}(t)) \cdot dt$$

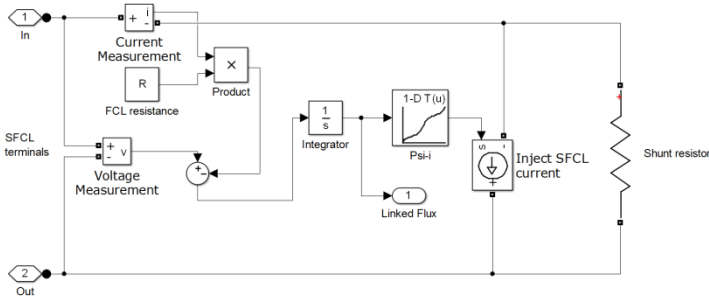


Fig. 4. Simulink model for the SFCL implementation

### 5.2 Evaluation of the Dynamic Behaviour of SFCL

To evaluate the behaviour of the SFCL using Simulink software, an electrical diagram was built. Fig. 5 shows this circuit, in the Simulink environment, which is composed of a voltage source, a line impedance, a load impedance, a circuit breaker and the SFCL.

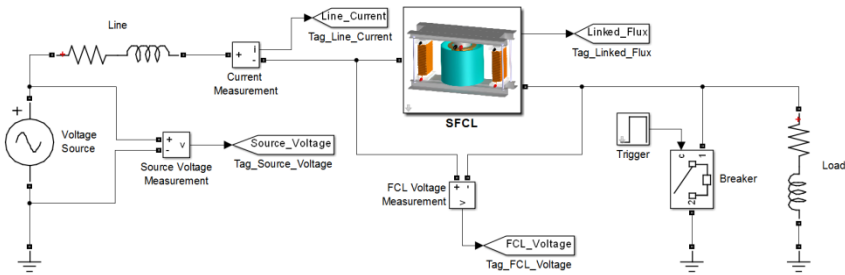


Fig. 5. Test grid implemented in Simulink

The achieved results from the proposed methodology were compared with real tests. Therefore, a simulation using this methodology and a real test were carried out considering  $u_g=50 \text{ V}_{rms}$ ,  $R_{line}=1 \Omega$  and  $R_{load}=20 \Omega$  (to compare the simulation with the real test the line and load are considered purely resistive). The internal resistance of the SFCL is  $R_{SFCL}=0.4 \Omega$ . A short-circuit was applied around  $t=1.49 \text{ s}$  and cleared around  $t=2.49 \text{ s}$ .

Fig. 6 shows the evolution of the line current as a function time, measured and predicted by the proposed methodology. Both curves show similar behaviour and good agreement. The fault current was limited to around 75% of the prospective current.

Fig. 7 shows the voltage drop of the SFCL as a function of time. As depicted, when a fault occurs the voltage drop increases and the fault current is thus limited. At normal operation, the voltage drop is less than 10% of the voltage power source.

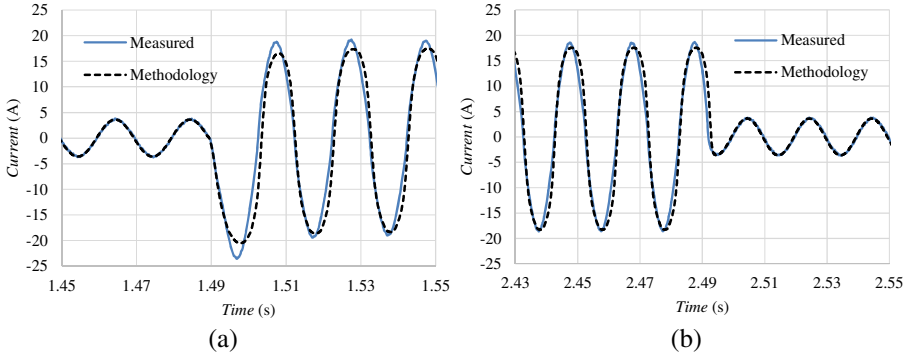


Fig. 6. Comparison between measured and predicted currents in the circuit under a fault. (a) At the moment the fault occurs (b) At the moment the fault is removed.

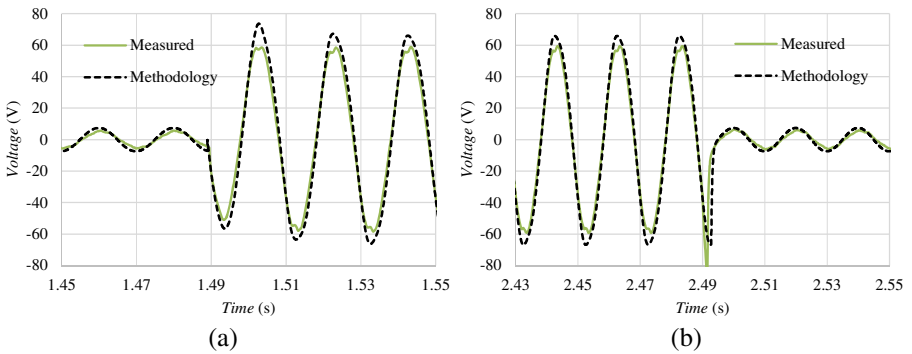


Fig. 7. Comparison between measured and predicted voltages drop in the SFCL under a fault. (a) At the moment the fault occurs (b) At the moment the fault is removed.

## 6 Conclusions

A methodology to simulate the dynamic behaviour of the saturated cores SFCL in an electrical grid was presented in this paper. The methodology shows good agreement with experimental measurements. Its main advantage is a drastic decrease in simulation times when compared with FEM software. This allows simulating these devices in complex grids, which is one requisite of utilities. Future work passes by including DC current explicitly in the  $\psi_{FCL}-i_{line}$  curve expression.

## References

1. Moon, W., Won, J., Huh, J., Kim, J.: A Study on the Application of a Superconducting Fault Current Limiter for Energy Storage Protection in a Power Distribution System. *IEEE Trans. Appl. Supercond.* **23**, 5603404 (2013)
2. Lee, P.J.: Applications and Related Technology. *Engineering superconductivity*, p. 391. John Wiley & Sons, Inc. (2001)
3. Raju, B.P., Parton, K.C., Bartram, T.C.: A Current Limiting Device Using Superconducting D.C. Bias Applications and Prospects. *IEEE Power Eng. Rev.* **PER-2**, 34–35 (1982)
4. Moriconi, F., De La Rosa, F., Darmann, F., Nelson, A., Masur, L.: Development and Deployment of Saturated-Core Fault Current Limiters in Distribution and Transmission Substations. *IEEE Trans. Appl. Supercond.* **21**, 1288–1293 (2011)
5. Xin, Y., Gong, W., Niu, X., Cao, Z., Zhang, J., Tian, B., Xi, H., Wang, Y.: Development of Saturated Iron Core HTS Fault Current Limiters. *IEEE Trans. Appl. Supercond.* **17**, 1760–1763 (2007)
6. Xin, Y., Gong, W.Z., Sun, Y.W., Cui, J.B., Hong, H., Niu, X.Y., Wang, H.Z., Wang, L.Z., Li, Q., Zhang, J.Y., Wei, Z.Q., Liu, L., Yang, H., Zhu, X.H.: Factory and Field Tests of a 220 kV/300 MVA Saturated Iron-Core Superconducting Fault Current Limiter. *IEEE Trans. Appl. Supercond.* **23**, 5602305 (2013)
7. Shahbazi, Y., Niayesh, K., Mohseni, H.: Finite element method analysis of performance of inductive saturable-core fault current limiter. In: 2011 1st International Conference on Electric Power Equipment - Switching Technology, pp. 352–355. IEEE (2011)
8. Pina, J.M., Suárez, P., Neves, M.V., Álvarez, A., Rodrigues, A.L.: Reverse engineering of inductive fault current limiters. *J. Phys. Conf. Ser.* **234**, 032047 (2010)
9. Pina, J.M., Pereira, P., Pronto, A., Arsénio, P., Silva, T.: Modelling and Simulation of Inductive Fault Current Limiters. *Phys. Procedia.* **36**, 1248–1253 (2012)
10. Arsenio, P., Silva, T., Vilhena, N., Pina, J.M., Pronto, A.: Analysis of Characteristic Hysteresis Loops of Magnetic Shielding Inductive Fault Current Limiters. *IEEE Trans. Appl. Supercond.* **23**, 5601004 (2013)
11. Vilhena, N., Arsenio, P., Pina, J., Pronto, A., Alvarez, A.: A methodology for modelling and simulation of saturated cores fault current limiters. *IEEE Trans. Appl. Supercond.*, 1–1 (2014)
12. Bitzer, B., Gebretsadik, E.S.: Cloud computing framework for smart grid applications. In: 2013 48th International Universities' Power Engineering Conference (UPEC), pp. 1–5. IEEE (2013)
13. Behzadifari, S., Salehfar, H.: Using superconducting fault current limiters to enhance the reliability of power transmission systems. In: IEEE PES General Meeting, pp. 1–8. IEEE (2010)