Chapter 3
Chirp Generators for Millimeter-Wave FMCW Radars

Dmytro Cherniak and Salvatore Levantino

Abstract The vast number of radar applications generates the demand for highly-linear, low-noise, fast chirp generators implemented in nanoscale CMOS technologies. Off-the-shelf chirp synthesizers are realized in BiCMOS technologies and demonstrate excellent phase noise performances, though, at high cost and limited modulation speed. This chapter describes a new class of fast and reconfigurable chirp generators based on digital bang-bang phase-locked loops, suitable for integration in modern CMOS processes. After analyzing the impact of the chirp generator impairments on a frequency-modulated continuous-wave (FMCW) radar system, a novel pre-distortion scheme for the linearization of critical blocks is introduced to achieve at the same time low phase noise and fast linear chirps. The chirp generator fabricated in 65-nm CMOS technology demonstrates above-state-of-the-art performance: It is capable of generating chirps around 23-GHz with slopes up to 173 MHz/μs and idle times of less than 200 ns with no over or undershoot after an abrupt frequency step. The circuit consuming 19.7 mA exhibits a phase noise of −100 dBc/Hz at 1 MHz offset from the carrier and a worst case in-band fractional spur level below −58 dBc.

Keywords CMOS · Phase-locked loops · Radar

3.1 Introduction

Cost reduction is the cornerstone in nowadays radar systems. The radar technology, which has been for a long time, since the invention in early 1930s, exclusive to military and defence, is now being adopted in a wide spectrum of applications

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including automotive, industrial and consumer market [1, 2]. In the context of advance driver assistance system (ADAS) and autonomous driving, the radar technology has been employed for about two decades for object detection as well as range, relative velocity and azimuth sensing. In the future, the combination of radar sensors with machine learning will enable the vision of the vehicle. In comparison with other environmental perception sensors such as cameras and light detection and ranging (LIDAR), radars operate under foggy, dusty, snowy and badly lighted environment, which is essential for the automotive applications [3, 4]. Initial automotive radar sensors were extremely expensive as they were based on discrete circuit elements. The next-generation radar systems were implemented with several monolithic microwave integrated circuits (MMICs) in high-performance GaAs technology [1]. Further cost reduction and increased level of integration was achieved by moving to SiGe bipolar or BiCMOS technology [5]. Most of the nowadays radar systems are realized in BiCMOS technology, but the fast development of the automotive industry demand for a single-chip radar solution in modern CMOS technology [6].

In a frequency-modulated continuous-wave (FMCW) radar system, an FM-modulated carrier is transmitted and the delay between the reflected and the transmitted carriers is taken as a measure of the distance, i.e. the range, between the radar and the target. Using triangular or saw-tooth waveforms to frequency-modulate the carrier, the delay between the reflected and transmitted signals can be easily and accurately measured by detecting the frequency offset between the two signals, as shown in Fig. 3.1. A carrier with a linear FM modulation is referred to as a *chirp* signal. The performance of an FMCW radar is mainly determined by the speed, linearity and phase noise of the chirp generator [7]. Different radar applications require different chirp configurations as well as different noise levels. In general, enlarging the modulation bandwidth, i.e. the peak-to-peak amplitude of the chirp modulation signal, improves the range resolution and lowering the phase noise increases the signal-to-noise ratio (SNR). However, reducing the period of the chirp (enabling fast chirps) would be one of the keys to improve the radar system performances. In fact, fast chirps allow:

- a larger separation in frequency of the targets,
- increasing the beat frequency beyond the flicker noise corner,
- increasing the maximum unambiguous velocity,
- improving the velocity resolution,
- averaging the detected signal, thus improving the SNR [8].

3.2 Digital PLL with Two-Point Modulation Scheme

The architecture of the DPLL-based modulator with the two-point injection technique is presented in Fig. 3.2a. The modulation signal $mod[k]$ is simultaneously applied with inverted sign to the feedback path of the phase-locked loop as well as added to the output of the digital loop filter. The above configuration allows to overcome

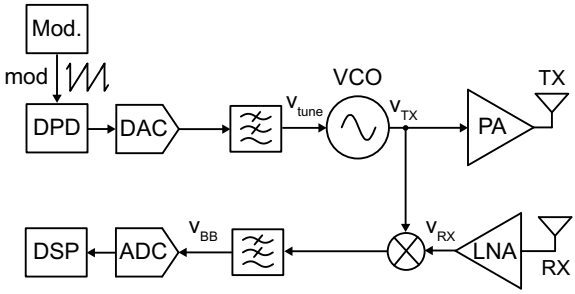

Fig. 3.1 FMCW radar architecture

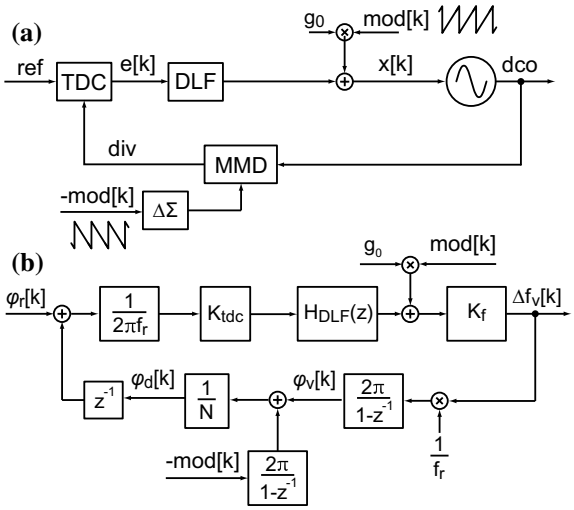

Fig. 3.2 DPLL-based modulator with two-point injection **a** architecture and its **b** phase-domain model

the bandwidth limitation of the conventional PLL-based modulators [9]. Figure 3.2b presents the simplified linearized phase-domain model of the DPLL-based modulator architecture in Fig. 3.2a. The signals $\varphi_r[k]$, $\varphi_d[k]$ and $\varphi_v[k]$ in Fig. 3.2b represent the variable phase of the reference, divided and output clocks, respectively. The signal $\Delta f_v[k]$ is the variation of the DCO output frequency and f_r is the reference frequency. The transfer function of the DLF is the standard proportional-integral one: $H_{DLF}(z) = \beta + \alpha/(1 - z^{-1})$.

The expression of the loop gain is given by

$$G_{loop}(z) = K \cdot H_{DLF}(z) \cdot \frac{z^{-1}}{1 - z^{-1}}, \tag{3.1}$$

where $K = K_f K_{tdc}/(N f_r^2)$, being N the feedback divider ratio, K_{tdc} the TDC gain expressed in [s/bit], K_f the DCO gain expressed in [Hz/bit].

Denoting as $mod(z)$ and $\Delta f_v(z)$ the z-transforms of the time-domain signal $mod[k]$ and the output frequency variation $\Delta f_v[k]$, and being $G_{loop}(z)$ the PLL

loop gain, the transfer function from $mod(z)$ injected into the feedback to $\Delta f_v(z)$ is:

$$H_{lp}(z) = f_r \cdot \frac{G_{loop}(z)}{1 + G_{loop}(z)}, \tag{3.2}$$

that is the standard low-pass transfer function of a PLL multiplied by f_r.

The transfer function from the other point of injection, at the DLF output, is instead the following one:

$$H_{hp}(z) = \frac{g_0 K_f}{1 + G_{loop}(z)}, \tag{3.3}$$

that is a high pass one.

If the value of the gain g_0 is exactly equal to f_r/K_f, the linear superposition of the two transfer functions results in an all-pass transfer function:

$$\begin{aligned} H_{mod}(z) &= H_{lp}(z) + H_{hf}(z) = \\ &= f_r \cdot \left(\frac{G_{loop}(z)}{1 + G_{loop}(z)} + \frac{1}{1 + G_{loop}(z)} \right) = f_r. \end{aligned} \tag{3.4}$$

In practice, the DCO gain K_f in (3.3) is not only variable over process, temperature and voltage (PVT), but also dependent on the output frequency, given the nonlinearity of a typical DCO tuning characteristic. Thus, the two-point injection technique requires an accurate estimation of g_0 coefficient in order to guarantee that it is always equal to f_r/K_f. Any inaccuracy in DCO gain estimation would alter the $H_{mod}(z)$ transfer function from its ideal value and give rise to the following frequency error:

$$\Delta f_{error} = mod(z) \cdot [f_r - H_{mod}(z)], \tag{3.5}$$

where $H_{mod}(z)$ is the transfer function from $mod(z)$ to $\Delta f_v(z)$, given by (3.4).

Intuitive considerations may suggest that the error made in the estimation of K_f is suppressed by the loop to some extent. However, how this error impacts the output Δf_{error} is not obvious and has never been addressed in the literature. In the following, the analysis of chirp linearity errors in the presence of DCO gain errors is carried out.

Replacing the DCO gain in (3.3) with the estimate $\hat{K}_f$ and computing again the expression of $H_{mod}(z)$, we derive the following equation:

$$\begin{aligned} H_{mod}(z) &= f_r \cdot \left(\frac{K_f}{\hat{K}_f} \cdot \frac{1}{1 + G_{loop}(z)} + \frac{G_{loop}(z)}{1 + G_{loop}(z)} \right) = \\ &= f_r \cdot \frac{1 + (1 + \epsilon_{K_f}) \cdot G_{loop}(z)}{(1 + \epsilon_{K_f}) \cdot [1 + G_{loop}(z)]}, \end{aligned} \tag{3.6}$$

where the last expression follows after introducing the relative gain error ϵ_{K_f}, such that $\hat{K}_f = K_f \cdot (1 + \epsilon_{K_f})$.

The chirp error ϵ_{chirp} normalized to the modulation amplitude BW can be derived (3.5) by replacing the expression of H_{mod} obtained in (3.6):

$$\epsilon_{chirp}(z) = \frac{\Delta f_{error}}{BW} = \frac{mod(z) \cdot f_r}{BW} \cdot \frac{\epsilon_{K_f}}{1 + \epsilon_{K_f}} \cdot \frac{1}{1 + G_{loop}(z)}. \tag{3.7}$$

Equation (3.7) reveals that, in the presence of DCO gain estimation error, the spectrum of the chirp error is given by the spectrum of the modulation signal after high-pass shaping with dominant pole located at around the closed-loop bandwidth of the PLL [the last factor in (3.7)]. This means that the PLL is able to reject chirp errors induced by the gain error, as long as the modulation speed is slow enough with respect to the bandwidth of the closed loop. If, instead, a portion of the spectrum of $mod[k]$ falls outside PLL bandwidth, the loop plays no role and the error propagates to the output causing chirp distortion.[1]

3.3 Adaptive Digital Pre-distortion

In FM modulators based on DPLLs, the nonlinearity of the DCO is the main source of chirp distortion. In practical DCOs, there are several sources of nonlinearity. On top of the intrinsic $1/\sqrt{LC}$ nonlinearity, DCOs may also exhibit a random or periodic nonlinearity due to mismatch within the digitally-controlled capacitor bank.

Figure 3.3 presents a typical class-B LC oscillator where the resonant tank includes a fixed inductor L_T and a digitally-controlled capacitor C_{Tx}, which is typically implemented using high-quality metal-metal capacitors with near-zero temperature and voltage coefficients [10]. However, the parasitic capacitance C_p of the MOS devices (e.g. cross-coupled differential pair, switch, etc.) exhibits a non-zero temperature and voltage coefficients which make the frequency-tuning curve dependent on those parameters.

In principle, DCO tuning characteristic can be linearized by applying the pre-distortion concept depicted in Fig. 3.4. The compensation can be implemented in either analog or digital way. Reference [11] presents a transformer-based LC-oscillator which mitigates the effect of the variable inductance. However, this approach requires complex electromagnetic (EM) simulations for an accurate design of the transformer and of the digitally-controlled capacitors. A more common approach is to implement pre-distortion in the digital domain by means of a look-up table (LUT) or a polynomial which is the inverse of the tuning characteristic of the

[1] More rigorously, the loop gain, $G_{loop}(z)$, in (3.7) should be slightly different from the nominal one, since it is also affected by the DCO gain errors itself ϵ_{K_f}. This correction, however, implies only a negligible variation in the loop gain value, and does not alter appreciably the final result given in (3.7).

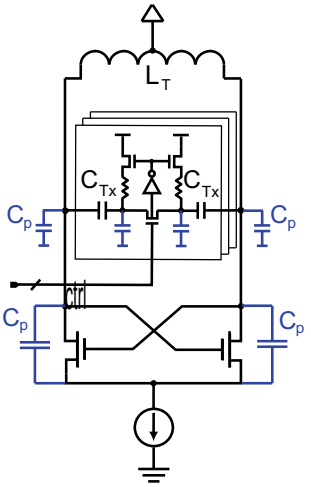

Fig. 3.3 Class-B DCO with annotated parasitic capacitance

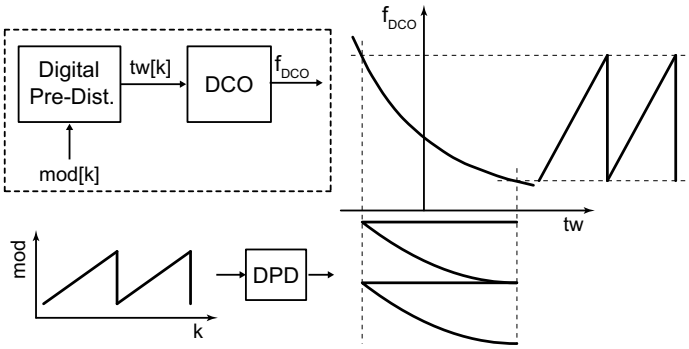

Fig. 3.4 The concept for DCO pre-distortion

DCO. In [12], the pre-distortion coefficients are stored in a 24 kbit SRAM LUT which is filled during the calibration phase that takes 4 s at the start-up. The main issue of this approach is that the pre-distortion coefficients are identified in foreground. So, the calibration is not robust against voltage and temperature variations.

A background calibration of the digital pre-distorter (DPD) was proposed in [13] which describes a DPLL-based phase modulator for wireless communications. The gain required to match the characteristics of each capacitor bank of the DCO is estimated in background by means of the LMS algorithm. The time constant of the implemented background calibration running at 40 MHz clock is in the range of 100 μs which allows effective tracking of slow temperature and voltage variations. To implement an ideal DPD for an N-bit DAC (e.g. like the DCO) a LUT with 2^N fields is required [12]. This kind of complexity is acceptable for the foreground DPD

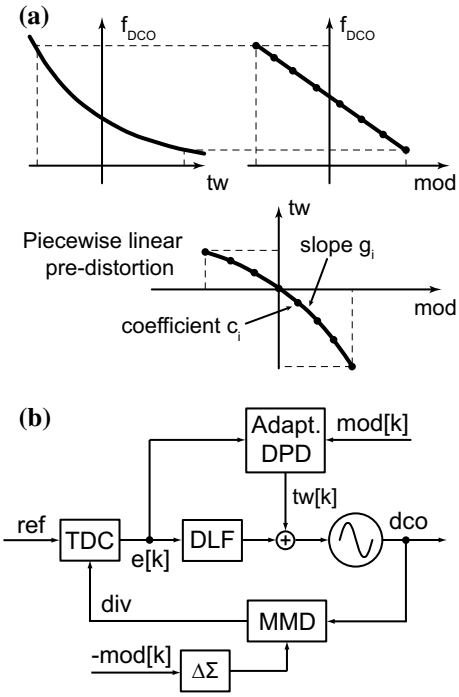

Fig. 3.5 The conceptual drawing of **a** a piecewise-linear DPD and **b** two-point modulator with an adaptive DPD

implementation. However, if the background calibration is required, the complexity of the digital part significantly increases. An LMS-based implementation would require a multiplexer and an accumulator for each LUT field.

The concept of a piecewise-linear DPD is aimed to reduce the complexity of the DPD and make an adaptive implementation feasible. In the context of DPLLs, an adaptive piecewise-linear DPD was originally proposed in [14] and later employed in [15, 16] for the correction of the digital-to-time converter (DTC) and time-to-digital converter (TDC) nonlinearity. The general idea of the piecewise linear DPD is illustrated in Fig. 3.5a. The inverse characteristic of the nonlinear block is approximated with a piecewise-linear curve. The DPD block is intended to remap the modulation signal $mod[k]$ to the tuning word $tw[k]$ in order to achieve a linear tuning characteristic of the output frequency f_{DCO} over the modulation signal $mod[k]$. The piecewise linear characteristic is constructed with a finite set of $\{c_i\}$ and $\{g_i\}$ coefficients representing the position of the segments and the connecting slopes, respectively.

Figure 3.5b presents the concept of the two-point digital PLL-based modulator which incorporates the adaptive DPD. The modulation signal $mod[k]$ is pre-distorted at the high-pass injection point before being applied to the phase-locked loop. The TDC output $e[k]$ is a digital representation of the phase error in the two-point modulator architecture. As it was presented in the previous section, any mismatch between the two injection points would appear as a phase error at the input of the TDC. Thus, the error signal $e[k]$ can be utilized to adapt the DPD characteristic in the background.

3.4 Implemented Prototype

A 23-GHz DPLL-based FMCW modulator was designed and implemented in an existing 65 nm CMOS technology [17]. The prototype features an adaptive piecewise-linear DPD with multiple slope estimation which is applied for DCO nonlinearity correction.

The block diagram of the implemented DPLL-based FMCW modulator is depicted in Fig. 3.6. The DPLL is based on a binary phase detector (BPD) (or a single-bit TDC) which operates in a random noise regime. The regime of the BPD is enabled by means of a DTC similar to the architecture originally proposed in [18]. The feedback path starts with a prescaler-by-four implemented in current-mode-logic (CML), which reduces the frequency of the DCO output to about 5.8 GHz and allows low-power implementation of the multi-modulus divider (MMD) in true-single-phase-clock (TSPC) logic. The output of the prescaler is also used to feed the pad driver.

The single-bit output of the BPD is fed into a digital loop filter which is implemented as a conventional proportional-integral (PI) filter with programmable coefficients. The digital core of the PLL is realized in a single-clock domain which simplifies its design. The clock used for the digital core is the divided clock after the DTC (div). The DPLL is fed with a 52-MHz reference clock derived from an on-chip crystal oscillator with an off-chip resonator.

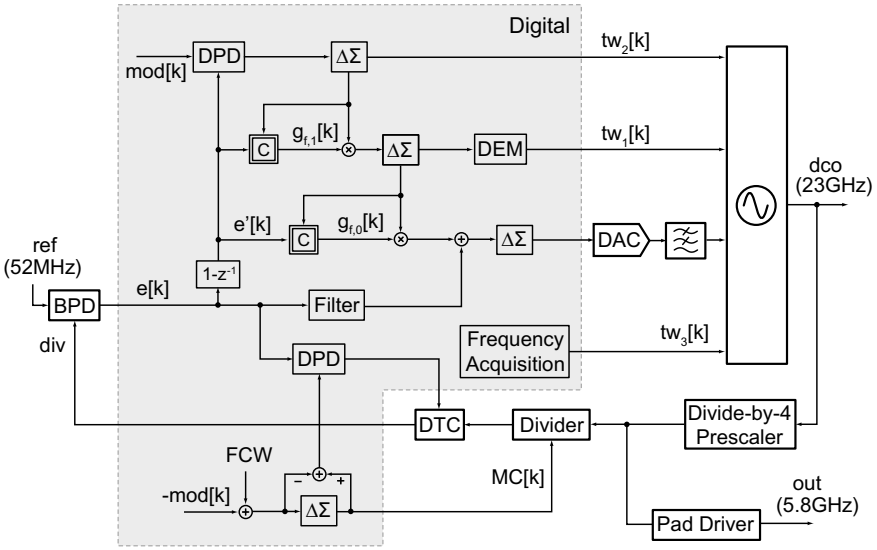

Fig. 3.6 Block diagram of the implemented DPLL-based FMCW modulator prototype

3.4.1 DTC Design and Control

The DTC is intended to cancel the quantization noise introduced by the MMD driven by a second-order $\Delta\Sigma$ modulator. The residual of the MMD quantization noise at the input of a single-bit TDC is within one LSB of the DTC which shall be designed to satisfy the random noise operation [18]. The nonlinearity of the DTC is suppressed by a DPD block [14] which ensures low spur and low phase noise operation of the implemented digital PLL.

The DTC is implemented as buffer with digitally-controlled capacitor load which is followed by a slope-regeneration buffer. Both of the buffers are implemented in CML to improve the rejection to supply disturbances. To realize a large delay-insertion range and fine LSB while maintaining low-area and parasitics, the digitally-control capacitor of the DTC is segmented in two 5-bit thermometer-coded capacitor banks, namely a $coarse$ and a $fine$ bank. Each capacitor bank is implemented using a digitally controlled MOS varactors. The DTC covers about 150-ps range with fine resolution of about 300 fs.

The control scheme of the DTC is based on cancellation of the quantization error which is introduced by the step of the coarse bank at the fine bank. A 16-segment digital piecewise-linear DPD scheme is applied to correct the nonlinearity of the coarse bank, to ensure low-noise and low-fractional spur operation. To match the characteristics of the coarse and fine capacitor banks, the quantization noise of the coarse bank $r[k]$ is scaled by an adaptive gain $\hat{g}_r[k]$ gain. The estimation of $\hat{g}_r[k]$ is implemented based on the LMS algorithm utilizing the quantization noise of the $\Delta\Sigma$ modulator $r[k]$ as a training sequence [18].

3.4.2 DCO Design and Control

To ensure a robust start-up without any additional circuitry, a class-B oscillator topology with an nMOS cross-coupled differential pair has been preferred over a class-C implementation. The main tank inductor is implemented as a single turn coil with a center-tap connected to the supply voltage and with five turns of a top metal layer connected in parallel. A tail filter made of a 75 pH spiral inductor and a 10 pF capacitor is employed to filter the noise of the tail current source, as well as to provide higher impedance at the second harmonic frequency similar to the concept proposed in [19].

To achieve a wide tuning range and fine frequency resolution, the DCO tuning characteristic is segmented in four different digitally-controlled capacitor banks. The coarsest bank is implemented using switched metal-metal capacitors. This capacitor bank is dedicated to coarse frequency tuning only and is designed to achieve about 13% of the tuning range. The finer banks, dedicated to modulation, are implemented using digitally-controlled MOS varactors. The finest tuning bank is implemented using an analog-tuned MOS varactor which is driven by a resistor-string 5-bit DAC.

The finest frequency resolution of the varactor-DAC cascade is about 150 kHz. The achieved complete tuning range is about 16%. The worst-case DCO phase noise, referred to 23 GHz carrier, is −106 dBc/Hz at 1 MHz offset frequency, at 10 mW power consumption. The flicker corner is located at about 200 kHz frequency offset. The control scheme of the multi-bank DCO features an adaptive piecewise-linear DPD applied to the coarsest capacitor bank dedicated to modulation since it contributes the most of the DCO nonlinearity.

The driving scheme for the finer banks is based on canceling the quantization noise of the coarser capacitor banks [13]. To match the characteristics of two consecutive banks, the quantization noise from the coarser banks has to be multiplied by a scaling coefficient (i.e. $\hat{g}_{f1}$ and $\hat{g}_{f0}$). The estimation of the required $\hat{g}_{fi}$ coefficients are done utilizing an LMS algorithm as depicted in Fig. 3.6. A digital delta-sigma modulator $\Delta\Sigma$ is used as a quantizer for each of the modulation capacitor banks since the statistical properties of its quantization noise are well suited for the LMS-based calibration [14]. The quantization noise of the finest bank is filtered by a second-order analog low-pass filter after the DAC.

The two-point modulation technique is implemented completely in the digital domain. The modulation signal $mod[k]$ is simultaneously added to the frequency control word and applied to the coarse tuning bank of the DCO. The adaptive piecewise-linear DPD scheme with multiple slopes estimation is introduced only at the coarse modulation bank, since its mismatch and nonlinearity are the most significant ones. The DPD is implemented with 16 segments. The number of segments is selected as a compromise between the accuracy of the nonlinearity correction and the digital hardware complexity.

3.5 Measurements

The prototype has been fabricated in a standard 65-nm LP CMOS process with no ultra-thick metal layer option. The analog and the digital portions of the chip whose photograph is shown in Fig. 3.7 occupy approximately the same share of the total 0.42 mm^2 area. The output of the frequency divider by four is used to carry out all the measurements. The output of the pad driver is wire bonded to the test board and used for testing. This setup reducing the output frequency to around 5.8 GHz simplifies both phase-noise measurement, which does not require external mixers, and modulation-analysis measurement, as it scales down by four the modulation depth.

The phase noise spectra in integer- and fractional-N modes measured by a R&S FSWP phase-noise analyzer are shown in Fig. 3.8. In both cases, the in-band noise plateau is at about −102 dBc/Hz and the phase noise at 1 MHz offset from the carrier at 5.928 GHz is about −112 dBc/Hz. The latter corresponds to about −100 dBc/Hz at 1-MHz offset when referred to the actual DCO output at 23.712 GHz. In fractional-N mode, the far-out phase noise exhibits a slight increment, increasing the absolute jitter from 213 fs (in integer-N mode) to about 242 fs (in fractional-N mode). Thanks

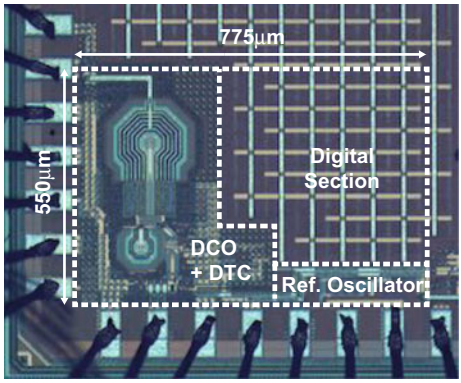

Fig. 3.7 Die photograph

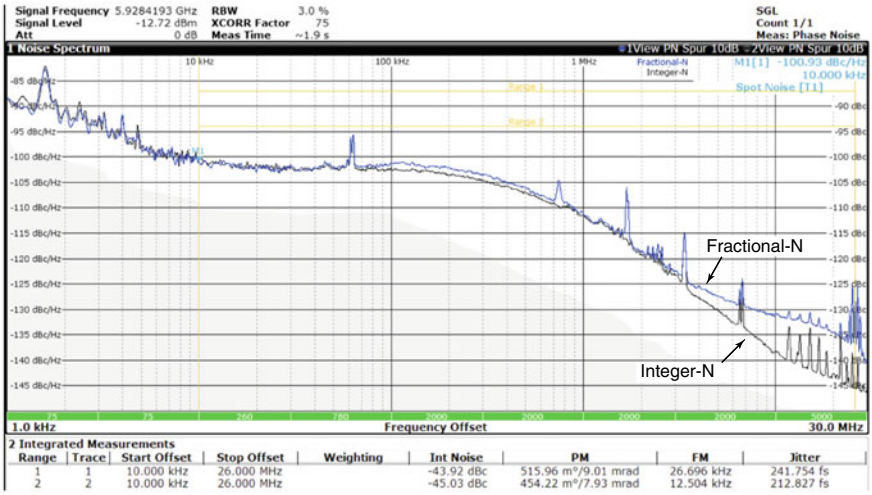

Fig. 3.8 Measured phase noise spectra in both integer-N and fractional-N mode at divider-by-four output

to the DPD of the DTC block, the worst case in-band fractional spur at the offset frequency of 173.8 kHz is below −58 dBc and the out-of-band spur at the offset frequency of 1.62 MHz is below −70 dBc.

An Anritsu MS2850A featuring 1-GHz demodulation bandwidth has been employed as vector signal analyzer (VSA). To assess the efficacy of the DPD in the DCO control, the modulator has been at first tested without enabling the adaptive DPD. A single gain for each bank of the DCO is estimated which corrects for mismatches between coarse and fine banks, but leaves the mismatches among the elements of the coarse bank and the systematic nonlinearity uncorrected. Figure 3.9a shows the demodulated frequency signal for a saw-tooth chirp with 40 µs period and

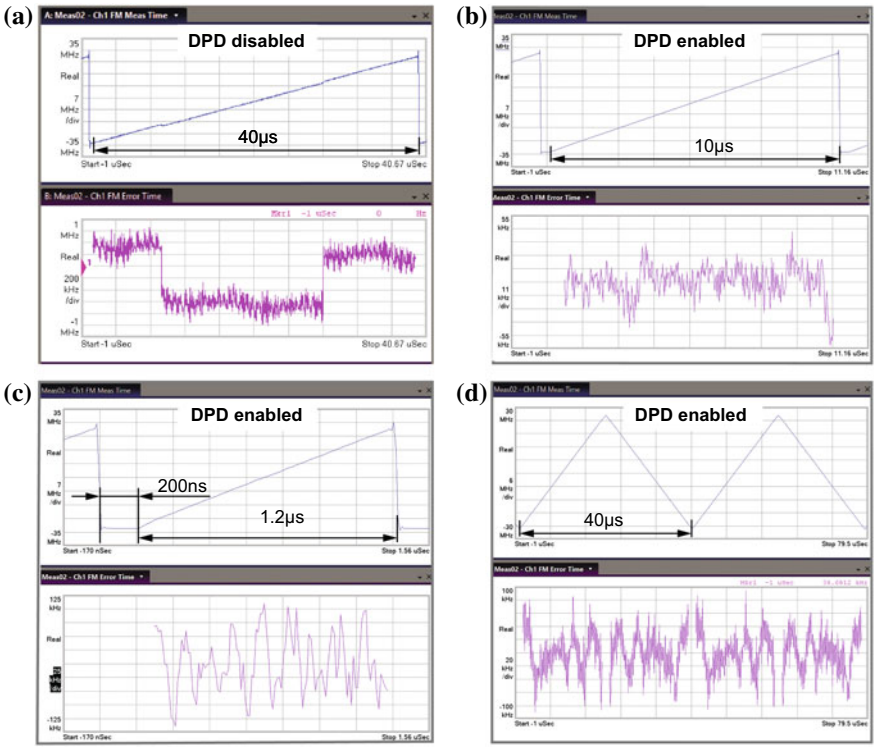

Fig. 3.9 Chirp measurements at divider-by-four output: **a** 40-µs saw-tooth with single-gain calibration (no DPD), **b** 10-µs-saw-tooth with DPD, **c** 1.2-µs saw-tooth with DPD, **d** 40-µs triangular with DPD

52-MHz frequency deviation at the output of the divide-by-four block (equivalent to 208 MHz at DCO output) and the corresponding frequency error. The effects of DCO nonlinearity are clearly visible in the scope, and the peak chirp error is about 1.058 MHz, that is about 2% with respect to the peak-to-peak chirp deviation.

The following figures, Fig. 3.9b–d, present instead the measurements when the adaptive DPD is enabled. The peak-to-peak frequency deviation is 52 MHz in both cases (equivalent to 208 MHz at DCO output). In Fig. 3.9b the chirp rise time is 10 µs, the resulting peak frequency error is below 50 kHz (equivalent to 200 kHz at DCO output), that is less than 0.1% of the maximum frequency deviation, and the RMS chirp error is 0.06%. Figure 3.9c shows the same frequency deviation covered in only 1.2 µs, that results in a state-of-the-art chirp slope of 173 MHz/µs at the DCO output. In this case, the peak error is below 100 kHz (i.e. below 0.2%). The circuit can generate also triangular chirps: Fig. 3.9d shows the demodulated waveform for a 40 µs period. The idle time required to match the 0.1% error specification is lower than 2.4 ns with no over or undershoot, thanks to the introduced DPD circuit which allows to exploit completely the two-point modulation technique.

Table 3.1 Performance comparison

	This Work	Wu JSSC14	Yeo ISSCC16	Vovnoboy JSSC18	Weyer ISSCC18	Ginsburg ISSCC18
Architecture	BBPLL + TPM	ADPLL + TPM	ADPLL + TPM	Analog PLL	DPLL	Analog cascaded PLL
Freq. range (GHz)	20.4–24.6	56.4–63.4	8.4–9.4	75–83	36.3–38.2	76–81
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm BiCMOS	40 nm CMOS	45 nm CMOS
Ref. freq. (MHz)	52	40	276.8	125	120	40
Chirp type	Saw-tooth/Triangular	Triangular	Triangular	Saw-tooth	Triangular	Saw-tooth
Chirp duration (μs)	1.2–315	420–8200	5–220	50–225	50–2000	40
Saw-tooth idle time (μs)	0.2	n/a	n/a	15	n/a	15
Max. chirp Δf_{pp} (MHz)	208	1220	956	8000	500	4000
Max. chirp slope (MHz/μs)	173	4.76	32.6	100	9.1	100
RMS freq. error[b] (kHz)	124/112 (0.06%/0.05%)	384 (0.03%)	1900 (0.12%)	3200 (0.04%)	820 (0.16%)	n/a
Phase noise[a] (dBc/Hz)	−90	−87.7	−86.2	−97	−73.7	−91
Spur level (dBc)	−58	−62	n/a	n/a	−55	n/a
Power (mW)	19.7	48	14.8	590	68	n/a
Area (mm^2)	0.42	2.2	0.18	4.42	0.18	n/a

[a] At 1-MHz offset referred to a 79 GHz carrier
[b] At max. chirp slope

Comparing the presented chirp generator with other state-of-the-art CMOS and BiCMOS implementations in Table 3.1, it can be concluded that the presented DPLL with two point injection and DCO pre-distortion is able to generate fast chirps with the largest maximum slope at better than 0.1% linearity, at competitive phase-noise and power consumption levels.

3.6 Conclusions

Future radar sensors for autonomous vehicles and consumer applications will require fast chirp generators in low-cost CMOS processes. This chapter presented a new class of fast, linear chirp modulators based on digital PLLs and two-point injection of the modulation signal. To mitigate the impact of the nonlinearity of the DCO tuning characteristic, a novel digital piecewise-linear pre-distorter with reduced hardware resources is introduced. The pre-distorter automatically tracks any process and environmental variations. The chirp modulator fabricated in 65-nm CMOS technology demonstrated chirp signals around 23-GHz with slopes up to 173 MHz/μs, less than 0.1% error, and idle times of less than 200 ns.

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