

Conclusions

The efficient placement of decoupling capacitors is the focus of Part IV. Traditionally, decoupling capacitors have been placed within the available space on-chip, however, this approach is not effective. Decoupling capacitors need to be placed within a specific distance from the current source to allow the charge to be efficiently transferred from the power supply to the decoupling capacitor, and within a specific distance from the load to achieve efficient charge transfer from the decoupling capacitor to the load. Based on these distances (or radii), the efficient placement of decoupling capacitor is described in Part IV.

The power delivery system can be further enhanced by distributing the decoupling capacitors, starting from a large decoupling capacitor placed far from the load and ending with small distributed decoupling capacitors placed close to the load. Signal integrity is also greatly enhanced by utilizing this methodology. Additionally, the co-design of the distributed on-chip power supplies and decoupling capacitors is described in Part IV, permitting the simultaneous placement of decoupling capacitors with the on-chip power supplies. These power supplies can be placed at close proximity to the load, since the area of these specially designed power supplies is relatively small.

These methodologies have been investigated for different systems under a variety of constraints, exhibiting efficiency and accuracy. The important issue of efficiently placing on-chip decoupling capacitors is the primary topic of this part.