Oversampled Time Estimation Techniques for Precision Photonic Detectors

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Abstract. The use of oversampling to reduce I/O requirements of time-to-digital converters for arrays of high precision photonic detectors is considered. Simulation results show that the high linearity offered by oversampled converters can be applied to time estimation. The averaging and lowpass filtering inherent in these techniques reduce jitter and enhance estimates of mean time delay. The effect of background illumination on the accuracy of time-of-flight estimates for Lidar range-finding is modeled using a first order sigma-delta modulator. Novel event-driven techniques are proposed for the reduction of sensitivity to background light level.

1 Introduction

Accurate time measurement is commonly required for space science, high energy physics, range finding and fluorescence lifetime sensing. The key component of such systems, integrated Time-to-Digital Converters (TDCs), Time to Analogue Converters (TACs) or gated counters have achieved single-shot resolutions of 10's of pico-seconds [1]. Often however, the quantity that must be estimated accurately is an average time delay between a cyclical stimulus and response. The conventional approach is to take many repeated single-shot time measurements and to construct event histograms. The average delay is then extracted from the mean of the event histogram. Averaging has two favourable effects; to reduce time uncertainty due to jitter and to increase SNR from spuriously generated events due to background noise. Particular examples of this are time-of-flight (TOF) measurement or time-correlated single-photon counting techniques for fluorescence imaging [2,3].

Detectors with both high time precision and sensitivity include photomultiplier tubes and avalanche photodiodes. Single-photon Avalanche Photodiodes (SPADs) have recently been realised in deep submicron CMOS processes [4]. Such detectors promise massively-parallel, single-photon detection with extremely high timing accuracy and

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low dark count. The ability to integrate arrays of SPADs with on-chip TDCs or counters is expected to yield imagers with unprecedented sensitivity and dynamic range. However, the high data bandwidths required to transmit photon arrival times or counts to off-chip memories for histogram construction are likely to have serious implications for power consumption, thermal effects and pin-count.

In this paper, we will apply oversampled techniques to improve the accuracy of average photon arrival time estimation and greatly reduce I/O data bandwidth. This is of particular interest for arrays of photonic detectors such as SPADs which can be integrated together with the other readout and processing circuitry in a single chip.

2 Background

2.1 Time-to-digital Conversion

Time-to-digital conversion is the process of converting time delay linearly into a numeric digital representation. Various architectures have been proposed with time resolutions down to a few picoseconds. However, the linearity of these converters has conventionally been limited to around 10-bits by matching [1]. Jitter and temperature stabilization are other key performance criteria.

Sigma-delta converters have been employed very successfully to achieve very high resolutions and linearity at the cost of reduced bandwidth [5]. To the best of our knowledge, the first use of a sigma-delta modulator within a TDC is described in [6] for the estimation of on-chip clock jitter. The authors construct a cascade of a mixer and lowpass filter with a sigma-delta modulator in order to achieve femtosecond time resolutions.

2.2 Optoelectronic System

The optoelectronic system which will be studied in this paper consists of an illumination source (usually a laser or laser diode) producing very short light pulses (femtosecond or picosecond) at 10-100MHz. The illumination is reflected from a target and returns to a detector and TDC system synchronized to the laser by a clock. This system has been used in the past to perform ranging by the time-of-flight method [7,8]. A similar system may be employed for fluorescence lifetime imaging and various other applications [2,3].

3 Sigma-Delta TDC

Fig. 1 shows a circuit diagram of a simple first order sigma-delta modulator with a time to voltage conversion input. A MASH (Multi-stAge noise Shaping) architecture has been chosen for simplicity and inherent stability although there are many others to which the same concepts may be applied [5]. The operation of the modulator is con-

trolled by the timing waveforms of Fig. 2 and is appropriate to any system with a repetitive pulsed illumination source.

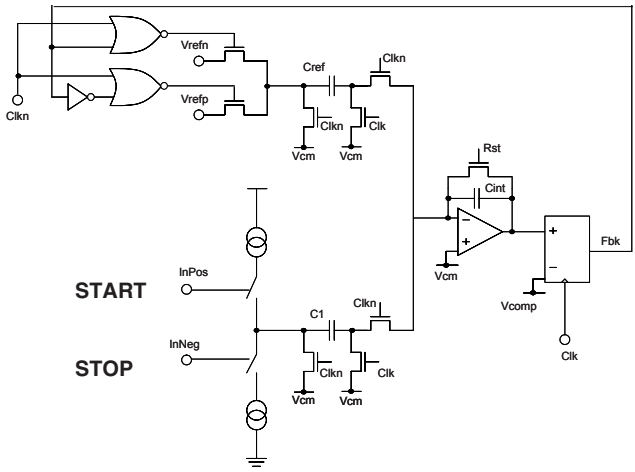

Fig. 1. Sigma-delta Time to Digital Converter based on a first order MASH architecture.

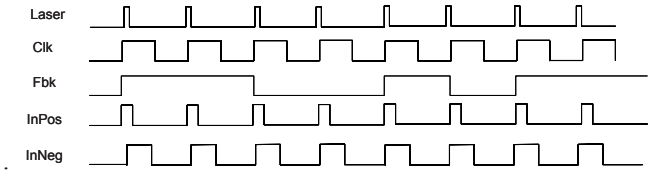

Fig. 2. Sigma-delta TDC timing.

3.1 Operation

The two-phase switched-capacitor implementation of a first order modulator produces an output bit-stream Fbk which will be passed to a lowpass decimation filter (not shown). The clock clk can operate at 10's of MHz synchronized with the pulse repetition rate of the pulsed light source. Fast triggering events from the SPAD or other optical detector generate the waveforms InPos and InNeg. In particular the falling edge of InNeg is related to the detection of the first photon after the laser pulse. Thus the time delay or time-of flight is represented by the delay time between the falling edges of InPos and InNeg.

The current source charge the capacitor C1 to a produce a voltage proportional to the time delay in a similar way to a time-to-analogue converter (TAC) or the charge pump of a PLL. The overlap time between the on-state of the positive and negative current source is based on a technique is used in PLL charge pumps to extend the linear range of conversion and eliminate dead band. Since the current sources are connected passively to the capacitor C1 and common mode voltage Vcm during clk, fast open-loop settling to the nanosecond time intervals of the photonic detector can be achieved. The settling and current requirements of the integrating OTA are determined during the next phase clkn and have a full half clock period. At the end of the period clk, capacitor C1 has been charged to a voltage linearly related to the delay time interval from laser pulse to the first photonic detected. A feedback decision has also been made by the comparator fbk to select either of the reference voltage Vrefn or Vrefp. During the next phase clkn, the selected reference voltage and the voltage on C1 are integrated on the capacitor Cint. This process is repeated over many repetitions of the laser and clock waveform.

3.2 Modeling

To investigate the properties of the system a software model of the modulator and signal source has been developed. We take the particular example of a time-of-flight system where the return signal from the emitted femtosecond pulsed light source is consider to be a Gaussian distributed photon detection peak. This represents the aggregate jitter in the detection system [7] and may originate from a number of sources. The distribution has an adjustable offset representing the TOF and standard deviation representing the jitter.

We also consider a background signal from ambient light or detector dark signal as a Poisson random process parameterized by a mean arrival rate in photons/sec. The output from the detector is considered to be a sequence of delay times of the first photon arrival after the repeated laser pulse. This event may either be triggered by the reflected laser pulse or by a background event photon (internal noise, the dark count rate DCR), whichever occurs first. The detector is considered to generate only one event per clock cycle.

Fig. 3 shows a sample histogram of photon detections for a clock frequency of 25MHz, jitter of 300ps and background arrival rate of 10Mphotons/sec or around 100Lux at 500nm without filtering. We consider that photons detected from the target can be modeled as a set of independent probabilities with different averages as a function of reflectivity. Thus on some clock cycles no photon is returned from the target and events are generated by background illumination, dark count or forced to occur by gating. Note that the jitter and TOF are normalized to the clock period in the forthcoming treatment.

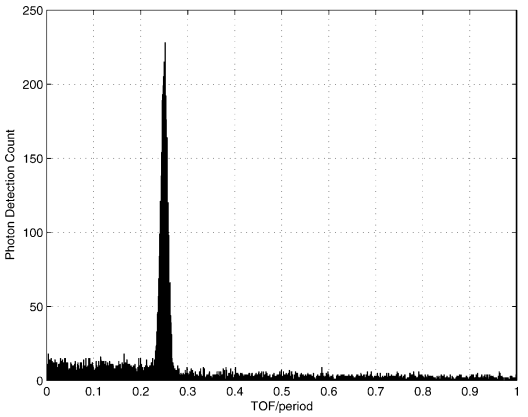

Fig. 3. Sample histogram of the first detected photon for a 25MHz laser repetition rate, 10ns time of flight and 2Mphotons/sec background.

4 Simulation Results

A second order MASH sigma delta modulator with oversampling rate N=256 and 3rd order comb filter has been simulated. A sweep of TOF measurements has been performed and a least mean squares fitting algorithm applied to the decimated modulator output in order to estimate linearity. A number of clock periods (10000) are used before analysis to avoid any transient effects. The noise level at the comb filter output is estimated from the standard deviation of the code over 10000 clock cycles.

Fig. 4 shows the output of the modulator and comb filter with no background noise and a 300ps jitter input with a 25MHz laser and system clock. As expected, the noise has been reduced by sqrt(N) or a factor of 16 from 300ps to 18.75ps. The linearity of the modulator is estimated to be around 10bits, limited only by the RMS noise of the input. As the oversampling factor is increased both jitter and linearity are improved. Note that the jitter on the input signal also acts as a dither and reduces the build up of tones which are known to reduce modulator resolution [5].

Fig. 5 shows the analysis repeated in the presence of 2Mphotons/sec Poisson arrival rate of background illumination. As the TOF is increased there is a greater probability of a background photon triggering the detector rather than the TOF signal. Below 0.1 TOF/period we obtain the same improvement in resolution as in the case without background. Above this level the noise level and distance accuracy is steadily degraded. In Fig. 6 the level of background illumination is varied whilst keeping a fixed TOF input. The minimum and maximum errors from a least mean squares linearity fit on the data is shown in Fig. 7. Below 0.1 TOF/Period the data has good linearity and above 0.1 TOF/Period we see a nonlinear departure and increasing uncertainty.

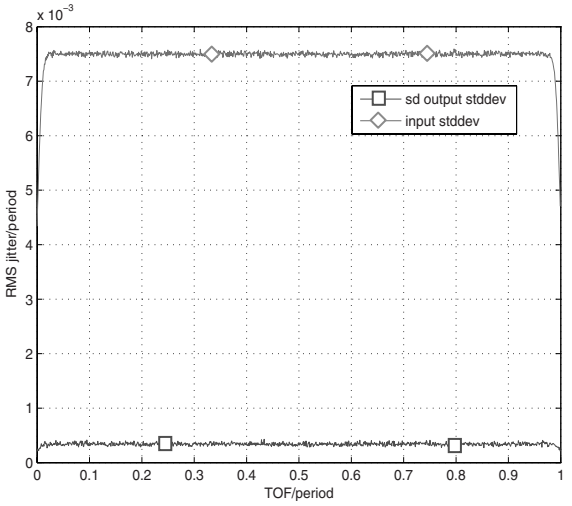

Fig. 4. Relative jitter of a 2nd order modulator/comb filter versus TOF DC level for oversampling ratio 256, period 40ns, input jitter 300ps. A 16x reduction in jitter at the output has been achieved.

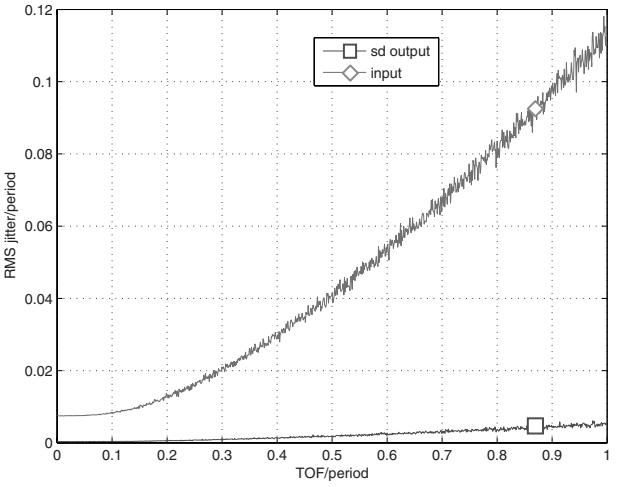

Fig. 5. Relative jitter of a 2nd order modulator/comb filter versus TOF DC level for oversampling ratio 256, period 40ns, input jitter 300ps in the presence of 2Mphotons/sec background illumination.

5 Departure from Linearity

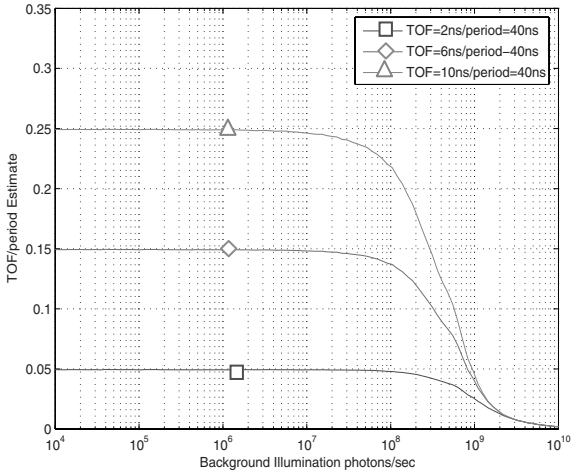

Fig. 6. Modulator output estimate of TOF versus background illumination level for three different TOFs. Shorter TOFs are more resistant to background illumination level.

The simulation results indicate that improvements in linearity, jitter and data rate can be obtained over histogram construction from single-shot TDCs. However, background light will cause departure from linearity when the TOF delay is comparable to the mean Poisson photon inter-arrival time (Fig. 6). Linearity above 10-bit matching level is achievable dependent on correct choice of oversampling rate and input TAC stage.

Fig. 7 shows how the maximum linearity error varies with relative time of flight. The uncertainty is roughly proportional to the relative time of flight. The histogram in Fig. 3 makes an assumption that a photon is received either from the pulsed emission source or the background within every half clock period interval. Two circumstances invalidate this assumption; 1) in a low light environment the probability of receiving a photon will be greatly diminished 2) a low reflectivity target will also greatly reduce the number of detected photons returning from the target. The former case is likely to be encountered in low signal environments such as in fluorescent imaging [9] and the latter in laser ranging with black surfaces or distant targets.

A standard sigma-delta modulator expects an input sample on every clock cycle. In the absence of a trigger from the detector, a full-scale input would be generated to the sigma-delta modulator resulting in a secondary peak of counts at exactly T/2 as shown in Fig. 8. These spurious integrations will skew the average integrated pulse delay [4].

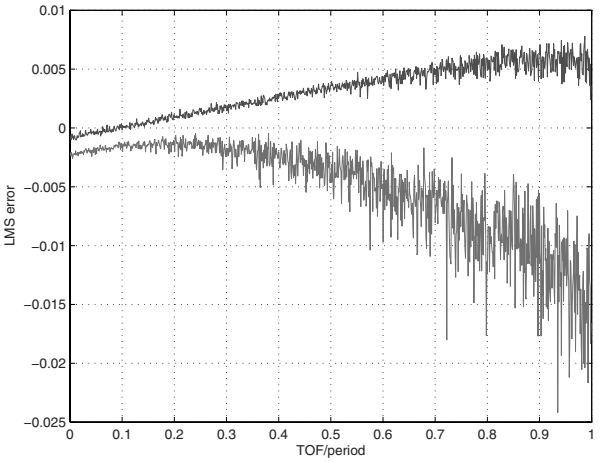

Fig. 7. Maximum and minimum linearity error of a 2nd order sigma-delta modulator versus TOF level for oversampling ratio 256, period 40ns and input jitter 300ps in the presence of 2Mphotons/sec background illumination level.

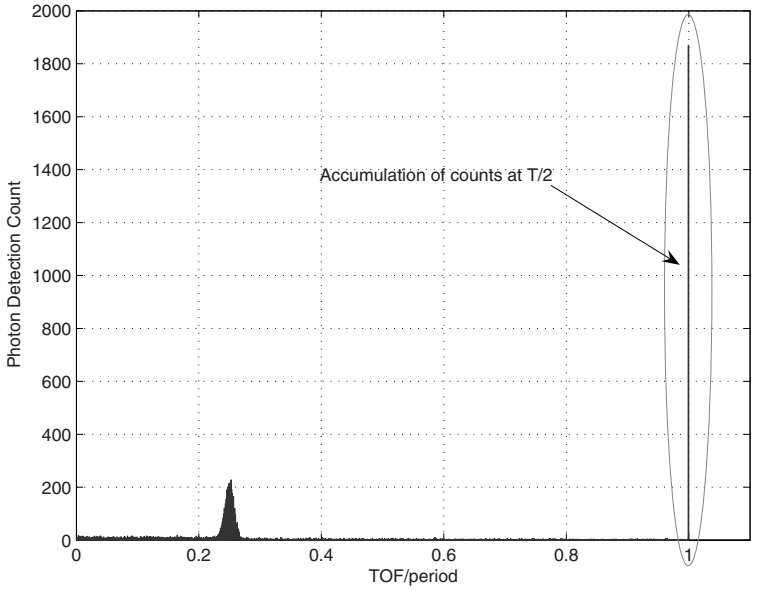

Fig. 8. A sample histogram of the first detected photon for a 25MHz laser repetition rate, 10ns time of flight and 2Mphotons/sec background illumination level. The accumulation of photons at T/2 is due to low probability of photon return from target.

6 Event-driven or Time-windowed Operation

The effects of high background illumination and low photon detection rate can be mitigated by a simple modification of the system operation: event driven clocking of the modulator triggered by a time windowed detector input.

Let us define a lower and upper time bound T_{lo} and T_{hi} where

$$0 < T_{lo} < T_{hi} < T/2 \quad (1)$$

Consider $T_{event}(i)$ to be the time of the first detector event after the i^{th} rising edge of the clock Clk

$$0 < T_{event}(i) < T/2 \quad (2)$$

We generate a new integrating clock signal Clkint(i) such that if

$T_{lo} < T_{event}(i) < T_{hi}$: Clkint(i) = 1

$T_{event}(i) > T_{hi}$: Clkint(i) = 0

$T_{event}(i) < T_{lo}$: Clkint(i) = 0

The integrating clock causes the modulator to integrate the analogue time estimation charge from Cin only if the detector event occurs within the bounds T_{lo} and T_{hi}.

In low light environments, setting T_{lo}=0 and T_{hi}=T/2 will suppress integration of spurious full scale signals due to the absence of an event in the half period time window.

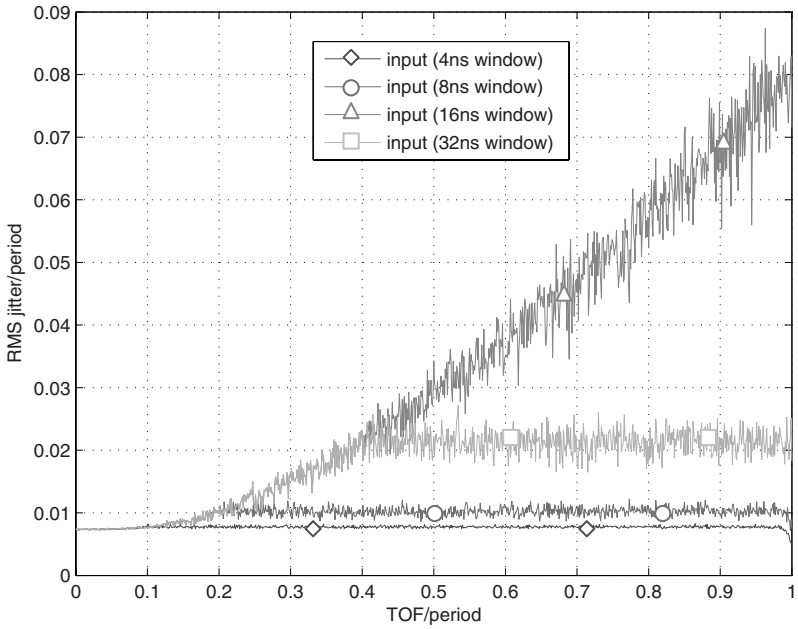

Fig. 9. Event driven operation of a sigma-delta TDC with various time window intervals. Relative jitter of a 2nd order modulator/comb filter versus TOF DC level for oversampling ratio 256, period 40ns, input jitter 300ps in the presence of 2Mphotons/sec background illumination.

In high background light environments T_{lo} and T_{hi} should be narrowed around the mean value of T_{event}. Triggers from the detector are inhibited until the falling edge of Clk. This pulse can be scanned by a variable delay to a position close to the mean TOF. Thus spurious integrations due to background can be minimized.

Fig. 9 shows how the residual jitter on the relative time of flight can be restored to the value in darkness by reducing the time window interval. In this case, the RMS jitter can be restored to the value without ambient light level with a relatively coarse sampling window of 4ns which would be relatively easy to implement in an integrated circuit. Wider time windows cause a ceiling on the maximum jitter following the unwindowed jitter versus relative TOF curve. In Fig. 10, we see that a 4ns time window is also sufficient to restore the linearity of the converter. The choice of time window duration is related to the maximum tolerable background light level and desired linearity and output accuracy of the converter.

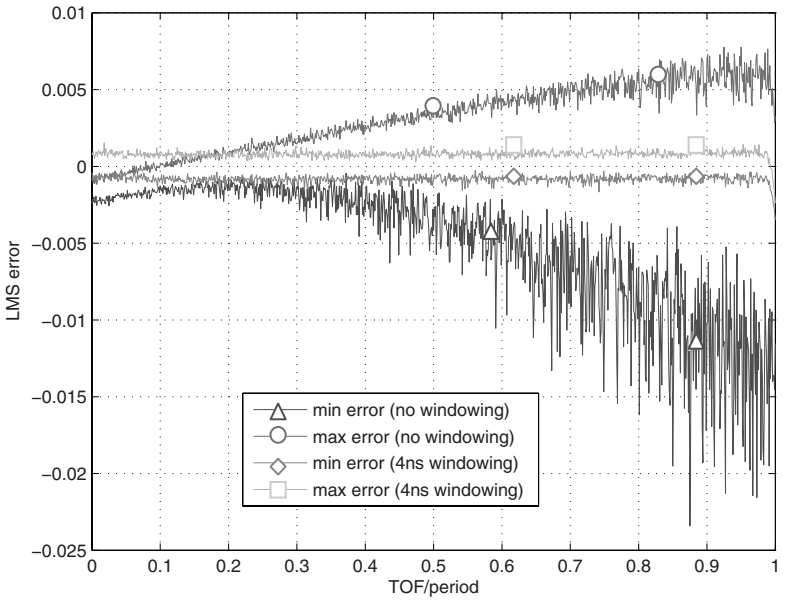

Fig. 10. Comparison of maximum and minimum linearity error of a 2nd order sigma-delta modulator versus TOF level for oversampling ratio 256, period 40ns, input jitter 300ps in the presence of 2Mphotons/sec background illumination level for windowed and unwindowed systems.

A 1st order sigma-delta TDC with a SPAD detector has recently been designed and sent for manufacture in a 0.35μm CMOS technology. The circuit occupies an area of

100um x 200um. This is relatively compact for a time-to-digital converter and promises miniaturized arrays of highly accurate time-estimators for time-resolved imagers.

7 Conclusions

Estimation of mean time-of-flight or decay time has been identified as an oversampled system. We have shown that sigma-delta converters provide a compact, efficient solution to achieve high time resolution, low jitter and reduced system IO bandwidth. A development of traditional sigma-delta converters has been proposed for low-light conditions or for suppression of high ambient light whereby the conversion cycles are event-driven. Simulations show that implementation of a narrow time window for event triggering is sufficient to reject ambient light and restore converter linearity and jitter. Circuit implementations of the trigger and event driven mechanism will be proposed in future work.

8 References

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