A VHDL-AMS Case Study:

The Incremental Design of an Efficient 3rd generation MOS Model of a Deep Sub Micron Transistor

C. Lallement, F. Pêcheux, Y. Hervé
ERM-PHASE, ENSPS, Pôle API, Bld. S. Brant, 67400 Illkirch, FRANCE

E-mail: {lallem,pecheux,herve}@erm1.u-strasbg.fr

Abstract: The paper presents an application of the VHDL-AMS formalism to state-of-the-art MOST simulation models. We present the principles, techniques and tools used to achieve the incremental implementation of an analytical third generation Spice transistor MOST model named EKV in VHDL-AMS, with relevant parameters set to match a deep submicron technology (gate length = 0.15 µm). The model includes the capacitances and resistors induced by the LDD structures as a function of gate voltage, and also considers thermo-electrical interactions between the transistor and its direct environment. Along with some considerations on the power of VHDL-AMS for modeling deep submicron devices, we give some examples of application of this innovative EKV MOS model.

1. INTRODUCTION

The design of innovative integrated devices, like MOEMS, involves a strong interaction of pluri-disciplinary objects on the same chip. These objects are tightly coupled by physical effects, and the corresponding exchanges can be modeled at various abstraction levels.

Our paper is an application of the innovative VHDL-AMS concepts to state-of-the-art MOS thermal-electronic simulation models. First, we present the principles, techniques and methodology used to achieve the design of an analytical third generation Spice transistor MOS model named EKV with

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The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: 10.1007/978-0-387-35597-9_40
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VHDL-AMS, with relevant parameters set [1] to match a deep submicron technology (gate length = 0.15 μm). Second, we add to this basic MOST model several characteristics specific to submicron technologies like the parasitic resistances and capacitances induced by the LDD structure. Third, we introduce the thermo-electronic interaction between the transistor and its environment and how it can simply be modeled in VHDL-AMS. Finally, we give some examples of application of the MOST model.

2. THE EKV MOSFET MODEL VERSION 2.6

In the historical evolution of the MOSFET compact models, The EKV MOST Model belongs to the third and last generation [2]. The main characteristics of this generation are [3]:

- the "original intent" to simplicity (in contrast to the second generation: BSIM, BSIM2, HSPL28),
- a small number of physically-based parameters,
- an improved mathematical conditioning,
- a single model equation for all regions of device operation,
- the use of smoothing functions

The major models of this third generation (BSIM3v3, BSIM4, MM9, EKV2.6 and soon EKV3.0 and MM11) are dedicated to sub- and deep-submicron device.

The most used model in the design community (BSIM3v3, BSIM4) has forgotten the "original intent" of simplicity, and a small number of parameters in contrast with the other models [2]; this can be explained by the BSIM 3-4 quest for "extreme" precision and the modeling of all small effects, thus resulting in a complex core. On the contrary, the EKV MOST model keeps maintaining a good simplicity/efficiently ratio.

The EPFL-EKV MOSFET is a scalable and compact simulation model built on fundamental physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current analog, and mixed analog-digital circuits using submicron CMOS technologies.

The EPFL EKV version 2.6 MOST model [4] is a charge-based compact model. It consistently describes effects on charges, transcapacitances, drain current and tranconductances in all regions of operation of the MOSFET transistor (weak, moderate, strong inversion) as well as conduction to saturation. The effects modeled in this model include all the essential effects present in submicron technologies. For quasi-static dynamic operation, both a charge-based model for the node charges and transcapacitances, and a simpler capacitances model are available.

2.1 The VHDL-AMS implementation

VHDL-AMS [5] is a language that allows the designer to describe mixed systems in the very same file. It has recently been chosen as the new IEEE standard for the modeling, the simulation, or the virtual prototyping of heterogeneous systems on a chip.

At the first order, writing the EKV MOST model in VHDL-AMS is a simple task, if we consider that any dynamic continuous model can easily be described as a set of simultaneous implicit or explicit differential algebraic equations (DAE). The VHDL-AMS analog solver is responsible for computing the values of the quantities such that the relationships hold (subject to tolerances), and the order of simultaneous statements does not matter. An example of VHDL-AMS implementation of a very simple EKV MOST model (case of a large n- MOST) can be found in [6].

2.2 VHDL-AMS Simulation results

All simulation results in VHDL-AMS included in this paper are made with a n-channel transistor of W/L = 1.5µm/0.15 µm, and with an p-channel transistor of W/L = 3.0µm/0.15 µm. The simulation environment is Anacad Advance AMS v1.1.

Figs. 1 to 2 present the MOST behavior in static mode in all regions of operation of the MOSFET transistor (weak, moderate, strong inversion) as well as conduction to saturation. Fig. 1 shows the drain current I_D (in log. and linear scale) vs. V_G characteristic for different V_S, from weak to strong inversion.

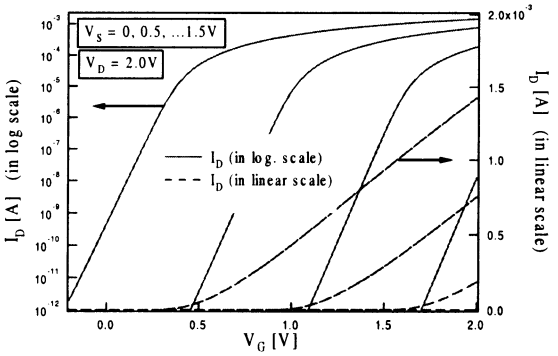

Figure 1. Simulation of the I_D versus V_G characteristic, for different source voltages.

Then, the I_D versus V_D characteristic for different V_G is shown in strong inversion in Fig. 2.

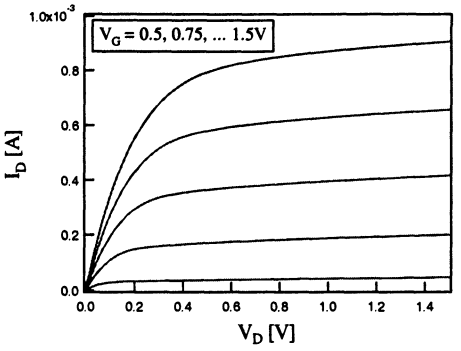

Figure 2. Simulation of the I_D versus V_D characteristic, for different gate voltages.

3. FEATURES SPECIFIC TO SUBMICRON

The LDD regions in the sub- and deep- submicron CMOS technologies introduce additional parasitic resistances between the source/drain electrode and the channel, as well as parasitic capacitances.

A problem with all these parasitic elements is their non-linear and bias dependent behavior. An efficient MOST model dedicated to deep-submicron design must imperatively take into account these elements. Equation (2), and Figs. 3-4 show some simple and accurate solutions to the modeling of the LDD region, and this with a few parameters (Table 1).

3.1 Series parasitic resistance

The source (or drain) resistance, *RSeff* (or *RDeff*), taking the LDD region into account can be defined as:

$$RSeff\ (or\ RDeff) = \frac{RS\ (or\ RD)}{1 + 0.5.\left[r + \sqrt{r^2 + 0.01}\right]} \qquad (2.a)$$

$$with \quad r = SVK.\left[(VG - VTOeff)/VK - 1\right] \qquad (2.b)$$

where *VTOeff* is the effective threshold voltage modified by bias and by the reverse short channel effect, and RS (RD) is the maximum resistance of source (drain). For design, one can define a layout-dependent model; so eq. 2.a. can be rewritten as:

$$RSeff = \frac{1}{Weff} \cdot \left[HDIF \cdot RSH0 + \frac{(LDIF + LD) \cdot RS0}{1 + 0.5 \cdot \left[r + \sqrt{r^2 + 0.01} \right]} \right] \quad (2.c)$$

where the definitions of *RSH0*, *LDIF*, *LD*, *HDIF* and *RS*, can be found in Fig. 3. W_{eff} is the effective width of the channel.

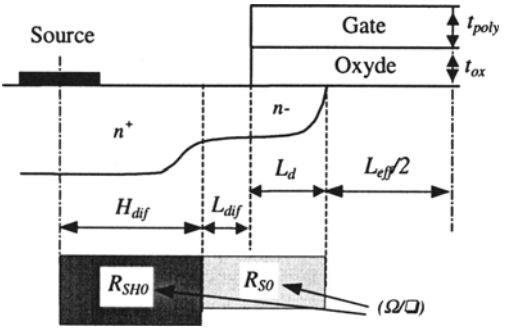

Figure 3. Definition of the resistive parameters in the LDD region.

3.2 The parasitic capacitances

The dynamic behavior of a MOST in deep submicron technology is strongly affected by its extrinsic capacitance formed by the overlap capacitance and the fringing capacitance (see Fig. 4). The fringing capacitance is constant, but the overlap capacitance is bias dependent. Its value is not equal to $C_{ov} = W_{eff} \cdot L_d \cdot C_{ox}$, but to $C_{ov\,eff} = W_{eff} \cdot L_{d\,eff} \cdot C_{ox}$.

C_{ox} is the oxide capacitance per area unit, and $L_{d\,eff}$ ($\leq L_d$) is a length essentially modulated by the bias.

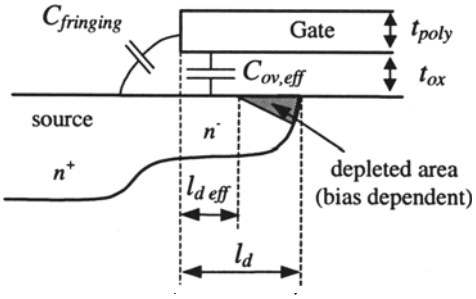

Figure 4. The parasitic capacitances in the LDD region (source or drain).

Purpose	Name	Description
Overlap Capacitance	LAMBDA	Overlap coefficient
	TPOLY	Polysilicon thickness
Series Parasitic Resistances	RS/RD	Total resistance at zero bias
	VK	Characteristic voltage
	SVK	LDD coefficient
	Optional	*parameters*
	HDIF	Path-length of the resistor in the heavily doped region (see fig. 3)
	LDIF	Partial path-length of the resistor in the LDD region (see fig. 3)
	LD	Gate underdiffusion (see fig. 3)
	RSH0 [in Ω/❑]	Sheet resistance (heavily doped region) at zero bias
	RS0/RD0 [in Ω/❑]	Sheet resistance (LDD region) at zero bias

Table 1. Parameters used to model the LDD regions.

3.3 Simulation results in VHDL-AMS

3.3.1 Series parasitic resistance (RS_{eff}, RD_{eff})

A typical characteristic of series parasitic resistance can be observed in Fig. 5, for two different drain bias.

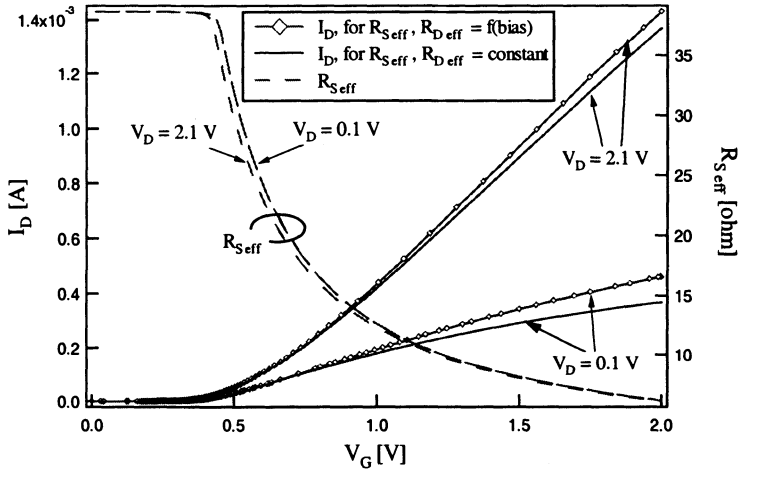

Figure 5. Simulation of I_D/R_{Seff} versus V_G characteristics for two drain bias.

Not taking into account the bias dependent of this resistance introduces some important errors on the drain current level, mainly for small V_D bias. These variations can considerably affect the parameters extraction procedures where, classically, channel length and series resistance are extracted altogether, at small V_D bias [7].

3.3.2 Parasitic capacitance

The parasitic capacitances represent a more and more important part of the global capacitance of the MOST (more 35% for a 0.15µm technology) as observed in Fig. 6, in the accumulation region. The influence of the fringing capacitance can be observed in the strong inversion region of Fig. 6; it represents the additional capacitance to COX (COX = W.L.Cox).

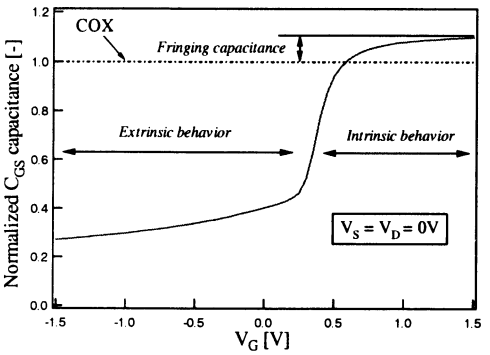

Figure 6. Simulation of the normalized global gate-source capacitance (C_{GS}/COX) [8].

4. THERMAL-ELECTRONIC MODELING

As the transistor size decreases, thermal interactions between devices on the same chip increase. These thermal effects are constantly amplified by the growing power density, and a failure in their estimation at an early development stage of the design often means extra costs and delays.

For the system designer, one of the major interest of VHDL-AMS is the simplicity with which models involving various physical domains (electronical, optical, mechanical, etc) can be interconnected. Along with the ability to describe hierarchical/multi-abstraction models, the power of VHDL-AMS relies on the fact that it allows the model designer to only detail the constitutive equations of the inner submodels. VHDL-AMS takes advantage of a graph-based conceptual description to automatically compute

the equations describing the conservative laws of the global model. The vertices of the graph represent effort nodes (**across** quantities like voltage, temperature or pressure) in the circuit, and the edges represent branches of the circuit through which information flows (**through** quantities like current, heat/liquid flow rate).

Thus, for the designer, the assembling of complex systems is nothing more than the connection of elementary objects through compatible terminals (ie, capable of exchanging informations), in such a way that the conservative semantics of the generalized Kirchoff laws are preserved at all points.

4.1 VHDL-AMS Electrical and thermal model

In the EKV MOST electrical model, several parameters are strongly dependent on temperature. Their respective temperature variation are taken into account by appropriate coefficients in the equations.

We model the heat diffusion through solid materials by sourcing dissipated power into a thermal RC network [9], which represents the material properties of the different layers. The temperature profile is the result of a heat flow in the thermal network.

In such networks, energy conservation states that the sum of all power contributions at a thermal node equals zero, and that the temperature at all terminals connected to a thermal node be identical. Thermal evolution of a system is thus ruled by the very same Kirchoff laws dictating the behavior of conservative systems : voltage becomes the across quantity temperature, and current becomes the through quantity heat flow.

VHDL-AMS provides an elegant solution to thermal-electronic interactions. Among the various packages provided with the simulation environment, the **thermal_system** package simply adds thermal capabilities to electrical models. The principle is to introduce a thermal terminal, with relative **through** and **across** quantities respectively bound to power and temperature.

The final EKV interface then becomes :

```
entity ekv1 is
    port (terminal d,g,s,b : electrical ;
          terminal j : thermal);
end;
```

with the following **quantity** relations :

```
quantity temp across power through j to thermal_ground ;
```

that define state variable **temp** as an extensive value, and **power** as the corresponding intensive value.

Using this electrical-thermal analogy, a thermal generator can simply be designed to model the ambient temperature with equation (3),

```
constant amb_temp: real := 300.0 ;
...
temp == amb_temp ;                    (3)
```

while thermal resistance and capacitance can respectively be described by equations (4) and (5).

```
temp == rth * power ;                 (4)
power == cth * temp'dot ;             (5)
```

Fig. 7 shows how thermal-electronic interactions between n-MOST and its direct environment can be modeled.

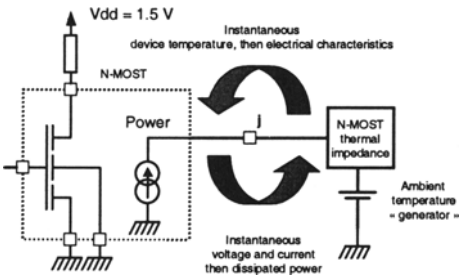

Figure 7. Modeling electro-thermal interactions.

4.2 VHDL-AMS simulation results

Electro-thermal simulations are given in Figs. 8-9, and Figs. 10-11.

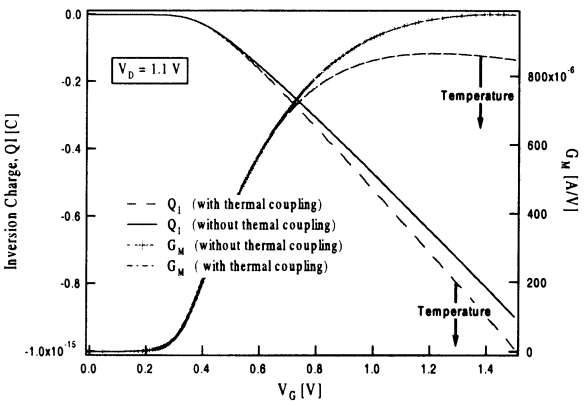

Figure 8. Characteristics of the inversion charge Q_I / transconductance G_m vs V_G.

The values of the capacitances and resistances of the thermal network have voluntarily been overstated This exaggeration increases the chip temperature of the n-transistor by more than 100°K in Figs. 8-9.

In Fig. 8, one can observe that a positive variation of the chip temperature of the n-transistor increases the inversion charge (QI), and downgrades the transconductance (G_M). Fig. 9 shows the output characteristic of the MOST.

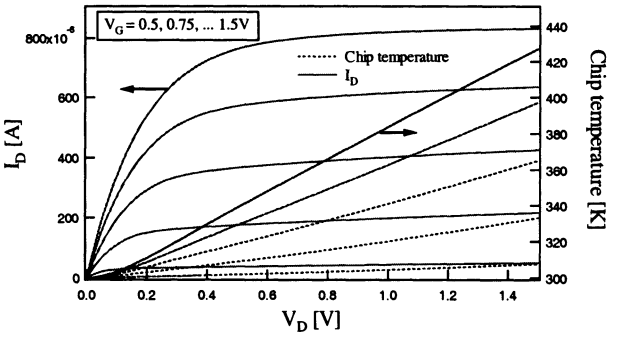

Figure 9. Simulation of the I_D / chip temperature versus V_D characteristics.

The I_D vs. V_D characteristic is downgraded with temperature variation in the chip compared to Fig. 2. obtained with the same electrical bias, but without thermo-electrical effect.

5. USING THE EKV MODEL IN VARIOUS DESIGNS

Fig. 10 presents an inverter design that validates the whole methodology.

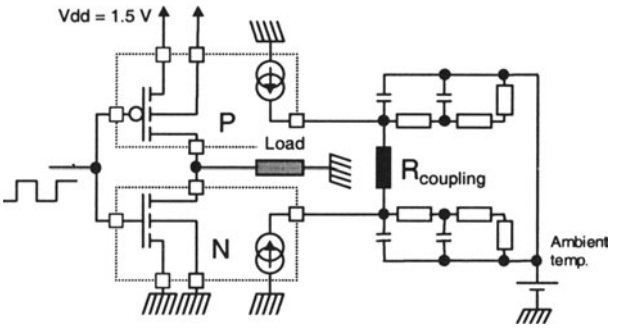

Figure 10. The inverter system, with RC network and thermal coupling.

The system details thermal coupling between the n-MOST and the p-MOST through **Rcoupling**. The inverter is excited by a squarewave stimulus and connected to a local thermal RC network. The two thermal networks represent the thermal constants of the various material layers.

For simulation purpose, as in §4.2. the values of the capacitances and resistances of the thermal network have voluntary been modified to point out the thermal effects.

Fig. 11 shows the temperature evolution in the inverter for two different values of **Rcoupling**. As expected, for a small value of **Rcoupling**, the temperature in the N and P transistors are tightly linked (dark curves in the figure). For a higher value, Fig. 11 shows the free temperature evolution of each transistor.

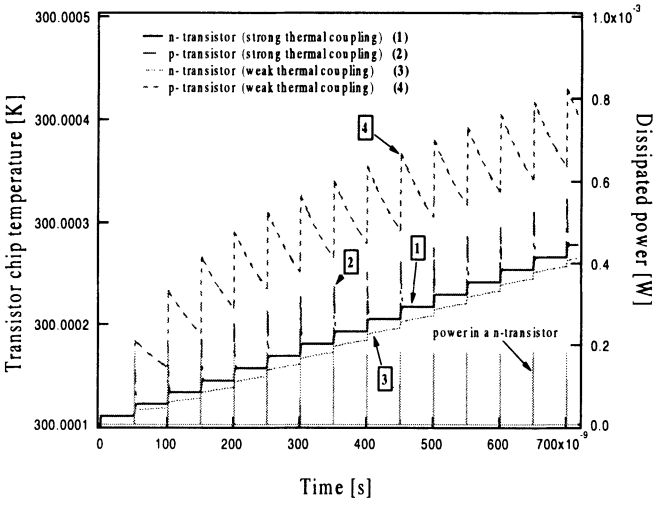

Figure 11. Simulation of the n/p - channel transistor chip temperature variation versus time during commutation (in an inverter), for two values of thermal coupling.

6. CONCLUSION

We are currently working on the VHDL-AMS release v.3 of the EKV model. It will notably include the quantum and polydepletion effects, and the NQS behavior [10]. This operational MOS transistor model can be seen as a possible starting point to simulate more complex structures. It is with such basic elements that VHDL-AMS provides optimal solutions to interconnect models of different domains, and the efficient modeling of MOEMS is almost within our grasp. For example, we have successfully instanciated the

EKV electrical model as a constitutive part of an analog opto-electrical system involving a light emitting diode and a photodiode [6] (both devices are very sensitive to temperature).

7. ACKNOWLEDGMENTS

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8. REFERENCES

[1] R. J. Baker: CMOS: Mixed-signal Circuit Design, Chap. 33. (http://cmosedu.com/cmos2/cmos2.htm).

[2] C. Lallement, F. Pêcheux, Y. Hervé, "A VHDL-AMS Case Study : The Incremental Design of an efficient of a 3rd generation MOS Model of a Deep Submicron Transistor", in Proc VLSI-SOC, pp. 467-472, Montpellier, France, Dec. 2001.

[3] D. Foty, *'MOSFET Modeling with SPICE - Principles and Practice'*, ISBN 0-13-227935-5

[4] M. Bucher, C. Lallement, C. Enz, F. Théodoloz, K. Krummenacher, "The EPFL-EKV MOSFET Model Equations for simulation, ver. 2.6", http://legwww.epfl.ch/ekv/.

[5] E. Christen, K. Bakalar, "VHDL-AMS-a hardware description language for analog and mixed-signal applications," *IEEE Trans. on Circuits and Systems, part II*, Vol. 46 Issue: 10, pp. 1263 –1272, Oct. 1999.

[6] C. Lallement, F. Pêcheux, Y. Hervé," *VHDL-AMS design of a MOST model including deep submicron and thermal-electronic effects*," 2001 IEEE Workshop BMAS 2001, Oct. 10-12, 2001, Santa Rosa, USA

[7] N. Arora, "Mosfet Models for VLSI Circuit Simulation: Theory and Practice, *Computational Microelectronics*, Springer Verlag, Wien New York, 1993.

[8] F. Pregaldiny, C. Lallement, D. Mathiot, *Paper Submitted to SSE.*

[9] C. Lallement, R. Bouchakour and T. Maurel, "One-dimensional Analytical Modeling of the VDMOS Transistor Taking Into Account the Thermoelectrical Interactions," *IEEE Transactions on Circuits and Systems, Part. I*, Vol. 44, N° 2, pp. 103-111, Feb. 1997.

[10] J. M. Sallese, et al, "Advancements in DC and RF Mosfet modeling with the EPFL-EKV charge based model," *8th Int. Conf. MIXDES*, Poland, pp. 45-52, 21-23 June 2001.