Moving MEMS into Mainstream Applications : The MEMSCAP Solution

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Abstract: This paper presents a fully integrated solution for the development of Micro Electro Mechanical Systems (MEMS) which covers component libraries, design tools and design methodologies which are used in conjunction with conventional design automation tools (EDA). This solution enables system houses in wireless and optical communications and consumer electronics markets to reduce their internal development costs and significantly accelerate their product development cycles.

1. INTRODUCTION

MEMS are the essential link between digital computation and the physical world. They enable the gathering of optical, electromagnetic, mechanical, acoustic, chemical, or thermal information and its conversion into digital data and also serve as the means for controlling the physical environment. Also, in many applications, MEMS serves as an enabling technology for implementing the required system functions in a compact, economical package.

The latest advances in MEMS technology have enabled the design of a new generation of electronic microsystems that are smaller, cheaper, more reliable, and consume less power. These integrated systems integrate numerous analog/mixed signal microelectronics blocks and MEMS functions

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The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: 10.1007/978-0-387-35498-9_57

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on a single chip or on two or more chips assembled within an integrated package. A major difficulty in designing these systems resides in the lack of information sharing between designers from different disciplines. With no common interface, such a separatist approach can result in catastrophe when prototype testing reveals a design flaw requiring additional iterations through the design and fabrication cycle. For example, none of the information derived from 3D field solvers on MEMS structures can be automatically transferred to an IC design tool. A secondary hurdle is enabling engineering teams to make full use of existing IP in MEMS. The ability to smoothly integrate cores into a system-on-silicon architecture provides system and IC designers with the latest functionality and process technology and dramatically reduces time-to-market. Until now, designers had to create MEMS by pushing polygons and understanding the fine details about the target fabrication process. Obviously, this approach demanded exceptional engineering skills and expanded design schedules and budgets. The MEMSCAP design environment and IP portfolio open up the playing field by capturing MEMS engineering knowledge to allow automation of MEMS-based designs among the extreme majority of engineers who do not push polygons. They also enable information sharing between system designers, IC designers, process engineers, and MEMS experts from various disciplines thereby reducing development time and cost.

2. A FULLY INTEGRATED SOLUTION

The interdisciplinary nature of MEMS and the significant expertise required to develop the technology has been a significant bottleneck in the timely design of new products incorporating MEMS technology. Until now, designers had to create MEMS by pushing polygons and understanding the fine details about the target fabrication process. Obviously, this approach demands exceptional engineering skills and expanded design schedules and budgets. In many cases it is difficult to justify the R&D investment of both time and money that is necessary to reap the benefits of MEMS technology. The approach used in the MEMS Engineering Kit is based on the following principles and features:

- Define two different flows: the component engineer and the system engineer,
- Ensure the link between the two flows,
- Provide to the system engineer an integrated solution enabling a seamless design flow from front-end to back-end,

- Enable the exchange of data between the different description level: the structural level (FEM/BEM), the system/behavioral level (HDL-A, VHDL-AMS, Verilog-AMS), the physical level (layout),
- Vehicle IP and provide design re-use capabilities.

The key elements of this design environment are a behavioral model to layout generator, a physical layout to 3D solid model translator, and a solid-model to behavioral model translator. These three tools in combination with existing design automation tools enable system designers, IC designers, process engineers, MEMS specialists, and packaging engineers to share critical design and process information in the language most relevant to each contributor. Before, none of the information derived from a given design tool could be automatically converted and transferred to another tool.

2.1 The MEMS Engineering Kit

The MEMS Engineering Kit is a new design paradigm that combines aspects of electronic design automation with mechanical, thermal, and fluidic computer-aided design. This Kit supports a wide range of advanced process technologies at leading MEMS foundries (e.g. MCNC/Cronos). The core software supports best of breed point tools and commonly used design environments (e.g. Mentor Graphics).

The environment contains elements for the device designer, enabling him to design modules, to simulate them, and finally to put the knowledge in the form of characterized standard cells in library. Commercially available optimization and yield management tools, such as OPSIM and ASPIRE have been extended to MEMS technology to enhance the work of the MEMS device engineers.

Figure 1 details the MEMS Engineering Kit design flow.

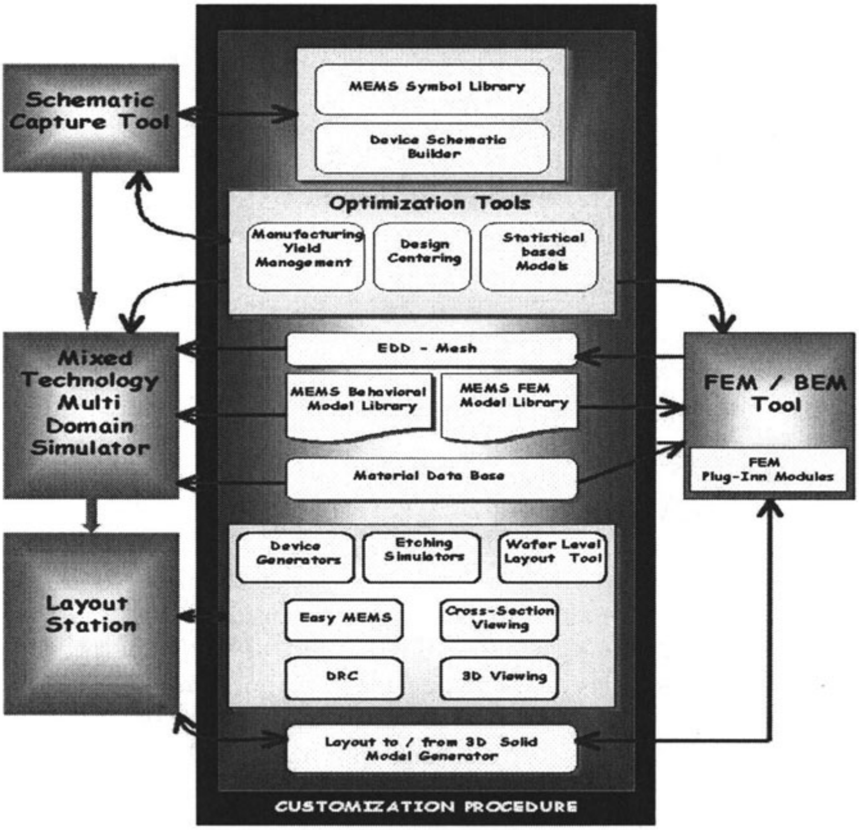

Fig.1. The MEMS Engineering Kit environment

The MEMSCAP MEMS Engineering Kit provides the following features:

- MEMS oriented schematic capture,
- a set of parameterized cells described at different levels (symbolic, behavioral, layout),
- optimization tools (Opsim) very useful for model development as well as specification parameter recycling,
- HDL-A code generator of non-linear behavioral models from lower level description,
- full verification of the design functionality (Continuum/Eldo/HDL-A),
- layout generators for mechanical structures, such as elementary structures (i.e. bridges, cantilevers, membranes, etc.) and application oriented structures coupled to the behavioral models, allowing the schematic driven layout feature,

- the layout generation of the whole MEMS (electronic and non-electronic parts) and a design rule verification,
- an extended design rule checker which can handle monolithic as well as hybrid designs,
- a multi-segment, multi-direction cross-section viewer,
- an anisotropic etching simulator for silicon and gallium arsenide as well as a sacrificial layer etching simulator,
- layout to 3D-solid model generator.

The concept of the environment is based on providing a fully integrated solution, easy to be used and reducing the development cycles of MEMS designs.

The MEMS Engineering Kit includes the Generic Kit and the Foundry Modules:

2.1.1 VULCAIN™ : The Generic Kit

The Generic MEMS Engineering Kit is a customizable design kit (includes a customization procedure to any process technology) and integrates existing third-party design tools (e.g. IC layout, circuit simulator, FEM field solver, etc.) into one common design environment.

Figure 2 shows a schematic capture for a torsional combdrive using building blocks. Each of these bricks encapsulate a behavioral model, written in HDL-A or in VHDL-AMS, making possible the simulation of this system.

A full system functionality can be verified, through a multi-level, mixed-mode, multi-domain behavioral simulation (figure 3). The system can be a MEMS component or a full system including the read-out electronics, whether it is integrated monolithically or in a hybrid assembly.

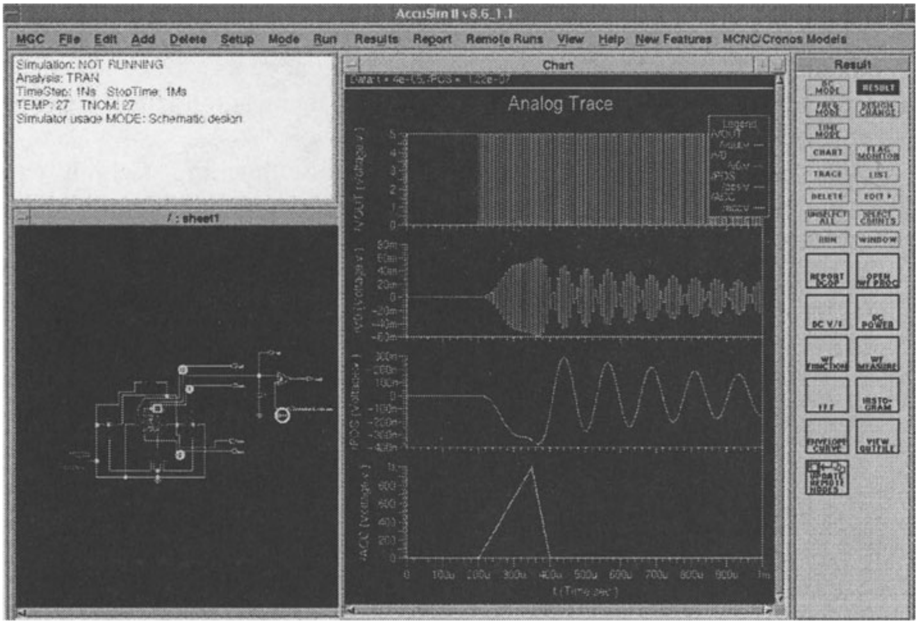

Fig.2. MEMS Oriented Schematic Capture

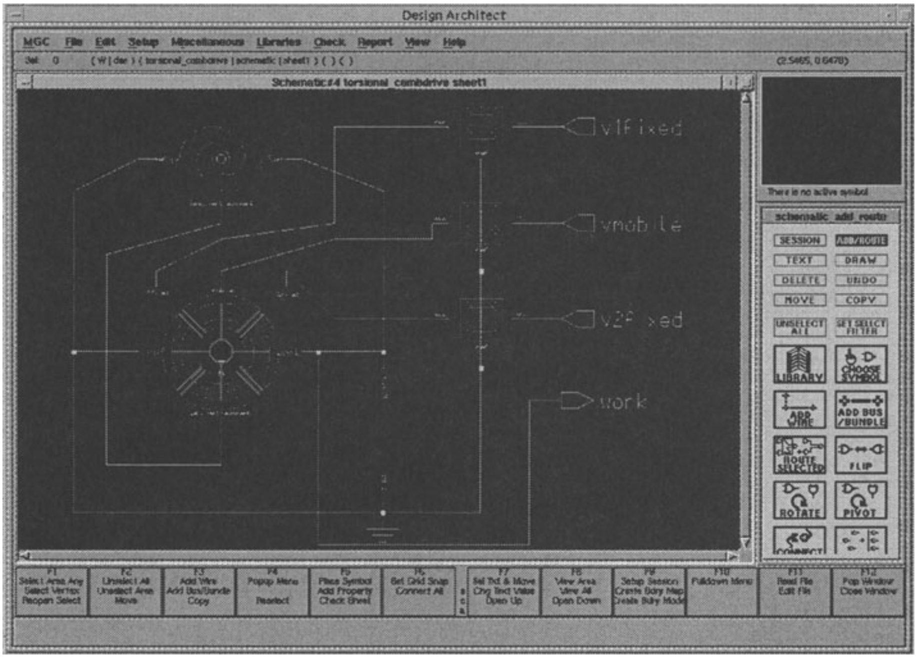

Fig.3. Multi-domain, multi-level, mixed-mode simulation

When simulation is done, the user can perform a schematic driven layout generation (SDL). In this operation, the device generators will consider the parameters fixed at the system level and map them automatically to the layout level keeping properties and connectivities.

Back-end operations, such as design rule checking (which can differentiate the MEMS rules from the electronics rules and verify them simultaneously), multi-segment, multi-angle, multi-direction cross-section viewer, and sacrificial or anisotropic etching simulation, can be realized (figure 4).

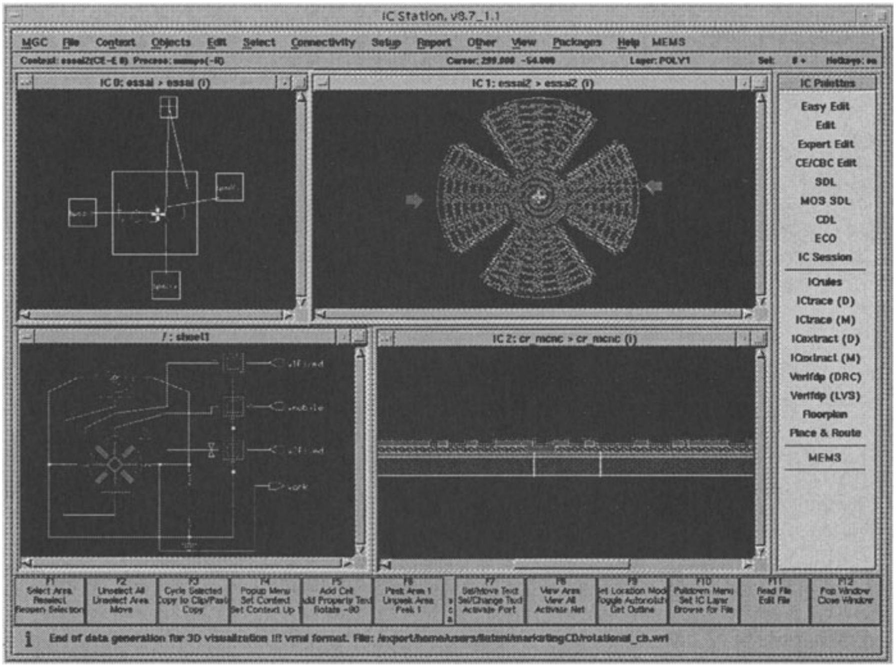

Fig.4. Back-end tools, such as cross-section viewer

This system flow is coupled to the component flow by ensuring the link with the field solvers, such as FEM or BEM tools. For this purpose, and in addition to the FEM/BEM to HDL-A translator described in the following sections, the kit includes a layout to 3D solid model generation which enable the generation of a selected layout area a 3D view (in VRML, or Geomview format) or a FEM input file (for ANSYS and very soon Coyote Systems). The user can select the layers he would like to consider in this generation or simply consider all the structuring layers. Figure 5 shows the 3D view of the torsional combdrive.

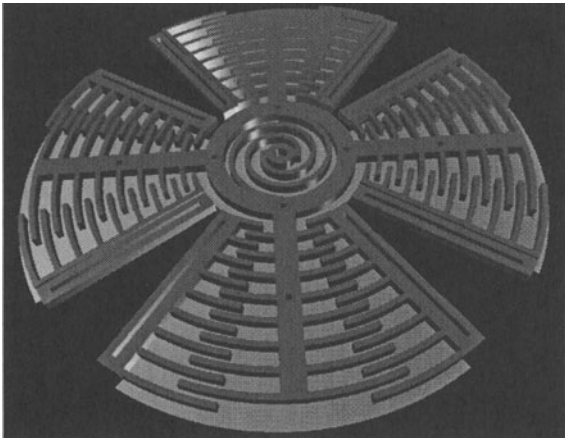

Fig.5. Layout to 3D Solid *Model* Generation

2.1.2 The Foundry Modules

A set of Foundry Specific Modules has been added in order to provide a "faster to fab" solution. In addition to the contents of a customized kit, a foundry specific module includes:

- DRC for the supported technology,
- Component Libraries

The Foundry Specific Modules currently includes, KanagaTM, the MCNC/Cronos Foundry Module. This module ensure a seamless design flow and includes a library of more than fully characterized 75 device generators manufacturable on the MCNC/Cronos production lines.

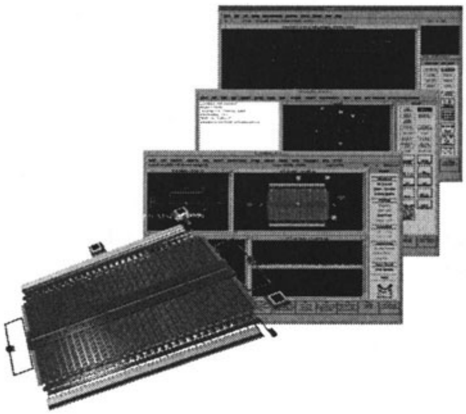

Fig.6. KanagaTM, the MCNC/Cronos Foundry Module, ensures a seamless design flow

2.2 Model Generation Tools: *Edd*^{TM}

Simulation of heterogeneous systems on the system level implies the simulation of the whole system and that of particular devices with a special emphasis on points of interests like functional behavior, timing, power consumption and so on. Simulation is very closely connected to modeling because only the system- or device-behavior can be simulated that has been taken into account while developing the models. Functional simulation of microelectromechanical systems (MEMS) and microcomponents can be done efficiently by using a single system description language suitable for a single mixed-mode simulator. The advent of analog HDLs such as HDL-A by Mentor Graphics and the future standard VHDL-AMS offer the possibility to create behavioral models of electrical and non-electrical devices without having the limitations of Spice. The expectations towards VHDL-AMS and commercial AHDLs are high: It is expected that these HDLs simplify the modeling as well as the simulation procedure of analog, analog/digital and other heterogeneous components.

AHDLs will find wide application in the domain of MEMS since modeling of nonlinearities is simplified and supported by almost all AHDLs. In practice, the creation of behavioral models for MEMS components causes several problems:

- The engineer responsible for creating the behavioral models needs excellent theoretical knowledge about the component as well as know-how about the simulation tools. It is difficult to find engineers who are experts in at least two engineering domains including the appropriate simulation tools.
- If the behavioral model is created using first order equations from theoretical work, the accuracy of this model may not be sufficient compared to the realistic 2/3D structural Finite-Element (FEM) model. Therefore often no verification of the behavioral model with regard to the structural 2/3D FEM model is done.
- There is no quantitative number for the accuracy of the behavioral model for other waveforms than the one used during the creation.
- The behavioral models have to obey certain standards concerning system-interfaces, generics etc. It is difficult to manage from the FEM-designers view.

A solution of this dilemma could be a tool that:

- Decouples the process of creating the behavioral model from the simulation process of the 2/3D FEM devices.
- Lowers the required knowledge of the AHDL for creating the behavioral model.

This tool (EddTM) enables the generation of non-linear dynamic behavioral and functional HDL-A models from models on a hierarchical lower level of abstraction (such as Finite-Element or transistor-level description) or measured data. The tool supports the efficient creation of nonlinear behavioral models in HDL-A without requiring deep knowledge of this AHDL. True HDL-A code is generated in a single architecture/entity-unit resulting in a faster simulation time than connected HDL-A models. It has been created as an interface between 2/3D-structural FEM-models and behavioral models in HDL-A (in that case the tool is integrated within the kit, and is called EddTM-Mesh), and it can also be applied for the generation of arbitrary behavioral models from lower level abstractions (e.g. such as analog or analog/digital Spice-descriptions. In that case, it is a stand-alone tool called EddTM-Net).

2.2.1 Edd™-Mesh : FEM/BEM to HDL-A Translator

This CAD-tool provides the following features:

- Simulation of the FEM-model.
- Fixed interface for checking in FEM-models in a CAD-library.
- Support of reuse of already created behavioral models in the library.
- Parameter optimization of the behavioral model.
- Differential adaptation of the behavioral model effects by comparing the waveforms of the FEM and the behavioral model and concluding the insertion or deletion of certain (nonlinear) effects.
- Support of model verification by using up to 10 different input stimuli.
- Check-in of the behavioral model in order to restart the model creation process.
- Creation of a single HDL-A Architecture/Entity pair that has a superior run time behavior than connected HDL-A models.

The basic idea for this CAD-tool is that the new behavioral model should be created in a differential way, i.e. starting with a relatively simple model the more complex one is created by adding missing and/or deleting obsolete effects until the resulting model satisfies a desired quality (the identity of I/O-waveforms for all possible input stimuli). Based on this idea, the tool uses a global optimization scheme, which can be subdivided in parameter and structural optimization. The lacks in the structure of the behavioral model are identified by operators, which are the arguments in a fuzzy-rule based environment for the representation of the knowledge concerning the used component. The basic algorithm is the following:

I. Select a start model from the database.
II. Select the input bitpattern which yields the worst costvalue (the worst correspondence between the real and the behavioral models).
III. Optimize the parammeters by applying simulation procedures (back to II if an internal counter has not exceeded a certain predefined value).
IV. If the targeted accuracy is not met, identify the lacks by operators and insert or delete a certain effect in the behavioral model. Back to II until an internal counter for the number of allowed structural optimizations has not exceeded a certain predefined value.

Figure 7 shows the structure of this CAD-tool in a detailed way.

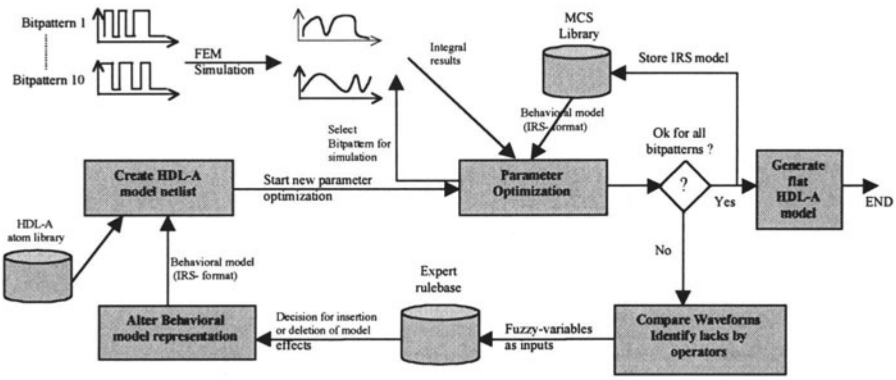

Fig.7. EddTM-Mesh Structure

It should be stressed that with the differential approach used here not all parameter values have to be optimized at each time, but special care may be spent on parameter values which are new (i.e. have been inserted in the last structural optimization step). It can be summarized that using this method more than 12 parameters can be optimized for a behavioral model.

Figure 8 shows the correspondence between the FEM model and the HDL-A generated model of an accelerometer.

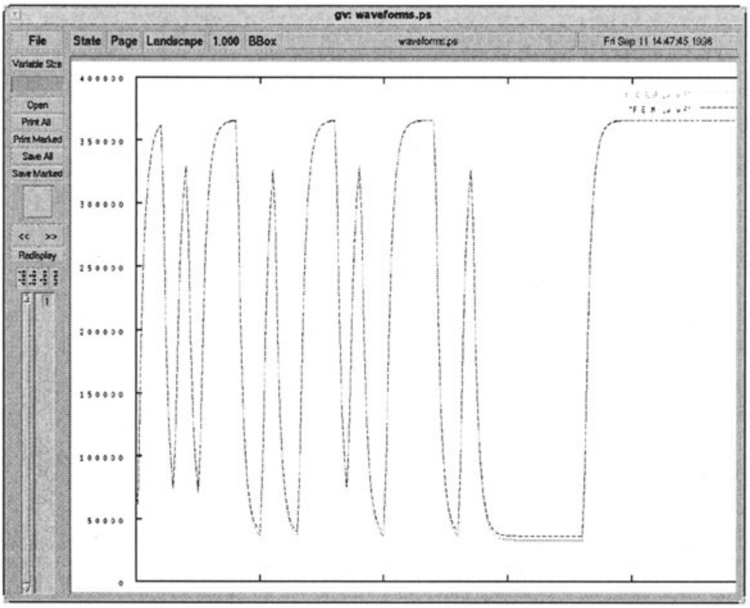

Fig.8. Correspondence between the FEM model and the HDL-A generated model of an accelerometer

3. CONCLUSION

This paper presents a design methodology and an integrated solution for the development of MEMS. It describes the whole design flow from front-end to back-end and details the related tools and functions integrated within a single environment. Finally, model generation tools and methodologies are also discussed and developed.

4. ACKNOWLEDGMENTS

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