A Design of Operational Amplifiers for Sigma Delta Modulators using 0.35um CMOS Process

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Abstract: An operational amplifier designed with 0.35um CMOS technology is presented. All the transistors are realized with minimum or near-minimum channel length. As the short channel length causes performance degradation, a proper operational amplifier structure is selected to compensate the performance degradation. The op amp is designed to meet the requirement of high-speed high-resolution sigma delta modulators. It has a folded-cascode first stage and a class-A output stage. It features a DC gain of 78dB, an open-loop unity-gain frequency of 266MHZ, a slew rate of 650V/us, and consumes 10.2mW from a +/-1.5V power supply. High level simulation is used to evaluate the OTA performance in sigma delta modulators.

1. INTRODUCTION

The fast development of CMOS process technique makes it possible to integrate more and more functions into a single Digital-signal-Processing chip. However, the physical signal (which is analog) still needs an interface to be handled by DSP. A/D and D/A converters are such interfaces. In the area of high resolution A/D conversion, sigma delta converters are the best choice. They adopt oversampling and noise shaping technology to move the quantization noise out of signal band, and then digitally low-pass filter the shaped noise. From the middle of 80s they have been widely used in digital audio applications. The biggest drawback of sigma delta modulators is that they can not convert wide band signals as their counterpart, flash A/D

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converter can do. The resolution of a sigma delta modulator (in bit, or dB) is nearly linearly proportional to the oversampling ratio. Thus to achieve high resolution the modulator must work at a sampling frequency that is much higher than the signal band. With a signal band of 1MHz and oversampling ratio of 16 (which is already relatively low), the modulator must sample at 32MHz. Many researches have been done to increase the signal band that can be converted by sigma delta modulators [1,2], and obviously that the essential task is to design a high performance operational amplifier which is used in switch capacitor integrators. The amplifier should have a high DC gain, large bandwidth, large slew rate (driving capability) and large output swing.

Although CMOS process has already stepped into deep submicrometer, the analog transistors are still often designed with much larger channel length than in digital circuits. One of the reasons is that using small channel length transistor will degrade the performance. For example, Rds, the drain-source resistance of a NMOS transistor in small-signal model will reduce according to the left formula due to channel-length modulation. And the short-channel effects will make things even worse. It is obvious that Rds will decrease when the channel length L decreases, even though the Width/Length ratio keeps the same. When Vds is so big that short-channel effect become apparent, Rds will reduce even faster than predicted by the above formula. Figure 1 shows the simulated Rds of a NMOS transistor in AMS 0.35um process [3]. The transistor has a fixed Width/Length ratio (5:1) and fixed V_{eff} (V_{gs}-V_{tn}) while the value of length changes from 0.4um to 5um. The maximum Rds in active regions is plotted against the channel length. Note that in an operational amplifier Rds is directly related to the DC gain. Figure 2 shows this simulation for a simple common-source gain stage with an active load (T2). The bias current and Width/Length ratio of each transistor are fixed, while the absolute value of the channel length is varied. The gain of this stage is changed accordingly. So using a short channel length transistor will automatically degrade the DC gain unless otherwise compensated. This compensation can be done on the structure level, for example, by changing a single stage to a two-stage structure. With a proper design, analog circuit can also take the advantage of advanced CMOS process without sacrificing performance.

$$Rds = \frac{2L}{\lambda \mu_n C_{ox} W (V_{gs}-V_{tn})^2}$$

where

$$\lambda = \frac{k_{ds}}{2L(V_{ds}-V_{eff}+\Phi_0)^{1.2}}$$

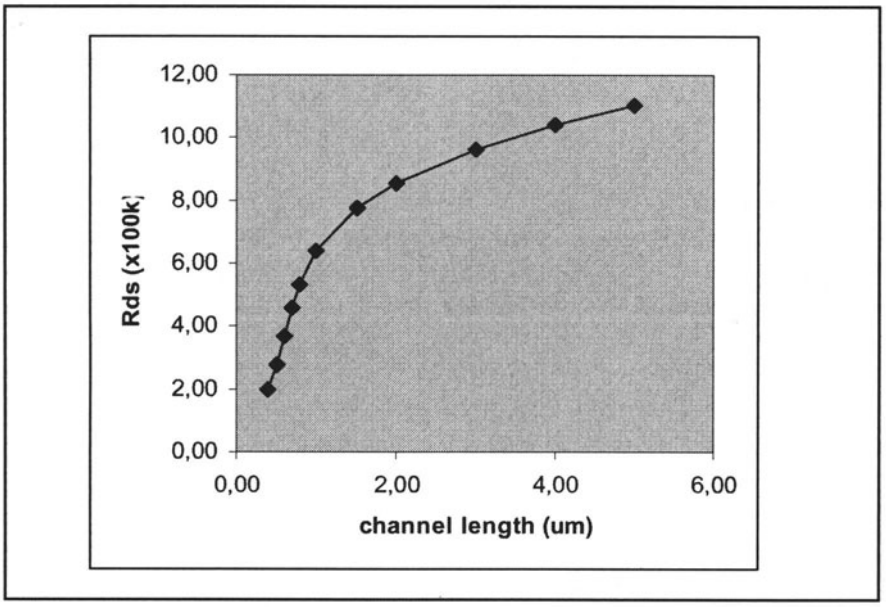

Figure 1. Rds of a NMOS with different channel lengths

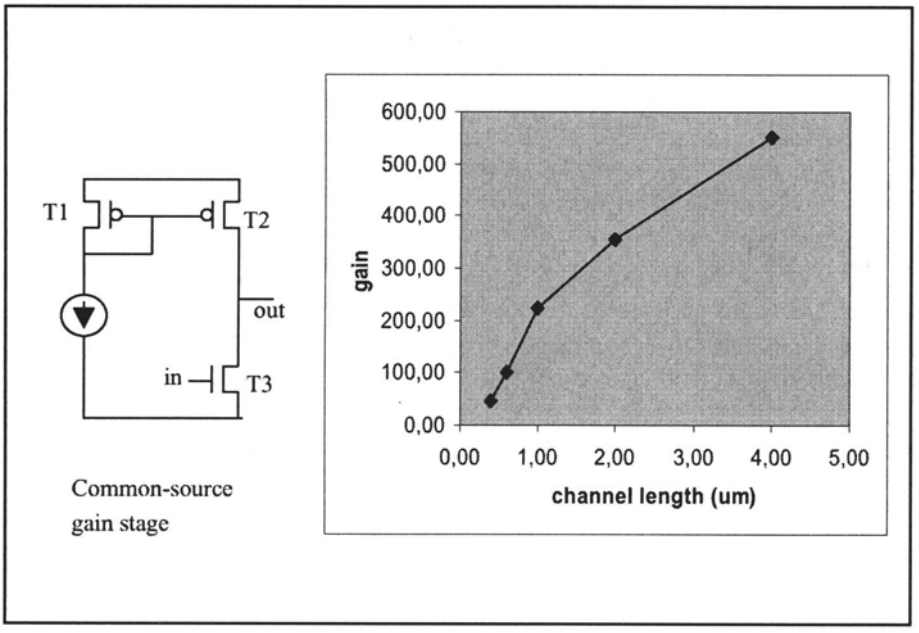

Figure 2. Gain of a common-source stage with different channel lengths

2. DESIGN TARGETS AND STRUCTURE SELECTION

The target is to design an operational amplifier for sigma delta modulators that can work at a sampling frequency above 40MHz. With high level simulation of sigma delta modulators this requirement of the modulator can be translated into several requirements of the amplifier [1], for example, the DC gain, the open loop cut-off frequency, the slew rate, the phase margin and so on.

As the amplifier will be used in switch capacitor circuits, the load is only capacitive (no resistance load). Thus the so-called Operational Transconductance Amplifier (OTA) is a good choice (output buffer stage is omitted). Folded-cascode OTA has been used extensively in switch capacitor circuits. It has the advantages of high DC gain, large output swing, large bandwidth and simple structure. Therefore it has been used successfully in many high-speed high-resolution sigma delta modulators [4]. However, to have a large bandwidth and large slew rate many of the transistors in OTA need to have very large transconductance, which also means large Width/Length ratio. This increases the die area and parasitics. If a short channel length, e.g. 0.35um, can be used to implement these transistors, we can reduce the chip size and the parasitics as well. However as mentioned before, using short channel length transistors will degrade the performance. So here a two-stage OTA [5] is selected as shown in figure 3. The inner stage is a traditional folded-cascode amplifier while the outer stage is a class-A stage. The OTA is designed using AMS 0.35um process. All the transistors have minimum or near-minimum channel length. With the addition of the second stage, the requirement of the first stage can be largely loosen, thus the transistor Width/Length ratio and bias current can be reduced. The class-A second stage provides large drive capability (slew rate) and large output swing (near rail-to-rail). As a result, it is possible to achieve higher overall performance while consumes less power and has smaller die area (compared with the single-stage folded-cascode implementation with large channel length). The other attractive advantage of this circuit is that it can work with very low operating voltage. With the careful arrangement of transistor sizes and bias currents, it can work well with 1.5V power supply [5]. This makes it a candidate circuit for future processes that require lower supply voltages.

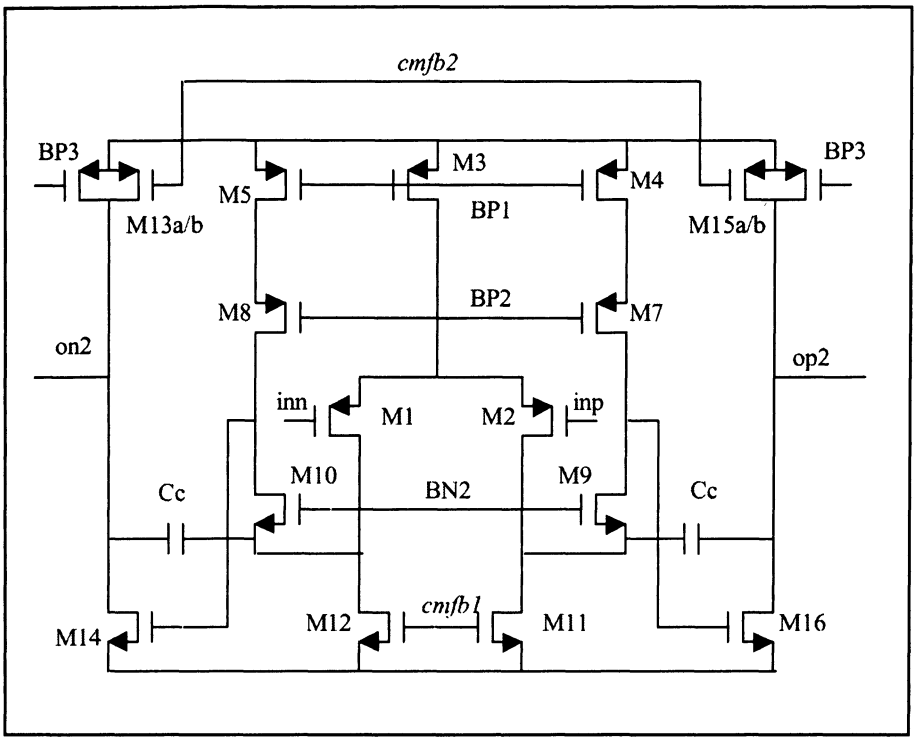

Figure 3. Two-stage OTA with folded-cascode inner stage and class-A outer stage

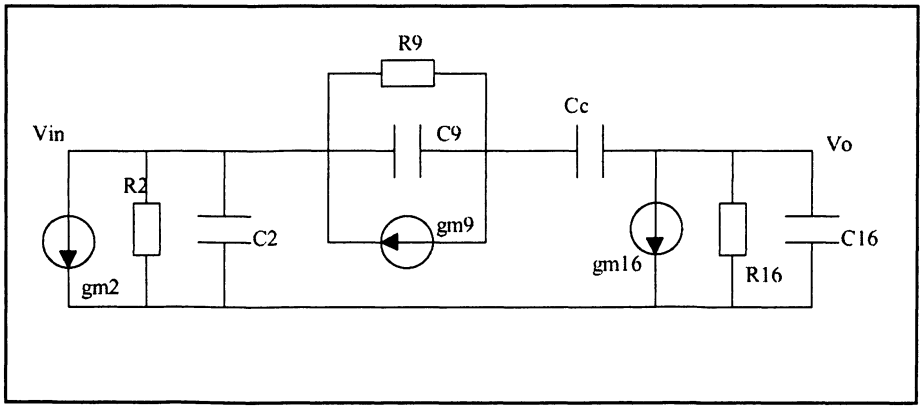

Figure 4. Simplified small signal model for differential half circuit

3. CIRCUIT ANALYSIS

3.1 DC Gain

In a sigma delta modulator the finite DC gain of the operational amplifier will cause integrator leakage [6,7], which degrades the overall performance, especially in cascaded modulators. To implement a high-resolution modulator, the DC gain should be made above 60dB. In CMOS Op amp it is conflicting to achieve both a high gain and large slew rate. A high gain requires small bias current while a large slew rate requires a large bias current. In this two-stage structure the first stage can be biased at a relatively small current to have a large gain, and the second stage be biased at large current to achieve large slew rate. The first folded-cascode stage has a DC gain in the order of $(g_m r_o)^2$, and the second class-A stage has a DC gain in the order of $g_m r_o$. So the total DC gain is in the order of $(g_m r_o)^3$. This makes it easy to achieve a DC gain of 1000 or higher.

3.2 Slew Rate

In a high-speed sigma delta modulator, the OTA slew rate must be large enough to guarantee that the output signal is accurately settled within a very short period (less than half of a clock period). Some empirical formulas can be used as a guideline to find the needed slew rate for a specific application. For example, "Slew Rate>7*Vref*fs", which is derived from high-level simulations [1]. The slew rate of the first stage is defined by the bias current in M1, M2 and their load capacitance (include compensation capacitor). The bias current of M14, M16 and the output load capacitance define the slew rate of the second stage. The overall slew rate is limited by either the first stage or the second stage, whichever is slower. If the first stage is designed to be fast enough the slew rate is defined by the bias current of the second stage and its load capacitance. The proper bias current can be found through SPICE simulation.

3.3 Frequency Response and Compensation

The first stage's frequency compensation is realised by cascode compensation capacitor Cc. Compared with standard Miller compensation, it has much better PWRR at high frequency and reduced capacitance load to the first stage. It is first introduced in [8] and then widely used in many designs [9,10]. The simplified ac small-signal model for the differential half circuit is shown in figure 4. With some reasonable assumption, the OTA can be modelled as a 3-pole 2-zero system. The first pole is formed by the input

transistors M1 and M2, so their g_m (g_{m2} in figure 3) should be big enough to move the first pole to higher frequency. The distance between the second and third pole is determined by the value of Cc. With a large Cc, these two poles are moved further away from each other. This is the so-called pole-splitting effect. However Cc also introduces a zero on positive real axis which will reduce the phase margin unless it is put far away from cut-off frequency. The proper value of Cc can be found through hand calculation of the simplified ac small-signal model, and then be verified through simulation. And it is worth mentioning that to have enough phase margin, the g_m of M9, M10 (g_{m9} in figure 4) and M14, M16 (g_{m16} in figure 4) should be much larger than that of M1 or M2.

3.4 Bias Circuit

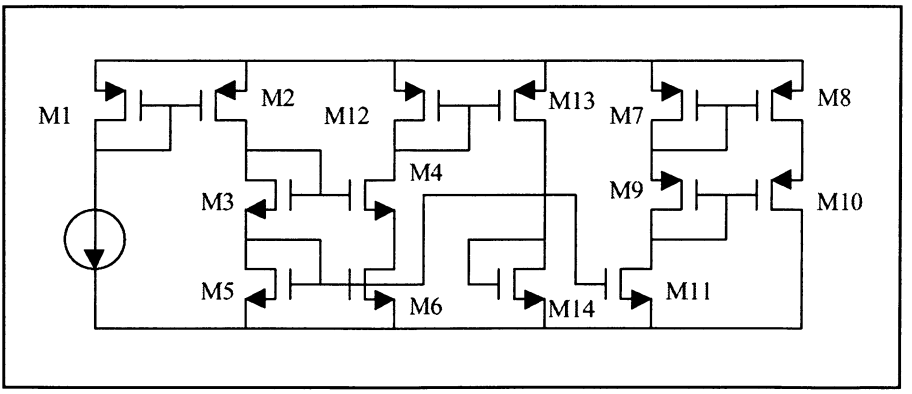

Figure 5. Bias circuit of OTA

The bias circuit of the OTA is shown in figure 5. It provides proper bias current for both PMOS and NMOS transistors. It also includes a duplicate of class-A output stage (MB13 and MB14) to establish its common-mode input voltage which is used in the first common-mode feedback circuit.

3.5 Common-mode Feedback

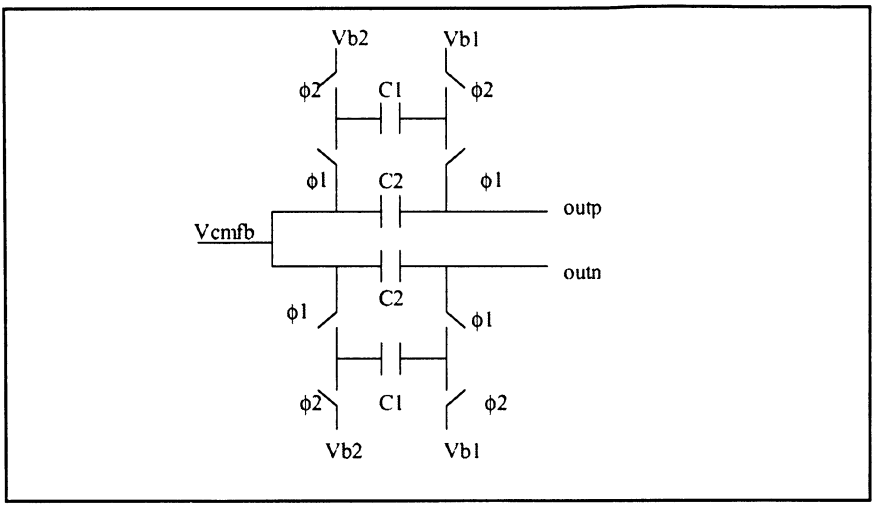

Figure 6. Switch capacitor common-mode feedback circuit

The control of common-mode output voltage is more difficult than in the folded-cascode OTA because there are two independent stages. Some designs use a single common-mode-feed-back (CMFB) circuit [2], where the common-mode voltage of the second stage is sensed and then put through a sign inversion circuit (often a current mirror, which consumes extra power) to control the bias in the first stage. In this implementation we use two separate CMFB circuits. With this scheme, we can accurately control the common-mode output voltage of the first stage to be the required input bias voltage of the class-A second stage [11]. The second stage's common-mode output voltage is set to be the middle of power suppliers. In this way the common-mode voltages of both stages can be fast and accurately controlled. The two switch-capacitor CMFB circuits are identical and shown in figure 6. They are suitable for switch-capacitor circuits and consume much less power than continuous CMFB circuits.

4. OTA PERFORMANCE SIMULATION

Figure 7 shows the simulated transient response and frequency response. In both cases each output terminal is loaded with 2pF capacitor. The slew rate is found to be 650v/us. The DC gain is 79dB, which is enough to meet the requirement of a high-resolution sigma delta modulator. The cut-off frequency is about 266MHz and the phase margin is 44 degree. Power

consumption is 10.2mW (not include the bias circuit) with +/- 1.5V power supply.

5. HIGH LEVEL MODULATOR SIMULATION WITH OTA NON-IDEALITIES

Once the OTA characteristic is extracted, it can be put through high-level sigma-delta modulator simulations. Figure 8 Shows a 5th order single-stage single-bit modulator optimised for OSR=64 [12]. A full SPICE level simulation of such a modulator is too time-consuming and often leads to inaccurate results. High level simulation (e.g. based on MATLAB) is therefore often adopted to efficiently evaluate the performance. To make this kind of simulation accurate enough to be useful, we must consider non-idealities in the component model. It is known that in a sigma-delta modulator only the first integrator's non-ideality has dominant influence on the overall performance [12]. Thus in high level simulations only the first integrator needs to be modelled with non-idealities, while all other components can be modelled as ideal. The non-idealities include kT/C noise, OTA noise, clock jitter, OTA slew rate, bandwidth and limited DC gain. The modelling of these non-idealities is described in [13]. The effect of clock jitter in sigma delta modulator can be simplified as its effect on the input signal sampling. The kT/C noise and OTA internal noise can be modelled as an input-referred random noise. The effect of finite DC gain can be modelled as a modification on integrator transfer function. The finite bandwidth and slew rate can be modelled with some form of non-linear integrator gain. The simulation uses a sampling frequency of 40MHz, and the signal band is 312.5KHz (OSR=64). It achieves a SNDR of 92.3dB (figure 9). Compared with the ideal case which has a SNDR of 110 dB (figure 10), about 18 dB SNDR is lost. This means the noise power caused by integrator non-idealities is about 10 time larger than the pure quantization noise. The kT/C noise contributes most to this 18dB SNDR lost (with only kT/C noise, the SNDR will reduce to 96dB), while the OTA non-idealities contributes much less.

6. CONCLUSIONS

In analog circuits which need large Width/Length ratio transistors (e.g. Op amp) we can consider using very short channel length transistors. With a proper design, the circuit can maintain its performance while having a

smaller die area and less parasitics. An OTA is designed in such a way for high-speed high-resolution sigma delta modulators. Its high performance makes it capable to work at a sampling frequency of 40MHz or more.

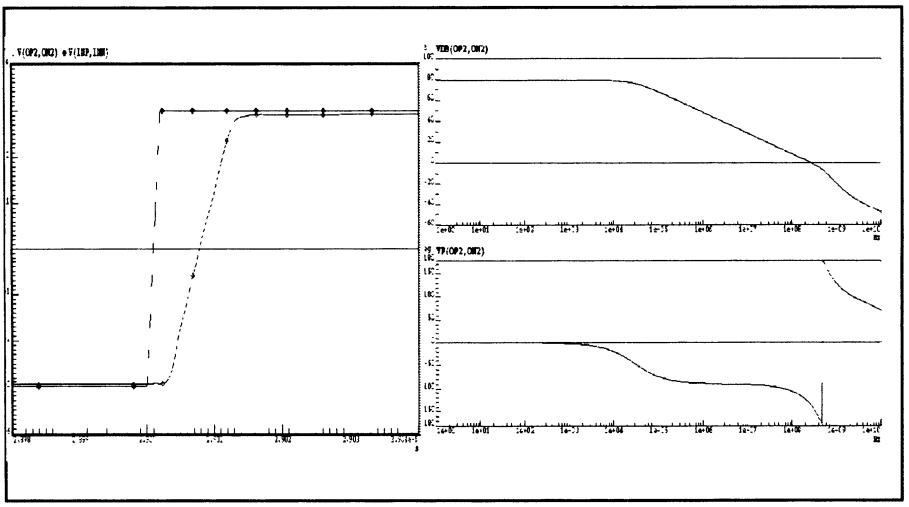

Figure 7. Transient response and frequency response of OTA

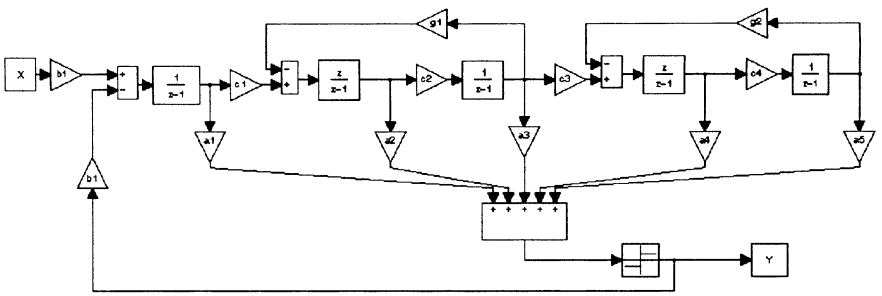

Figure 8. A 5th order single-stage single-bit sigma delta modulator (The coefficients are optimised for OSR=64. a1=0.5734; a2=0.5279; a3=0.4495; a4=0.2588; a5=0.2620; g1=0.0032; g2=0.0375; b1=0.8711; c1=0.4087; c2=0.2200; c3=0.2264; c4=0.0528)

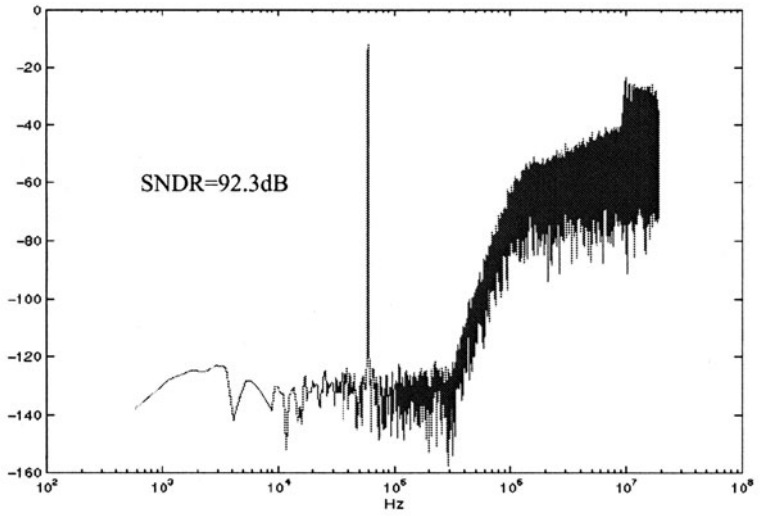

Figure 9. PSD of modulator output with first integrator's non-idealities included

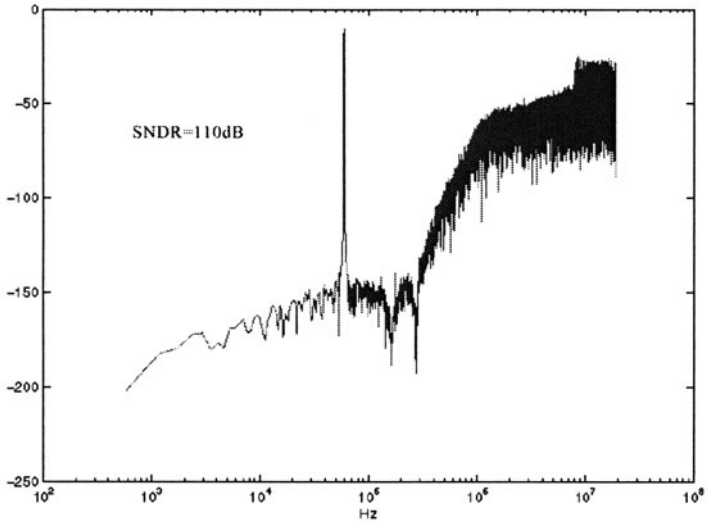

Figure 10. PSD of modulator output with all the components treated as ideal

7 REFERENCES

[1] A. M. Marques, V. Peluso, M. S. J. Steyaert and W. Sansen, "A 15-b Resolution 2-MHz Nyquist Rate DS ADC in a 1-um CMOS Technology", *IEEE J. Solid-State Circuits*, vol. 33, Jul. 1998, pp. 1065--75

[2] A. R. Feldman, B. E. Boser and P. Gray, "A 13-bit, 1.4-MS/s Sigma-Delta Modulator for RF Baseband Channel Applications", *IEEE J. Solid-State Circuits*, vol. 33, Oct. 1998, pp. 1462--69

[3] http://www.ams.co.at/corporate/profile.html

[4] S. Ingalsuo, T. Ritoniemi & H. Tenhunen, "New Differential Amplifier for High Speed Switched Capacitor Circuits", *in proc. of European Conference on Circuit Theory and Design (ECCTD-91)*, Copenhagen, Denmark, September 1991.

[5] A. M. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter", *IEEE J. Solid-State Circuits*, vol. 34, May. 1999, pp. 599--606

[6] S. R. Northworthy, R. Schreier and G. C. Temes, *Delta -Sigma Data Converters, Theory, Design, and Simulation*, IEEE press, 1997

[7] B. E. Boser and B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters", *IEEE J. Solid-State Circuits*, vol. SC-23 Dec. 1988, pp. 1298--1308

[8] B. K. Ahuja, "An improved Frequency Compensation Technique for CMOS Operational Amplifier", *IEEE J. Solid-State Circuits*, vol. SC-18, Dec. 1983, pp. 629--633

[9] D. B. Ribner and M. A. Copeland, "Design Techniques for Cascoded CMOS Op Amps with Improved PSRR and Common-Mode Input Range", *IEEE J. Solid-State Circuits*, vol. sc-19, Dec. 1984, pp. 919--625

[10] K. Nakamura, M. Hotta, L. R. Carley and D. J. Allstot, "An 85 mW, 10b, 40 Msample/s CMOS Parallel-Pipelined ADC", *IEEE J. Solid-State Circuits*, vol. 30, Mar. 1995, pp. 173--183

[11] S. Rabii and B. A. Wooley, *The Design of Low-Voltage, Low-Power Sigma-Delta Modulators*, Kluwer Academic Publishers, 1999

[12] B.X. Li and H. Tenhunen, "Hierarchical Modeling of Sigma Delta Modulators for Noise Coupling Analysis", *in proc. of 1999 Southwest Symposium on Mixed-Signal Design*, Apr., 1999, pp. 58-62

[13] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto and F. Maloberti, "Modeling Sigma-Delta Modulator Non-idealities in Simulink", *in proc. of IEEE International Symposium on Circuits and Systems*, May, 1999, pp. II 384-387