An Analog Non-Volatile Storage System for Audio Signals with Signal Conditioning for Mobile Communication Devices.

Geoffrey B. Jackson, Saleel V. Awsare, Lawrence D. Engh, Mark A Hemming, Peter Holzmann, Oliver C. Kao, Chun Mai-Liu, Carl R. Palmer, Aditya Raina

Storage Devices, A Winbond Company, 2727 North.First Street, San Jose, CA 95134, USA

Key words: Mobile Communications, Multi Level Storage (MLS), Configurable System

Abstract: Presented is a system on a chip for conditioning of voiceband analog audio signals for use in mobile communication devices. The system allows for direct interface to acoustic transducer elements and provides signal conditioning to gain adjust, multiplex, filter and mix two independent signals. The system can record these processed signals as analog samples in a non-volatile flash EEPROM array for later retrieval. Control of the system is achieved via a serial interface, which is used to configure and control the device. All necessary components of the system are provided on chip including analog processing elements, non-volatile storage and high voltage and reference generation.

1. INTRODUCTION

In any mobile communication system (e.g. cellular telephony)(Fig.1), it is indispensable to have the ability to process two streams of information; namely upstream (information from the local user to the remote caller) and downstream (information from the remote caller to the local user). Other desirable features in a mobile communication environment include a voice

The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: 10.1007/978-0-387-35498-9_57

L. M. Silveira et al. (eds.), *VLSI: Systems on a Chip*

memo function, full-duplex voice record and playback, answering machine and call screening functions. Also, minimum external components and low power consumption are vital. This paper describes a system on a chip solution capable of processing and storing voice-band signals while incorporating all of these aforementioned features. By inserting itself between the baseband module of a cell phone and the acoustic transducers, this unique system on a chip can perform the analog processes of several chips thereby enhancing system level integration.

2. CHIP ARCHITECTURE

The chip is divided into three parts (Fig. 8). The top section contains the high voltage circuits needed to program the flash cells along with the digital logic needed for the SPI interface, chip control and timing generation. The middle section consists of the array, column drivers, and row decoders. The column drivers include analog sample and hold circuits along with analog comparators to perform the analog non-volatile storage algorithm. The bottom section consists of the analog signal paths and associated signal conditioning circuits and the reference generation circuits. Three separate power buses are used for isolating noise, one for high voltage generation circuits, one to supply digital logic and a third for the analog section. The chip runs from a 2.7V-3.3V supply and incorporates programmable power down control to minimise power consumption in all modes

2.1 Memory Array and Operations

A 0.6um two poly source-side injection (SSI) cell (Fig. 2) is the basic unit of the memory array. The flash cells are arranged in an array of bit lines (Fig 5), word lines and common source lines shared by adjacent rows This memory cell consists of a select gate (SG) transistor and a floating gate (FG) transistor merged in a split-gate configuration. There are three terminals–the common source (CS), which accesses from the FG-transistor side, the drain, which accesses from the SG-transistor side and the select gate (SG). The memory array is organised in a NOR architecture, where the select gates form the word lines, the drains are strapped by first metal to form the bit lines and the common source lines, parallel to the word lines are strapped by second metal. The programming voltage is coupled to floating gate via CS diffusion to FG overlap. Hot carriers from the channel current promote impact ionisation on the source-side of the FG transistor provide efficient cell programming. Poly to poly electron tunneling erases the cell. Refer to

Table 1 for the conditions applied to the memory cell during a Read, Program and Erase operation.

2.2 Algorithm and Programming Characteristics

To write an analog sample from the sample and hold circuits to the memory cell, a writing algorithm is used. The writing algorithm is based on a closed loop iterative program and verify cycle. The cell is first erased and then subjected to a train of programming pulses applied to the common source node as illustrated in (Fig. 3a). A column is selected by sinking the appropriate programming current from the bit line as illustrated in (Fig. 3b). After each programming pulse, the cells are read back and compared to the voltage of sample and hold, capacitor. When the desired value is reached the bit line current sink is disabled barring further programming. This programming algorithm is made practical to achieve a large cell window for stored signals,. The variations of memory cells from wafer to wafer and lot to lot further reduce such window as illustrated in (Fig. 3c).

2.3 The S/H and the Writing Circuits

Once the signal has been sampled onto the sample and hold capacitors, the samples are programmed into the memory cells in parallel; hence there are multiple sample and hold (S/H) circuits on the system. This allows the actual programming of the memory cell to take much longer than the sampling time. The samples will be held and used by the writing circuit. The sample and hold circuit is shown in (Fig. 4). This S/H circuit can be connected to a unit gain operational amplifier (Op Amp), which is common to all the other S/H circuits. The 'select' signal determines which S/H will be connected. When the S/H is disconnected, the analog input sample can be retrieved from the source node of a native NMOS transistor. This voltage will then be used to program the memory cell. The signal 'bank select' connects either 'bank A' or 'bank B' of the S/H circuits. There are two banks of S/H circuits. While programming the samples of one bank the other bank can be loaded with new samples. Therefore, programming the memory array is a non-stop operation. (Fig. 5) shows how the S/H circuit including the two banks is connected to the writing circuit. During programming, a common source node and a select gate node in the memory array are selected by the 'Xdecoder'. The 'Waveshaper' and the high voltage 'Driver' supply the waveform as shown in (Fig. 3). This waveform is applied to the selected common source node. During each programming cycle a high voltage (HV)

pulse is applied to the common source node, while a programming current is flowing to a selected bitline. This bitline is selected through a column multiplexer (MULTIPLEXER). After the HV pulse is applied, the source follower voltage (Vsf) of the selected cell is read and compared to the sampled voltage. If the Vsf is equal or less than the sampled voltage a latch will be reset. The latch will cause the selected bitline to be tied to an inhibit voltage 'Vxx'. This will stop further programming. There are multiple copies of the S/H circuit with comparator latch and column MULTIPLEXER on-chip. This allows the multiple cells to be programmed in parallel.

2.4 HV generation and distribution

Fig 6 illustrates a simplified block diagram of the high voltage generation and distribution. The erase and iterative programming pulses (Fig. 3a.) are generated via the block CDAC, which is a digital to analog converter. As the counter (10bit HVINC) counts up CDAC produces pulses from 6 to 12 V, which increment in 16mv steps. The pulses are applied to the CS of memory cell in the array. Two separate op amps are used during the read and the program operations. The voltage applied to the CS line is force-sensed to eliminate the drop along the decoder switches. The voltages are then passes through a predecoder (XRED) and a decoder (XDEC) according to which memory cell in the array needs to be programmed.

2.5 Analog Path

The analog path (Fig. 7) has been designed to provide maximum flexibility and ease of integration when interfacing with any mobile communication system. There are three signal inputs namely, MIC+/-, AUXIN, ANAIN and three signal outputs, ANAOUT+/-, SP+/-, and AUXOUT. Internally there are several analog processing blocks interconnected by programmable multiplexers. Fully differential signal paths are utilised on-chip to maximise signal quality and the multiplexers utilise pumped gate bias to reduce distortion and non-linearity. The processing blocks are as follows:

- Microphone Automatic Gain Control (AGC). This is designed for a 3mV to 300mV input signal with an output level fixed to maximise the array resolution. The AGC is a two-stage circuit consisting of a variable gain stage utilising NMOS transistors with a variable gate control voltage to control the gain followed by a novel switched capacitor AC coupled, fixed gain stage.

- Summation Amplifiers. These two amplifiers allow the mixing of signal paths to achieve full-duplex recording or playback functions.
- Sample Rate of the device. It has four user selectable settings to produce sample rates of 4, 5.3, 6.4 and 8kHz. The oscillator is referenced to a 0TC(0 Temperature Coefficient) current source derived from an on-chip bandgap reference.
- Low Pass Filter. This a 5^{th} order Chebyshev filter used as an anti-aliasing filter in record mode and a smoothing filter in playback. The filter uses MOSFET resistors whose control voltage is derived from the oscillator current, forcing the cut-off frequency to track the oscillator frequency over the 4-8kHz range of sample frequencies.
- Volume Control. An 8-step volume control/attenuator is provided allowing signal adjustment in 4dB steps.
- Balanced ANAOUT amplifier. A high signal quality balanced output is provided to interface to the cellular baseband section
- Speaker Driver. A 23mW speaker driver is integrated to differentially drive an 8-Ohm load. The amplifier uses pumped voltages to allow rail-to-rail output swing.
- Variable Gain Input Amplifiers. The AUXIN and ANAIN inputs incorporate variable gain amplifiers to allow interfacing of signal levels to the array.
- Multilevel non-volatile analog memory storage array, which can be written upto one million cycles, and stores data without power consumption for 100 years.

A description of the various paths is given below (Fig.7). These paths are activated by issuing SPI commands to the system:

a) *Feed-through Mode:* In this mode the user communicates with the remote caller without the device recording or conditioning the signal. The user's signal is received at MIC+ and MIC-, goes through a 6dB gain element and is transmitted to ANAOUT+ and ANAOUT-. Also the remote user's signal can be received at ANAIN, passed through a variable gain amplifier, a multiplexer, and to a speaker driver which drives the speaker.

b) *Record Mode:* In this mode the user's signal is coupled in at MIC+, MIC- and goes through an AGC circuit which produces a signal level that fits the array window, and input multiplexer, summing amp, filer multiplexer, low pass anti-aliasing filter which smoothes this signal, another summing amp and is stored in the non-volatile array. The signal can also be recorded from AUXIN. The signal of the remote caller can

be coupled to ANAIN and can be recorded with the local user talking at the same time.

c) *Play OGM Mode:* This mode is used to play an outgoing message in a mobile application or in a pure answering machine application. The signal goes from the storage array to the anaout amplifier that transmits the signal upstream through the baseband circuit, via a path consisting of the following blocks: filter multiplexer, low pass filter and summing amp2.

d) *Full duplex record mode:* In this mode both sides of a conversation (user and caller) can be recorded. The analog signal of the user is transmitted upstream to the remote caller through the signal path that includes the 6dB amp, anaout mux and anaout amp, sum2 amp, the agc amp and the input mux. The remote caller's signal is received at ANAIN and is transmitted through the anain amp, output mux, and speaker driver amplifier to the user. The remote caller's analog signal is also fed to sum1 amp, which mixes the 2 signals. This mixed signal passes through the filter to the storage array.

e) *Full duplex play mode:* This mode is used to playback a stored message to the remote caller while the user is talking to the remote caller. The signal paths involve mixing the user's analog signal at the Mic inputs with the message in the storage array and transmitting the mixed signal upstream to the remote caller. The user's analog signal is coupled to the Mic inputs and routed to sum1 amp through the AGC amplifier and the input mux. The message in the storage array goes through the filter, through the filter mux and is applied to sum1 amp which mixes the two signals. The mixed signal is routed to ANAOUT+, ANAOUT- through the anaout mux and amplifier for transmission upstream to the remote caller. The second path involves mixing the remote caller's analog signal with the message recorded in the storage array and providing the mixed signal to the user. The remote caller's analog signal is received at ANAIN input, amplified by a variable gain amplifier, through the sum2 amp which mixes the remote caller's signal with the message stored in the storage array and provides this to the volume control circuit which adjusts the level of the signal and presents it to the speaker driver through the output mux.

2.6 Command Set

For interfacing to a microcontroller, this system uses the SPI interface with a smart instruction set. The instruction set is designed to easily accomplish frequent operations such as play or a record operation or message cue operation. The analog path is configured by the user via a 32 bit configuration register which is used to set multiplexer's gains, sample rate and allow power down of unused blocks thus reducing power consumption.

3. CONCLUSION

A 2.7V to 3.3V analog signal processing and storage system has been presented (Fig. 8) for interfacing with the cellular baseband system (Table2), combining a fully integrated programmable signal interface. The system has a configurable signal path to maximize flexibility and ease system integration with all wireless and cordless chipsets. In mobile communication applications, the system allows for two-way call recording, call screening, playback or recorded message during a call, voice memo, and an answering machine/call screening function.

4. ACKNOWLEDGEMENTS

The authors would like to thank James Brennan Jr., Don Tran, Theresa Chung and Chris Chan for their support during the project.

5. REFERENCES

[1] T. Blyth, et al., *ISSCC Digest of technical Papers*, pp. 192-193, Feb. 1991.

[2] H. Tran, et al., *ISSCC Digest of technical Papers*, pp. 270-271, Feb., 1996.

[3] J. Brennan, et al., *Proc of NVSMW*, pp. 41-42, August, 1998.

[4] B. Yeh, *U.S. Patent No. 5,029,130*, July, 1991.

[5] Y. Tsividis, et al., *IEEE JSSC*, pp. 15-30, Feb., 1986

[6] Al Kordesh, et al,VLSI Technology Systems, and Applications, June 1999

[8] C.Liu, et al, VLSI Technology Systems, and Applications, June 1999

Table1. MEMORY CELL OPERATIONS

		Mode	
Parameter	Erase	Program	Read
Bit line current Ip or Id		-1uA	-1uA
Common source voltage Vcs	0V	6-12V	2.2V
Select gate voltage Vsg	~15V	2.3V	4.2V
Bit line voltage Vsf	float	~0.8V	*measure*

Table 2. CHIP CHARACTERISTICS

PARAMETER NAME	VALUE
Temperature	- 40C to 90C
No. Of equivalent bits	~ 8
VCC	3.0 V +/- 10%
SAMPLE RATES	4,5.3,6,4,8KhZ
DURATION	4-8 minutes
Analog Path SINAD	62.5dB(@ 1kHz dBm0)
AGC Input Range	3-300mV
Speaker Driver Power	24mW @ 8 Ohms
Record Cycles	100,000(typical)
Message Retention)	100 Years (typical)
ISB	< 1 μA
Die Size	4.1 x 7.6 mm
ICC	< 30 mA
Technology	0.0um Flash CMOS
SINAD	42 dB @32 mVpp, 1 kHz
THD	0.5%

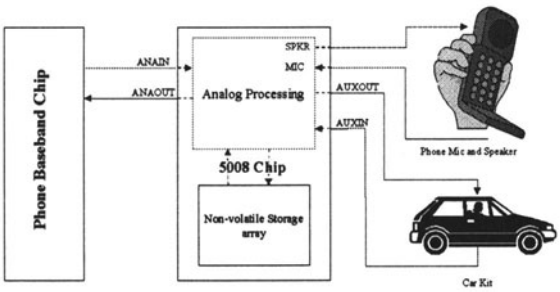

Figure 1. System Configuration for Applications

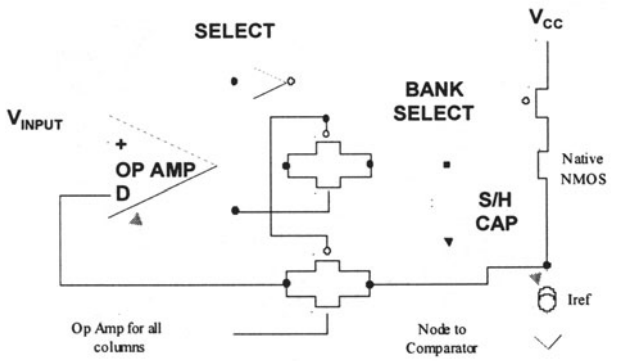

Figure 2. Cross Section of Cell

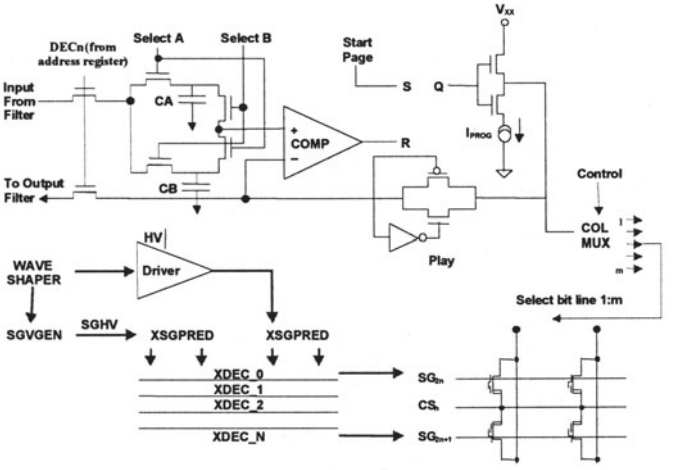

Figure 3. Cross Section of Cell a) a depiction of the erase and cumulative program sequence b) memory cell schematics c) Vsf-Vcs cumulative program characteristic curve, analog signal and analog window

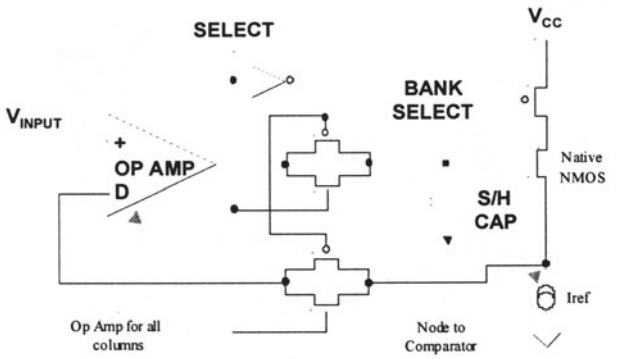

Figure 4 The S/H circuit – the Op Amp drives one S/H at a time to bring the comparator node to the same voltage as Vinput

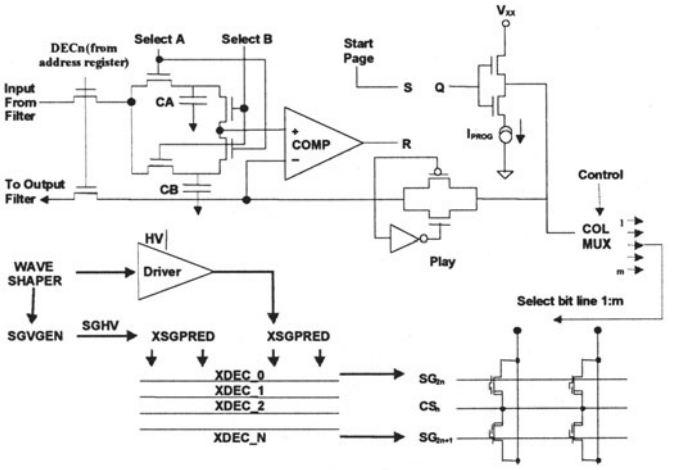

Figure 5 The writing circuits – the wave shaper, HV driver, row decoders, comparators column multiplexer and the memory array

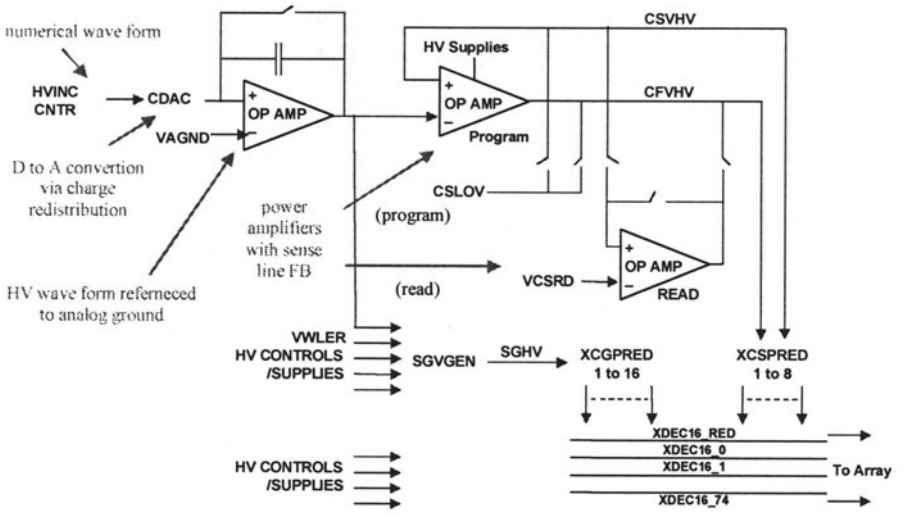

Figure 6. Data Storage Architecture

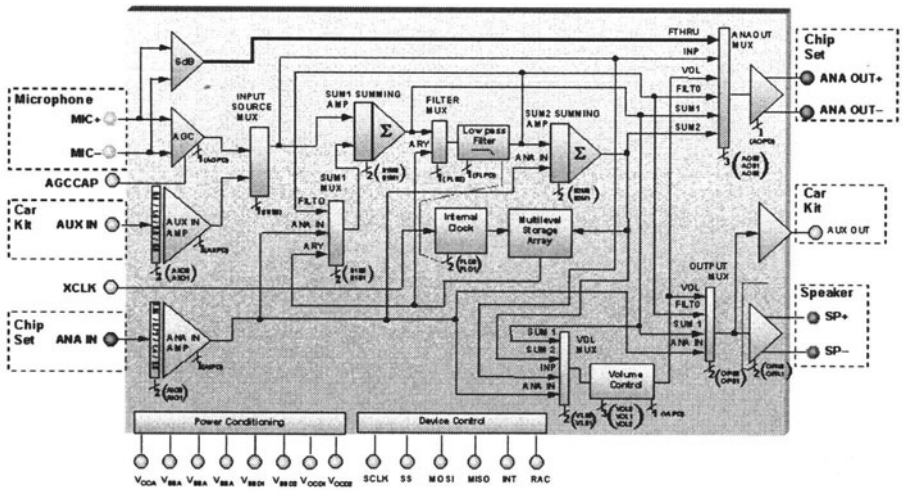

Figure 7. Analog Path Block Diagram

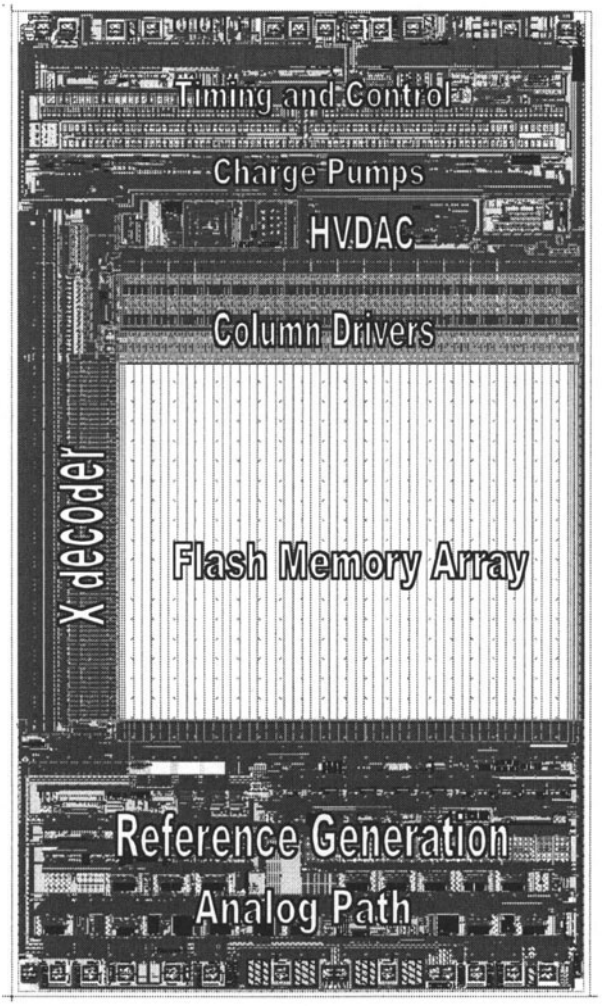

Figure 8. Die Photo