Optimizing Mixer Noise Performance: a 2.4 GHz Gilbert Downconversion Mixer for W-CDMA Application

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Abstract A downconversion mixer for wideband CDMA application is designed and fabricated in a 0.5 μm CMOS technology. The mixer operates at 2.4 GHz frequency with a 3 V power supply and consumes only 4.5 mW power. Targeting in designing high performance mixers of high yield within short design cycle, this paper addresses RF mixer design issues from an optimization and statistical point of view, and derived the noise equation based on a simple noise model of the Gilbert-cell mixer. The mixer achieved a conversion gain of 14.3 dB, a SSB noise figure of 10.4 dB, and an IIP3 of -8 dBm.

Keywords: RF Mixer, Noise Optimization, WCDMA

1. INTRODUCTION

In recent years the portable communication market has been a strong driving force for IC technology development. In portable systems, low-power and low-cost are the most common requirements. Under the surface of these requirements, the full analog and mixed-signal single-chip solution is of great interest to researchers among industry and academic institutions. This in turn stimulates the evolution of new system architectures with emphasis in using submicron CMOS technology.

Along with the new architectures and new technologies are the numerous wireless standards in different regions and for different services. The current world may not be able to foresee the merge of these different standards. In fact, the standards themselves are lastingly evolving and new standards are

The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: 10.1007/978-0-387-35498-9_57
L. M. Silveira et al. (eds.), *VLSI: Systems on a Chip*

still emerging, each with different system specifications and creating highly challenging problems for RF components design. In a portable communication system, RF components take only a very small fraction of the whole system, but the cost for RF parts is relatively much higher than that of baseband and digital parts. This is mainly due to the fact that systematic design methodologies for RF components of high performance are still limited or immature. One example to show the complexity of the problems is the design for low noise figure RF blocks. In general, a RF block can be designed to have an optimum noise figure with regard to a given source impedance. Yet optimum noise figure does not agree with optimum impedance matching, optimum power consumption, or maximal linearity. In a more complicated case, the noise performance of a mixer is even hard to be analyzed in a closed analytical form. Thus, most commonly, a RF system/block is designed in an ad-hoc fashion, with a high cost of human power and a low yield of products.

This paper presents the design of a Gilbert cell mixer which is used in a direct downconversion architecture for a wideband CDMA RF transceiver at the 2.4 GHz ISM band. The design will address the issues mentioned above, and seek to provide some half theoretical and half empirical methods to speed up the design process. Section 2 gives a description of the whole mixer. Section 3 discusses the performance optimization of the mixer with regard to transistor sizes. In Section 4 we give the design result for the mixer followed by a few comments to conclude the paper.

2. CIRCUIT DESCRIPTION

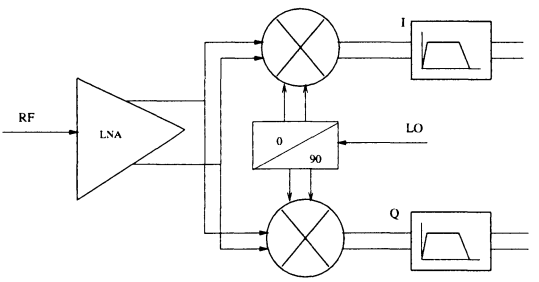

Figure 1 Direct downconversion RF front-end

The direct downconversion wideband CDMA receiver structure is shown in figure 1. The RF signal is located in the 2.4 - 2.48 GHz frequency band, being spread over a 32 MHz bandwidth. We adopted the double balanced Gilbert-cell mixer in our application mainly because the overall performance of Gilbert mixers is generally superior to that of other type of mixers at Gigahertz working frequency. Since low-voltage and low-power design is the mainstream for

portable products, this work will address the LV/LP design issues with regard to Gilbert cell mixer. The power supply in this design is 3 volts. It should be noted that new mixer architectures should be sought as power supply is scaled down below 2.0 V. For RF mixers, while most design efforts are centered on designing the mixer core to achieve good noise figure, linearity, conversion gain, etc., attention should also be paid to the biasing circuits to ensure the core circuit work well and achieve good performance [7]. For instance, variation of the tail current, and variation of LO biasing, can degrade the linearity and noise figure tremendously. Figure 2 is the complete circuit diagram of the mixer,

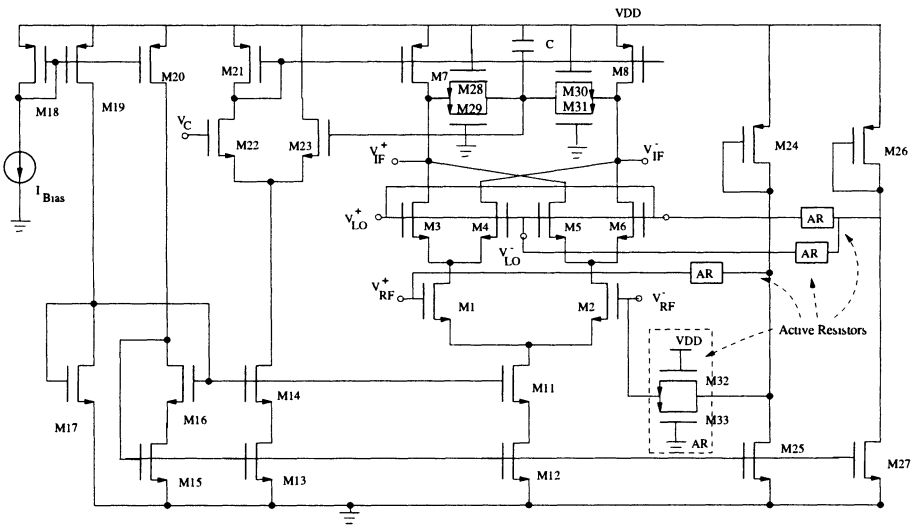

Figure 2 Schematic diagram of the mixer

similar structure can be found in [4] [5].

In this circuit, transistors M1-8 form the core of the Gilbert cell, with M1-2 the input transconductance stage, M3-6 the commuting switches, and M7-8 the PMOS active load. For certain applications, the load transistors M7-8 can be replaced by passive inductors, hence to reduce the power supply. However, inductive load is not suitable for our broadband and direct downconversion case since the inductive load essentially presents a variable gain over the frequencies and zero gain at DC.

The tail current of the Gilbert cell is supplied by a wide-swing current mirror composed of M11-12 and M15-17. The wide-swing current mirror keeps the Gilbert cell from distortion at the low end of the output voltage swing. For testing purpose, the biasing current of the whole circuit is controlled through an exterior current source of 0.1 mA(I_{Bias}). The scaling factor of the current mirror is 1:10, giving 1 mA for the nominal tail current of the Gilbert cell. Instead, the actual obtained current is 1.1 mA because device parameters such

as V_T vary with regard to channel width and length. In this current mirror, M11-12 work right at the edge of the triode region, so do M15-16. To account for the parametric mismatch during fabrication that might deviate any of M11-12 and M15-16 from working in active region, the drain current of M19 is designed to be slightly larger than that of M20 [2]. With the above design, the output tail current is constant when the drain voltage of M11 is driven to as low as 0.3 V.

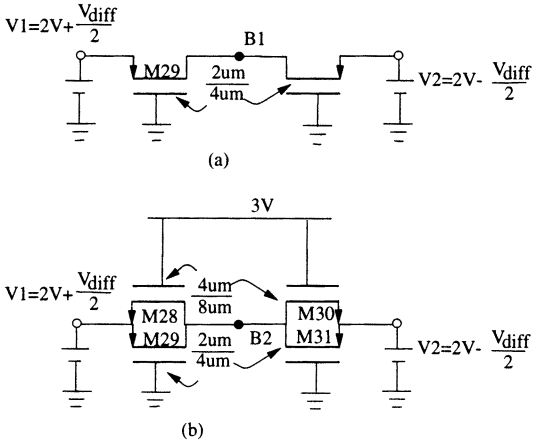

Figure 3 Common-mode voltage acquistion

Transistors M21-23 form the common-mode feedback loop. The common-mode voltage is acquired by transistors M28-31, which work in triode region and function as active resistors. Since the gate-source voltage applied to M28-29 and M30-31 are not equal, the circuit is not symmetrical, meaning the resistance given by M28-29 and M30-31 are not equal. Figure 4 shows the common-mode voltage characteristics when a differential-mode signal is

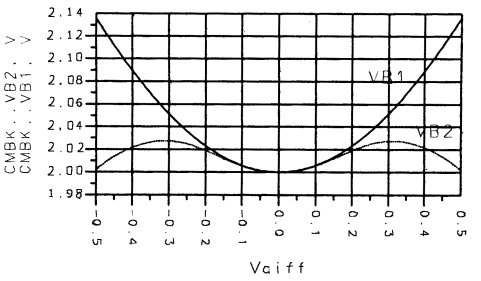

Figure 4 Common-mode voltage

applied as shown in figure 3(a)(b). Without any common-mode voltage variation, the differential-mode voltage will drive the CMFB loop, causing the common-mode output deviate from its nominal value. If the differential output has a wide swing, this deviation may cause problem for succeeding stages. Note that the NMOS transistors in this complementary structure add to the noise of the circuit. If the noise contribution from M28, M30 is significant, we should consider using only M29 and M31 [figure 3(a)]. However, the PMOS-only configuration causes even larger deviation [VB1 in figure 4(a)].

M24-27 provides DC biasing voltage to the LO and RF ports. The AR blocks, briefed for active resistors (M32-33), are used to isolate the negative and positive input signal ports, and to keep the biasing circuitry from loading the input signals.

3. PERFORMANCE OPTIMIZATION

To achieve a high quality of communication under existing technologies, the RF front ends are often required to work right at their performance limits. The design of a satisfactory RF system is a trade-off of many critical performance parameters. Generally, the design of RF components is a try-and-error procedure. It is worthwhile to investigate optimization techniques to speed up this procedure. With CMOS technologies, performance parameters of RF components are directly related to the width and length of building transistors. For a given circuit, ideally, we can represent all the performance parameters by these geometric parameters quantitatively, which gives a complete description of the problem space. As long as the problem space is completely describable, one can identify a set of optimal solutions to satisfy the targeted system specifications. It also becomes possible to investigate how each geometric parameter affects the system performance, thus to identify those most critical parameters. In reality, however, with tens of transistors in a circuit, the problem space has already been prohibitively large in terms of the variable geometric parameters, let alone that in RF frequency, one need to take high order parasitic effects into consideration. For these reasons, many works consider the optimization problem with regard to only parts of the performance parameters [6] [3], or less complicated circuits such as LNA [1]. The overall design optimization of mixers, somehow is still a myth to designers, and much effort is based on experience.

To design the Gilbert cell mixer for our direct downconversion application, we need to size transistors M1-8 carefully to approach a trade-off among the different performance parameters. The first consideration is the LO leakage and self-mixing problem. With down-scaled tail current, the aspect ratio of the M1-8 can be chosen to be small, as a result, the transistor sizes can be also small, which reduces parasitic capacitance and in turn reduces LO leakage. However,

the transconductance of M1-2 should be moderately high enough in order to achieve certain conversion gain. The effective gate-source voltage of M3-6 should be small enough to ensure that the transistors can be switched on and off quickly, at the same time, to avoid pushing the source voltage of M3-6 too low such that M1-2 is driven to triode region. These two requirements demand larger aspect ratio for M1-6. Meanwhile, the aspect ratio of M7-8 is chosen to satisfy the output DC working point. To obtain proper conversion gain, the length of M7-8 can be adjusted so that the output impedance is changed.

The noise figure is affected when we scale the sizes of M1-8. We want to see how each transistor contributes to the noise of the mixer. Generally, with MOS devices, large device geometry is desirable for better noise performance. Intuitively, for the mixer, increasing the conversion gain will reduce input-referred noise level. The problem is that in our case we favor moderate gain. In other words, with moderate gain, the noise performance may not meet system specification. A fine tuning of the width and length of M1-8 is then necessary.

For the wideband direct downconversion mixer, we realize that the main noise contributors are baseband flicker and thermal noise, and thermal noise downconverted from RF frequency. The actual noise mechanism of the mixer is hard to describe analytically. We attempt to understand the noise in such a way:

- Baseband noise from M3-8 directly contributes to the output without the need to consider frequency mixing.
- Baseband noise from M1-2 also directly contributes to the output. To understand this, one just needs to notice that M3-M5, and M4-M6 always form a path from M1 or M2 to the IF ports.
- LO signal and its harmonics mix with noise from M1-2 at different noise band near LO and its harmonics down to baseband [3].

To investigate the noise behavior with regard to the transistor geometry, we simplify the problem and look at only the signal path formed by M1, M3, and M7. The equivalent noise model is illustrated in figure 5. We first assume that all three transistors working in active region (This assumption is true when LO signal are in transition).

The input-referred flicker noise is given by

$$\begin{aligned} v_{in,f}^2 &= v_{g1,in}^2 + v_{g3,in}^2 + v_{g7,in}^2 \\ &= v_{g1}^2 + v_{g3}^2 \frac{(\frac{I}{\lambda_n L_1})^2}{g_{m1}^2} + v_{g7}^2 \frac{g_{m7}^2}{g_{m1}^2} \\ &= \frac{K}{W_1 L_1 f} + \frac{K}{W_3 L_3 f} \frac{(\frac{I}{\lambda_n L_1})^2}{2\mu_n C_{ox} \frac{W_1}{L_1} I} \end{aligned}$$

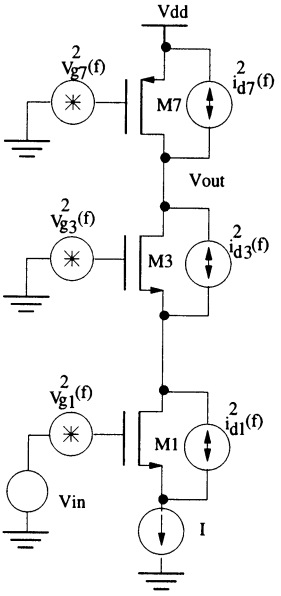

Figure 5 Noise model of the Gilbert cell

$$+\frac{K}{W_7L_7f}\frac{2\mu_pC_{ox}\frac{W_7}{L_7}I}{2\mu_nC_{ox}\frac{W_1}{L_1}I}$$
$$= \frac{K_1}{W_1L_1f}+\frac{K_2I}{W_1L_1W_3L_3f}+\frac{K_3L_1}{W_1L_7^2} \tag{1.1}$$

where K_1, K_2, K_3 are process dependent constants.

The input-referred thermal noise is given by

$$\begin{aligned} v_{in,t}^2 &\simeq \frac{i_{d1}^2}{g_{m1}^2}+\frac{i_{d3}^2r_{ds3}^2}{g_{m1}^2(r_{ds1}+r_{ds3}+r_{ds7})^2}+\frac{i_{d7}^2r_{ds7}^2}{g_{m1}^2r_{ds1}} \\ &\simeq \frac{4kT\frac{2}{3}g_{m1}}{g_{m1}^2}+\frac{4kT\frac{2}{3}g_{m3}}{g_{m1}^2}+\frac{4kT\frac{2}{3}g_{m7}(\frac{\lambda_pL_7}{I})^2}{g_{m1}^2(\frac{\lambda_nL_1}{I})^2} \\ &= K_4\frac{\sqrt{L_1}}{\sqrt{W_1I}}+K_5\frac{L_1\sqrt{W_3}}{W_1\sqrt{L_3I}}+K_6\frac{\sqrt{W_7L_7}L_7}{W_1L_1\sqrt{I}} \end{aligned} \tag{1.2}$$

where K_4, K_5, K_6 are also process dependent constants.

Now consider the situation when M3 works in triode region (M1 and M7 still in active region). The noise terms contributed by M1 and M7 are still valid in equation (1.1) and (1.2). However, in first order approximation, the flicker noise of M3 does not have much influence on $V_{in,f}^2$ and can be neglected from

equation (1.1). The input referred thermal noise from M3, is now given by the following equation,

$$\begin{aligned} v_{in,t3}^2 &= \frac{I_{ds}^2 r_{ds3}^2}{g_{m1}^2 r_{ds1}^2} \\ &= \frac{\frac{4kT}{\mu C_{ox}\frac{W_3}{L_3}(V_{gs3}-V_t)}}{2\mu C_{ox}\frac{W_1}{L_1} I(\frac{\lambda_n L_1}{I})^2} \\ &= K5\frac{L_3 I}{W_3 W_1 L_1 (V_{gs3}-V_t)} \end{aligned} \tag{1.3}$$

The obtained noise equations can be utilized in design optimization. One can find that increasing W_1 will reduce both thermal noise and flicker noise. Increasing L_1, however, does not necessarily achieve lower noise, implying that an optimal value exists for L_1. The equations also quantitatively illustrate the geometric influence of other transistors, as well as the biasing current and LO voltage. The result, in combination with those in [6] [1], is aimed to provide some insight into mixer design and performance optimization. It efficiently helped to reduce the design time in achieving appropriate conversion gain, noise figure and linearity in our design. It should be reminded that the simplified model does not take 2nd or higher order parasitic effect and short channel effect into consideration. More rigorous efforts should be taken to ensure analytical reliability and accuracy.

4. CONCLUSION

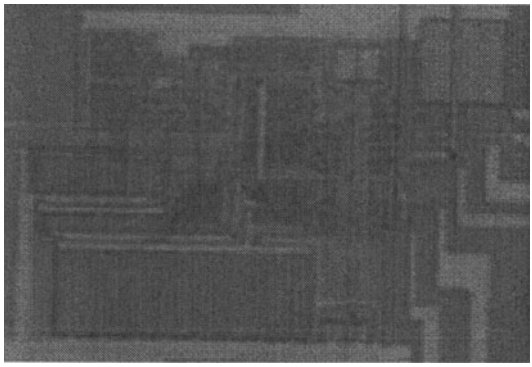

Figure 6 Die Photo

This paper presents the design of a direct downconversion mixer for wide-band CDMA application. Figure 6 is the die photo of the mixer fabricated in

a 0.5 μ m CMOS technology. Table 1 summarizes the simulated performance parameters. The test is still under processing.

Specifications	Results
Power Supply	3 V
Current Consumption	1.5 mA
LO Input Power	0 dBm
RF Input Power	-60 dBm
Conversion Gain	14.26 dB
SSB Noise figure	10.66 dB
IIP3	-8.02 dBm
SFDR	65.03 dB

Table 1 Performance Summary

In this work, we discussed the design and optimization issue of mixers. We derived the noise equations according to a simplified noise model as a guideline for mixer design. For high volume and high performance RF components design, systematic design methods, along with effective statistic analysis techniques, should be pursued in the near future.

5. ACKNOWLEDGMENTS

Support for this research was provided by Texas Instrument Graduate Fellowship at The Ohio State University.

6. REFERENCES

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