ATM and Optics

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Abstract

The contribute reviews aspects of the interaction between the asynchronous transfer mode (ATM) technology and the optical technologies. ATM for broadband networks presents some issues which result appealing for an optical approach. Some of them consist in the possibility of implementing ultra-high velocity ATM protocol functionality, in the development of free-space packet switching networks, in the solution of the access contentions to a shared transmission resource by deploying the wavelength resource. On the other hand, the development of the optical layer gives the transmission bandwidth availability which forecasts a larger penetration of ATM even at the network edge.

In the communication some examples of the ATM/optics interaction will be given. In particular it will be shown how to implement optically two basic functions of the ATM protocol, that is the Header Error Control and the Traffic Policing. Also, the interaction between a remote ATM network and the access network will be object of the presentation.

Keywords

All-optical switching, photonic packet-switching, ATM switching, header processing, node interface.

1 INTRODUCTION

In the last decades one of the most relevant phenomena in telecommunications has been the 'photonization' of ever increasing portions of the fixed communication infrastructure of the worldwide networks (Sato, 1996). This process began with the rapid deployment of optical fibers in almost all network levels as an alternative to copper wires. Technical and economical advantages of the new transmission medium were so strong that not only copper was almost

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completely abandoned for the new installations, but also a new branch of research in optics applied to telecommunications was fostered.

With the introduction of the optical amplifiers the optical fiber transmission systems evolved so rapidly that they are now a fully established technology, though still many issues remain to investigate. New records of transmission performance, such as nonregenerated distance, bit-rate and number of wavelengths, are continuously achieved by advanced systems, while commercial systems are always evolving toward high reliability and low cost targets.

In the present situation the 'photonization' process is on its way to enter a second phase, which is the penetration of optics into switching. If information propagates through the links of a network in an optical format, it seems quite convenient that it should not be converted to an electronic format in each node, to be converted in optics a second time on the next link: this main reason justifies the idea of optical switching. If this is true in principle, the realization of switching by means of optical technology has proved to be a nontrivial task, and in some cases quite difficult.

In the following of this contribution, after a short look at the perspectives of optical networks in general, we review the current status of research on ATM photonic switching. This particular aspect of optical networks can be considered nowadays an advanced topic compared to other solutions. In fact, even if many research activities have been dedicated to it, various critical issues remain unsolved. We will therefore review the main projects regarding all-optical ATM switching, mainly focusing on the node architectures, propose some new investigation objectives and outline what are in our opinion the 'hottest topics' for the future.

2 A PERSPECTIVE ON OPTICAL NETWORKS

The main feature which characterizes all-optical networks is transparency (Iannone, 1996): this property implies that optical signals can traverse more nodes and links without undergoing opto-electronic conversions (other properties such as scalability and modularity are also very important).

There can be different definitions or different levels of transparency. Transparency in the widest sense (*full optical transparency*) is attained when all network functions are independent of the signal modulation format and speed. In this case both digital and analog optical signal (as a subcarrier multiplex of CATV channels) can be switched by the nodes of the network. A more limited level (*bit-rate optical transparency*) concerns networks where only digital and intensity modulated optical signals can be routed, but processing performed by the nodes is independent of their bit-rate. When optical networks based on packet switching are considered, then another meaning of transparency can be given: *payload optical transparency*. In order to perform packet switching nodes must process only the header of the packets. Optical packet switching nodes can be therefore designed in such a way that they are transparent to the bit-rate of the information carried in the payload, as this part of the packet it does not have to be read or modified.

Research in optical switching led to the proposal of different solutions which exploit various levels of optical transparency.

In the access area all-optical switching has been employed in the passive optical network (PON) networks. Time-division multiplexed (TDM) PONs (Figure 1a) are the most developed solution (Faulkner, 1997). The TDM multiple access protocol required to manage the upstream traffic is implemented by electronic equipment located in the network terminations. Therefore the network cannot be considered truly optically transparent. An alternative solution for FTTH is WDM PON (Frigo, 1996) (Figure 1b): each user is identified by a wavelength channel, and the remote node consists of a wavelength-routing passive device, such as the wavelength grating router (WGR). These networks can be made *fully optically transparent*, and solutions have been proposed in which both digital (for voice and data traffic) and analog channels are switched (Frigo, 1997). A critical issue in this networking

approach is the scalability, as the number of users is limited by the number of wavelengths that can be routed.

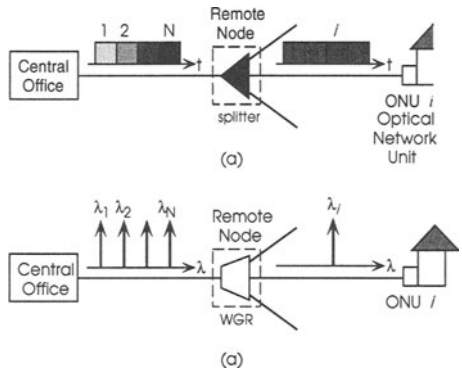

Figure I Passive Optical Network architecture: (a) TDM PON and (b) WDM PON.

The remote nodes of PONs perform only fixed routing, which is not a real switching function. All-optical switching performing a full switching functionality has been instead more developed in the transport area. Wavelength division multiplexing (WDM) technology is nowadays the main research topic in optical networks. A new network layer responsible of the switching of optical paths by means of optical cross-connect (OXC) nodes has been defined. In the WDM layer transparency is mainly intended as *bit-rate optical transparency*. The WDM core network is interfaced with higher network layers by means of electronic switches or SDH multiplexers (Sato, 1996). A scheme of the WDM transport layer is represented in Figure 2a. The optical paths in the transport network are circuit-switched. Besides routing also wavelength assignment must be performed by the network management system. Algorithms to evaluate optimal routing and wavelength assignment (RAW) have been analyzed in various studies (Banjeree, 1997), (Subramanian, 1997), also considering the case when OXCs are able to perform wavelength conversion of the optical paths. A general functional architecture of a WDM OXC is shown in Figure 2b. The node must provide switching connectivity in both space and wavelength domain. The reconfiguration time of optical paths is relatively long (in the order of milliseconds). In (Iannone, 1996) and (Sato, 1996) two main classes of OXC architectures have been identified, the first based on space switching and the second on wavelength switching. The first class is further subdivided into models based on a switching matrix and models relying onto the delivery and coupling concept. The blocking properties of these are also discussed there. The combined use of the space and wavelength multiplexing domains allows the exploitation of design criteria different from those typical of classical electronic switching matrices. The new wavelength multiplexing domain is also essential in photonic packet switching architectures, as we are going to explain later.

3 PHOTONIC ATM SWITCHING

Research in photonic packet-switching evolved in parallel with WDM. Many solutions have been proposed up to now, but none of them seems yet to have reached the same stage of development as WDM, for the reasons we will discuss in the following of the paper. Among all the solutions, we will consider in particular those relating to ATM switching techniques.
The investigation of ATM all-optical switching seems motivated by the opportunity of applying more general concepts of photonic packet-switching to a network model which is

well established and standardized. Moreover ATM seems to be a future-proof technology, as it allows transport features required by the future telecommunication services. Actually some disappointments about the initial expectations on ATM arise due to the fast diffusion of Internet and to a slower penetration of those services which rely upon severe quality of service targets and mostly justified the ATM features. Nevertheless, new architectural solutions such as IP-over-ATM (Decina, 1997) suggest not to abandon this subject.

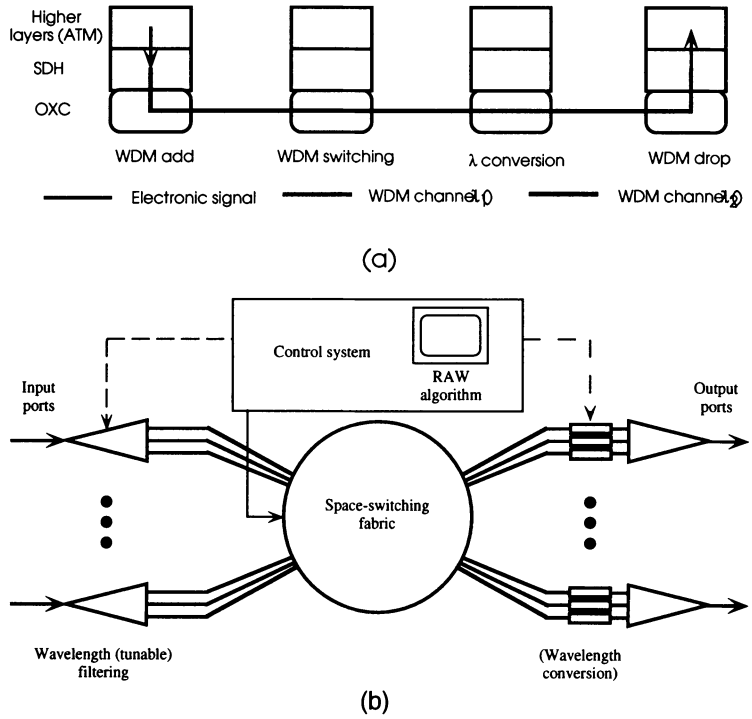

Figure 2 WDM transport networks: (a) a scheme of WDM optical path switching and (b) a functional scheme of an Optical Cross Connect.

An ATM network (de Prycker, 1995) is based on a paradigm quite different from the one we described for the WDM layer:

- Complete packet (or cell) switching operation has to be performed in this case in every node of the network (Figure 3a). This operation requires that the node identifies the cell, reads some routing information from the header and modifies it. Therefore *full optical transparency* can not be achieved in any way. The only transparency a photonic implementation would allow is what we called *payload optical transparency.*
- ATM is a connection-oriented packet switching technique. Virtual circuits and virtual paths are established, managed and terminated by the access nodes which perform more functions (belonging to the adaptation layer) than the internal nodes. The rate at which virtual circuits and virtual paths are set-up, routed and closed is dependent on the service characteristics and can potentially be of the order of the cell rate. This means that an ATM node not only must perform cell switching fast enough to adapt to the bit-rate, but also must be rapidly reconfigurable.
- The number of channels managed by an OXC is limited by the number of wavelengths per fiber. In ATM the number of virtual channel is by far much higher, since each channel is simply identified by a logical address carried by the VPI/VCI field of the header (2^{32} available values!).

In order to better understand photonic ATM switching a brief review of these basic functions according to ATM protocol could be helpful (Pattavina, 1998). The relevant layers of the protocol stack in this discussion are those whose functions are usually implemented by hardware, i.e. the physical layer and the ATM layer.

The ATM layer comprises the following functions:

- generic flow control
- cell header regeneration and extraction
- cell VPI/VCI translation
- cell multiplexing and demultiplexing
- policing and congestion control.

The physical layer is further subdivided in transmission convergence and physical medium dependent sublayers. The former comprises:

- cell rate decoupling
- header error control (HEC) sequence generation/verification
- cell delineation
- cell scrambling/descrambling
- transmission frame adaptation
- transmission frame generation/recovery.

The latter comprises:

- bit timing
- physical medium management.

A general architectural scheme of a node is represented in Figure 3b. The main difference between this and the other scheme reported for the WDM OXC in Figure 2b is the presence in this case of buffers and of processing interfaces.

The buffering capacity is essential for statistical cell multiplexing, and can be implemented in different ways and variously located inside the node architecture. The buffers and the space switching fabric together perform the core function of the switch, often referred to as multiplex switching.

All the other functions of ATM and physical layers are performed by the processing interfaces (one per each input/output port of the node). The most important of these functions is cell VPI/VCI translation: a peculiar characteristic of ATM is in fact the requirement of changing the logical address of a virtual channel or path at every node (label switching). HEC verification in particular is also very important since it is the basis also for cell delineation. Cell rate decoupling must be done when cells inside the multiplex switch assume a different format due to the addition, for example, of local routing information or guard-band intervals among consecutive cells. Transmission frame adaptation, generation and recovery are not necessary any more if we suppose that in the physical layer bit streams are organized directly as raw cells and are not carried by any transmission frame (like SDH). This simplification is quite important for an all-optical implementation, as we shall underline later on.

Summarizing, in an ATM switching node, beside multiplex switching, two other fundamental operations are performed by the processor interfaces: header reading and header writing. The payload of the cell is in no way involved in any of these ATM processing function, thus proving that *payload optical transparency* can be achieved by an optical implementation.

Most of research developed since today on photonic ATM switching has been dedicated to the multiplex switching. We will now briefly review the main solutions that have been proposed, trying to examine their architectural properties.

Two main approaches to photonic ATM switching fabric design have been followed. In the first approach only the switching fabric is considered, while buffering is left as a separate problem. In the second approach, instead, space switching and buffering are treated as an integrated problem.

Unbuffered architectures

In (Prucnal, 1993) simple 2x2 photonic switching elements (SEs) have been designed, which are capable of implementing cell self-routing on the basis of a local address and output port conflict resolution and have no buffering capacity. By employing these elements as building blocks, larger switching fabrics can be obtained. These fabrics can be defined partially connected networks, since a SE of a stage is not connected to all the SEs of the next stage. Thanks to the self-routing capability, different networks can be created with various blocking characteristic. The simplest is the Banyan network, which is blocking as is well known, since it provides a single path per inlet/outlet pair and each interstage link is shared by several inlet/outlet paths. To improve blocking performance deflection routing has been proposed: if two cells have to be routed onto the same interstage link of the fabric, one is actually routed towards the required destination, while the other is sent onto a sub-optimal path. Blocking can be removed if the connection requests to the switching fabric are previously sorted. The most known example of an architecture providing this feature is Batcher-Banyan, in which a Banyan network is put in cascade after a sorting network (Batcher). Photonic SEs designed for the Banyan network can be quite easily transformed into sorting elements, which are the building blocks of the Batcher sorter.

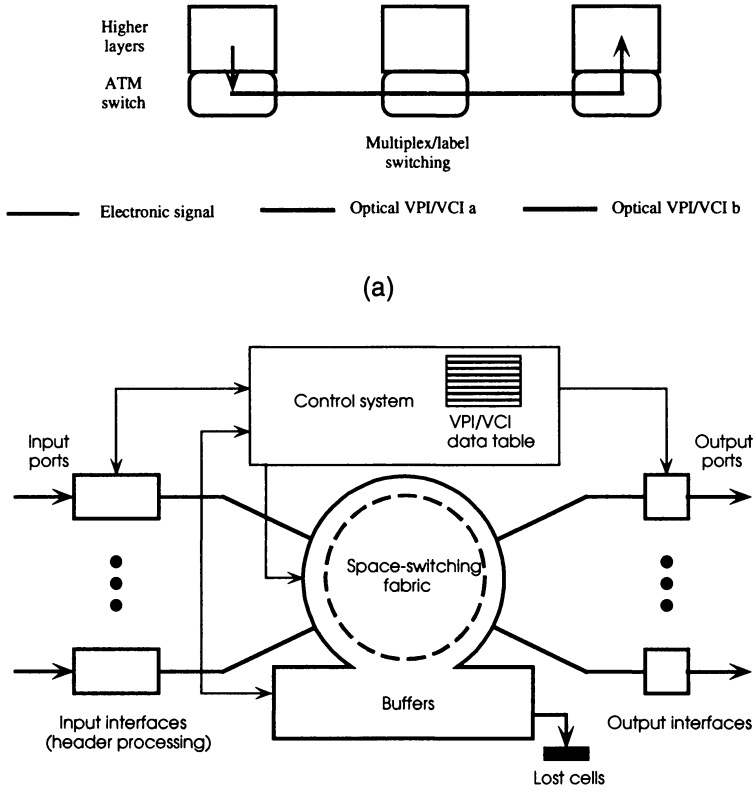

Figure 3 ATM networks: (a) a scheme of ATM switching and (b) a functional scheme of an ATM switching node.

Another type of unbuffered architecture can be obtained by connecting in various topologies output-multiplexing building blocks. These blocks have N inputs but $N{\cdot}K$ outputs: though they

have no inner buffer, they resolve output conflicts, since up to K cells can be routed to the same output in the same time slot. In ATMOS an output-multiplexing architecture has been proposed, based on a building block called Multidimensional Switch (Eilenberger, 1995). In this block the output multiplex is easily realized by wavelength multiplexing more cells on an output fiber.

Buffered architectures

In the second approach to ATM switching design more complex architectures have been proposed. The concept common to all of them is that the complete switch should be obtained connecting stages of smallest modules, according to a fully connected topology (each module of a stage is connected to all the modules of the next stage), such as a Clos topology (Casoni, 1994). This design concept allows to distribute most of the control and management functions, thus simplifying the control system of the node. Each module is equipped with buffering capability, so that also buffering is distributed. In ATMOS a reference model of the overall switching system has been identified whose parameters are: 256 input/output ports with a bit-rate of 2.5 Gb/s per port (Masetti, 1996). The target performance proposed for the switch is: 0.5 Tb/s throughput with a load of 0.8 Erl per port. These dimensions and performance can be accomplished employing single modules which have around 16 input/output ports. The buffering capacity is then assigned to each module according to the cell-loss probability which must be achieved. These figures, evaluated in ATMOS project, can give the order of magnitude of the sizes also of other photonic ATM switching systems.

The switching module architectures can be classified according to the position of the buffers as: input, output and shared buffer modules.

Input buffer modules have been seldom developed (Varvarigos, 1997), since this structure suffers from the head-of-the-line blocking phenomenon.

Most of the proposals concern the architectural solution with output buffering. In these systems storage elements are usually realized by means of fiber delay lines. However different peculiar properties of optical signals are exploited in order to let all the output buffers be accessed by cells coming from all the input ports at the same time (speed-up).

An architecture proposed by NTT (Tsukada, 1996) is called Ultrafast Photonic ATM Switch (ULPHA). This switching module employs the time resource to realize the speed-up. This is achieved by optically compressing the cells in time in such a way that, if N is the number of inputs and T (s) is the cell duration, inside the node each cell has a duration T/N (s). Actually the system is designed to operate with electronic signals at the input ports, but in principle it could also operate on an all-optical flow, provided that the input electro-optical modulators are substituted with all-optical modulators.

Architectures proposed in ATMOS and KEOPS projects rely instead on wavelength to obtain the speed-up necessary to access the output buffers. The first module proposed is the Fiber Delay Line Switch (Gabriagues, 1995). In this architecture cells at the inputs are wavelength converted and each one is "colored" according to the destination output port, which on the other hand will have an optical filter to identify the correct cells. Then all the cells are wavelength division multiplexed in a common buffer structure of fiber delay lines. The position of each cell in the buffer is determined by an optical structure based on the broadcast and select concept. A second module has been proposed (Broadcast and Select Switch) (Masetti, 1996) not very different from the Fiber Delay Line, but which allows cell multicasting .

Another output buffer architecture proposed by NTT is Frontiernet (Sasayama, 1997). In this case variable wavelength converters at the input and tunable filters at outputs are employed. Moreover a WGR instead of a star coupler is used to multiplex signals. The functionality of this architecture is similar to the Fiber Delay Line, but broadcast and select structure is not required.

The third class of switching modules comprises shared buffer architectures. An example is the Fiber Loop Memory Switch (Cinato, 1995), proposed in ATMOS. The buffering structure is composed of a single recirculating fiber loop, which is shared by wavelength division

multiplexing. A number of logical FIFO queues, one per output port, are created and managed by the (electronic) control system over the same physical loop memory. An input cell is converted to a wavelength assigned according to the position it must occupy in the logical FIFO queue corresponding to its destination. Tunable filters in the outputs select the correct cell in each time slot.

The implementation of the processing interface functionality by means of all-optical subsystems has been studied only in the last few years, mainly as a consequences of the advances in all-optical processing device technology. One of the first example of this new activity is the header regeneration and writing subsystem proposed by (Chiaroni, 1996). The subsystem is based on the semiconductor optical amplifier (SOA), which seems to be a promising device. Another example (which actually has been proposed a bit earlier) is the cell synchronization and alignment subsystem based on fiber variable delay lines (Prucnal, 1993). Even if the cell flow is optical, the control signals of the subsystem are still obtained by electronically reading the header of the cells.

4 OPTICAL IMPLEMENTATION OF ATM NODE SUBSYSTEMS

In this section we present some application areas regarding ATM node on which we focus our attention. We briefly propose different solutions where optics allows to achieve high performance operations on the signal. Our aim is just to demonstrate the feasibility and the advantages of employing optical technology in telecommunication switching nodes. Optics can offer several benefits over traditional electronic approaches based on serial processing of information, because of the opportunity to explore new and efficient architectures.

Novel architectures able to exploit in a very efficient way the capabilities of optics in order to perform ATM interface processing are described. The proposed examples constitute the premise of photonic subsystems building for communication ATM nodes.

VPI/VCI field recognition

In ATM nodes the channels are identified by a logical address carried by the VPI/VCI field of the cell header. In any hypothesis of self-routing packet switching it is fundamental to recognize optical information. Here we propose an optical technique able to perform the recognition of digital words in a passive way without any opto-electro and electro-optic conversion. The recognizer is based on an optical Vander Lugt correlator realized by means of volume holography (Gu, 1995). To use it the input data flow must be converted in a spatial word constituted by a 2-D pattern of optical bits.

In a Vander Lugt architecture realized by means of volume holography the optical signal which carries the information to be recognized is set at the front focal plane of a lens so that the signal Fourier transform is obtained at the rear focal plane, where a thick recording medium is centered. A coherent reference plane wave lights the holographic medium. The interference pattern induced by the signal and the reference beams is stored as a perturbation of the index of refraction. When a new signal is coming in input, it can be compared with the stored pattern by detecting the Fourier transform of the diffracted beam at the rear focal plane of a new lens. In this point we read the correlation between the input signal and the stored one. Large storage capacity together with real-time response makes volume holography a very promising candidate for next generation optical processing. Multiple information can be recorded within the same holographic medium using angle multiplexing and can be used like a database for signal recognition. The input signal is in fact compared simultaneously with all the stored data producing an optical output just in the spatial position corresponding to the recognized information (Figure 4).

In Figure 5 we present the experimental results in the case of recognition of the digital byte 191. The storage of 256 holograms in visible light corresponding to the whole set of bytes in a single $LiNbO_3$ crystal is performed. A complete recognition of a single digital word in real time is obtained using phase-coded input signals.

Header Error Control

Parallelism represents one of the most advantageous features for future optical switching nodes. It matches naturally the use of spatial bandwidth: each signal of a parallel data stream is transported through a spatial channel by a light beam. Many spatial channels can propagate together in the same volume with no crosstalk. Parallelism is fully deployed by means of free-space architectures.

We present an example of free-space architecture employed in ATM processing: a parallel header error control (HEC) sequence decoder performing error detection on the incoming ATM cell headers. We do not consider the correction-mode HEC operation in this design.

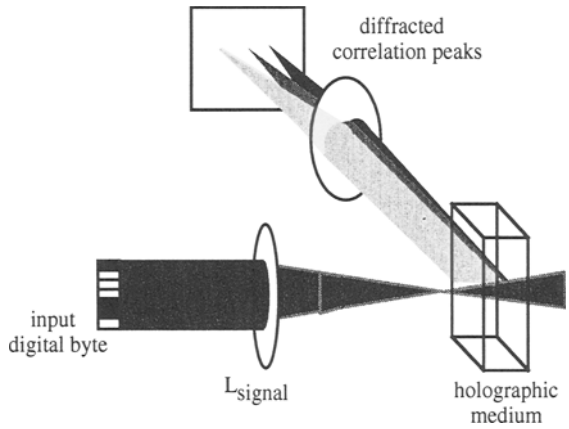

Figure 4 Volume holographic optical correlator useful for digital word recognition.

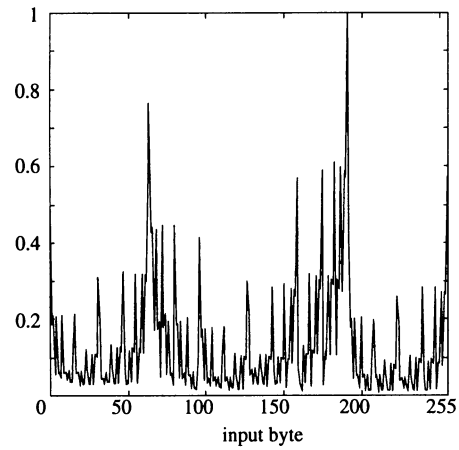

Figure 5 Correlation intensity related to the byte to recognize 191 as a function of the phase-coded input bytes. The correlation signals are detected in output of the volume holographic correlator and are normalized by the peak intensity of the autocorrelation signal.

The HEC is a function necessary to protect the information contained in the cell header from transmission errors. According to ITU-T standards (ITU-T I.423) the code in HEC processing is a "shortened" cyclic code. Using the classic serial algorithm (Benedetto, 1987), in which binary polynomials represent the header digital words, the decoding operation is carried out

by computing a polynomial named syndrome, constituted by the remainder of the division between the received header to process and the generator polynomial. The serial decoding operation is generally implemented by electronic hardware, where a shift register performs the binary polynomial division operating at the bit-rate speed.

By resorting to matrix algebra we can find an alternative parallel decoding algorithm more suitable to exploit all the advantages of a free-space structure. In this formalism the error detection is achieved simply through the analysis of the syndrome vector **s**: if any bit of the vector is "1", then an error is present. The vector **s** is obtained multiplying the received header **y** (including 40 bits) by the transposed matrix **H'**:

$$\mathbf{s} = \mathbf{y}\,\mathbf{H'}$$

H (8x40 in size), the parity check matrix, is calculated directly from the generator polynomial of the code. Hence we can perform the HEC decoding completely in a parallel way, just by means of a single operation, with no flip-flops or memory required. Using modulo-2 arithmetic the operation $\mathbf{s} = \mathbf{y}\,\mathbf{H'}$ is the result of a sequence of scalar sums and products. The syndrome **s** can be evaluated from a **C** matrix (8x40) obtained through the AND operation:

$$\mathbf{C}(i, j) = \mathbf{Y}(i, j) \text{ AND } \mathbf{H'}(i, j) \qquad \forall \begin{cases} 1 \le i \le 8 \\ 1 \le j \le 40 \end{cases}$$

where the matrix **Y** (8x40 in size) is built by placing 8 identical columns side by side, each column equal to **y'**, the transposed of the row vector **y** corresponding to the received word. The vector **s** becomes:

$$\mathbf{s}(i) = \bigoplus_{j=1}^{40} \mathbf{C}(i, j) \qquad \forall\ 1 \le i \le 8$$

We propose a free-space implementation of the parallel algorithm described above (Figure 6). The received header signal is converted in a spatial form and then divided in 8 replica in order to obtain the 2-D **Y** matrix image. A simple array of beam-splitters can perform this operation. Then the AND operation between **Y** and **H'** is implemented simply by means of a spatial filter. This mask interrupts the optical propagation in relation to the "0" positions in **H'** and is transparent in coincidence of "1s". Because all the elements of **H** are "a priori" known, this operation is performed in a completely passive way. To perform multiple XOR operation along the 8 columns of **C** logic devices must be employed. 2-input XOR gates can be used in different configurations. The analysis of the syndrome vector can be obtain performing an OR operation on its 8 elements.

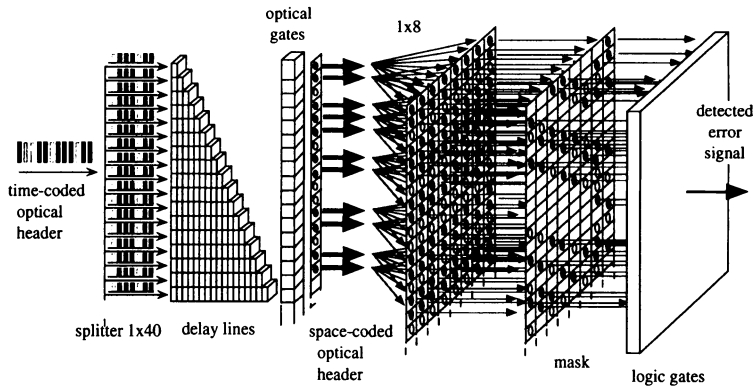

Figure 6 Scheme of the proposed implementation of the HEC optical subsystem.

The described structure is an example of a free-space architecture capable to perform a header processing function in an optical way. The utilized parallel decoding algorithm allows to eliminate the need of shift register and buffers. Parallelism allows the switching speed of

each single logic gate operating in the subsystem to a certain data bit-rate is lower than the required one in the serial configuration. In fact in a system operating on a parallel data flow an equivalent bit-rate can be defined as the bit-rate of a single data channel of the flow multiplied by the degree of parallelism.

Policing function

In an ATM network the policing function controls the traffic of the transmitted data cells in order to protect the network against excessive congestion resulting in a degradation of the quality of the offered service. Policing allows the behavior of the traffic source to be restricted in accordance with the specifications negotiated in the contract between the users and the network provider.

Here we consider the policing function related to the control of the peak cell rate (PCR), i.e. the maximum rate at which the source can generate new cells. The virtual scheduling algorithm (VSA) is one of the algorithms standardized by ITU-T (ITU-T I.371). The traditional implementation of a policer based on VSA is realized by means of logic and mathematical elementary blocks performed by electronics. We explore new functional structures more suitable to exploit the capabilities of the optical devices.

In Figure 7 we propose a new scheme useful for the VSA optical implementation. The cells coming from the input link enter the policer. Here a cell input recognizer generates a recognition signal which acts on an optical controller. It must set the state ("open" or "closed") of an optical gate at the input of the system. According to the recognition signal the optical controller, by means of a suitable control signal, tailors a temporal window in which the connection input remains open. The temporal width of this window is established according to the maximum allowable cell rate negotiated with the network. If a new cell comes while the input gate is still closed, it is discarded.

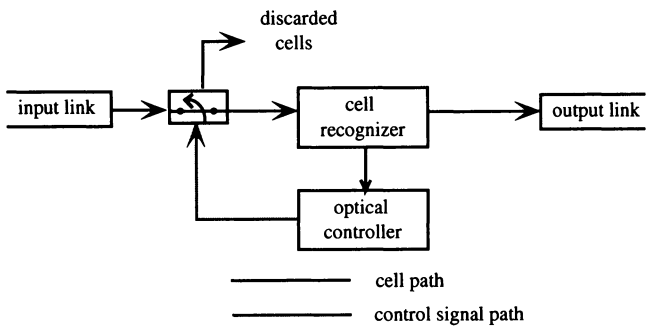

Figure 7 Logic scheme of the policer based on VSA.

The functional operators identified in the scheme described above are implemented using devices like couplers, delay lines and optical flip-flops. The cell-input recognizer can be realized in a simple way by means of an optical correlator capable to recognize a space-coded digital word. We have simulated the behavior of the system: Figure 8 and Figure 9 show the simulation results respectively in the case of a variable bit-rate input traffic and of a traffic with a bit-rate three times bigger than the allowed one. In our simulation the optical gate and the flip-flop in the controller are modeled like semiconductor optical amplifier (SOA) devices in interferometric structures (Chiaroni, 1995) in order to perform all-optical operations in which every control is optical.

5 CRITICAL ISSUES

The high complexity of a photonic ATM switching node that we tried to illustrate can be an obstacle for its future development, especially considering the competition versus WDM optical technology and also versus ATM electronic switching. Critical issues that arise involve technology, system and network aspects.

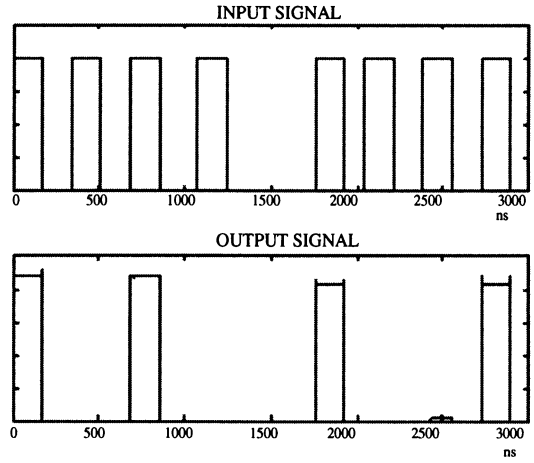

Figure 8 Simulation results of VSA policer operation. Upper trace: the input traffic at variable bit-rate. Lower trace: the restricted output traffic (maximum peak bit-rate STM-4).

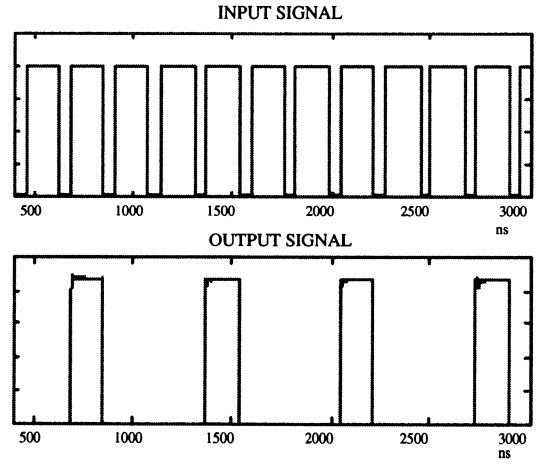

Figure 9 Simulation results of VSA policer operation. Upper trace: the input traffic at a bit-rate three times bigger than the allowed one. Lower trace: the restricted output traffic (maximum peak bit-rate STM-4).

If the advantages in terms of functionality of ATM versus WDM are clear, a debate issue is the advantage of an optical ATM solution versus an electronic implementation. It is true that the realization of a very large bandwidth node is a difficult task also in electronics (Butner, 1996), especially in those subsystems, like line interfaces, where bit-to-bit parallelization (the

technique used to overcome the speed limitations of CMOS technology) can not be employed. However the costs of electronic components remain nowadays still much lower than that of optical devices. A final assessment of this point is still impossible, given the continuous evolution of both the technologies. Another penalty of optical technology is reliability. It has been demonstrated (Wosinska, 1997) that at present all the proposed ATM optical architectures have a reliability quite lower than that required by standards.

From a system point of view the advantages of all-optical ATM must be still investigated. Unfortunately the architectures described in the previous section has been tested only as prototypes with limited functionality: for instance the cascading of modules in multistage architectures has only been simulated, while all the experiments have been performed on a single module. Beside that, quite often only the multiplex switching fabric has been tested by experimentation. The all-optical subsystems proposed belonging to the processing interface, instead, have been tested separately or have not been tested yet. Often in experiments some all-optical subsystems are replaced by an electronic version, due to technical or economical reasons. If some functions of a photonic ATM node are implemented by electronics, the advantages of optics, such as *payload optical transparency*, may not be achievable. The fact that photonic nodes cannot still be tested as integrated complete systems prevents them from being experimented in a real network environment.

The positioning of photonic ATM in the network layer structure is not yet as clear as in the case of WDM. Various attempts, for example, have been made to define a frame structure which suites to optical packet switching better than the ATM cell, but which in the mean time is not too far from ATM standards. None of the proposals made gained since now an outstanding role.

Another problem still to solve is to better understand where in the network infrastructure all the advantages of photonic ATM could be better exploited.

In the transport area the interoperability with lower network transport layers should be taken into account. If ATM cells should be carried in SDH frames, for instance, the *payload optical transparency* offered by photonic ATM nodes would appear useless, since up to now SDH processing can only be done by electronic devices.

In the access area the conditions are quite different. We have studied the problem of introducing an all-optical ATM switch as the remote node in a fiber-to-the-home (FTTH) access network. Due to the simple tree topology of the FTTH an ATM switch located in the remote node behaves as a cell dispatcher for the downstream flow and as a statistical multiplexer for the upstream flow. While in the case of the cell dispatcher technology and system aspects are more interesting, the cell multiplexer behavior should be analyzed from a network performance point of view. In order do this we chose as a reference the TDM PON model defined in (Faulkner, 1997), which is also compliant to the standard draft (ITU-T 50-E). In this model an ATM upstream traffic is managed by means of a multiple access protocol called Global FIFO, implemented by electronic equipment located both in the central office and in the user network terminations (Optical Network Units, or ONUs). This protocol is based on dynamic time slot allocation on the basis of requests that each user periodically sends to the central office. The amount of bandwidth of the total upstream flow depends on the occupancy status of the local buffer in each ONU (user buffer). Cell collisions cannot occur, since time slots are properly allocated in a centralized way. In the case of the photonic ATM remote node there is no centralized remote assignment and cell collisions do happen. Therefore the node must be able to resolve cell collisions and must also be equipped with a certain buffering capacity in order to reduce the cell loss probability.

The study, conducted with various traffic source models (here only the constant bit-rate - CBR - case is shown, but results with other sources are quite consistent), has shown that the most relevant advantage of the ATM solution versus Global FIFO is in terms of delay (Figure 10). In fact in Global FIFO the TDMA protocol sets a minimum waiting time for each cell to be transmitted necessary for the permit-message exchange; the same constraint is not set by ATM. Also the delay variation is reduced in the ATM case (Figure 11). Such a neat advantage

has not been found in terms of cell loss probability (Figure 12). The buffering capacity required inside the node is a trade-off between cell-loss probability and the node architectural complexity. Increasing the optical buffer in the node to reach low loss probability might lead to a cost increase which could be too high for such a cost sensitive area as the access network. Additional methods have also been investigated to allow a cooperation between the buffer in the ATM node and buffers located in the ONUs, which quite improves the situation.

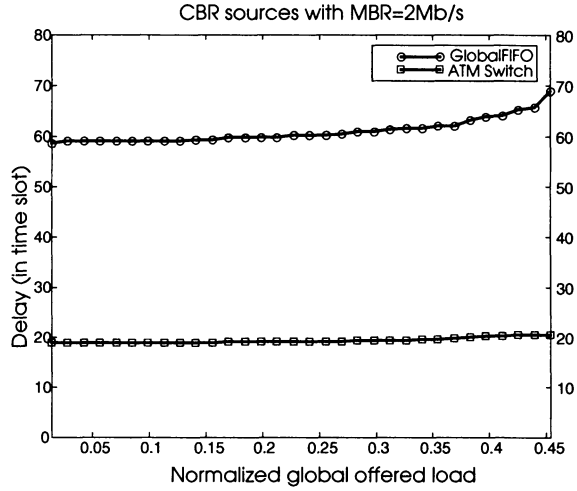

Figure 10 Comparison of cell mean delay between Global FIFO and ATM (CBR traffic).

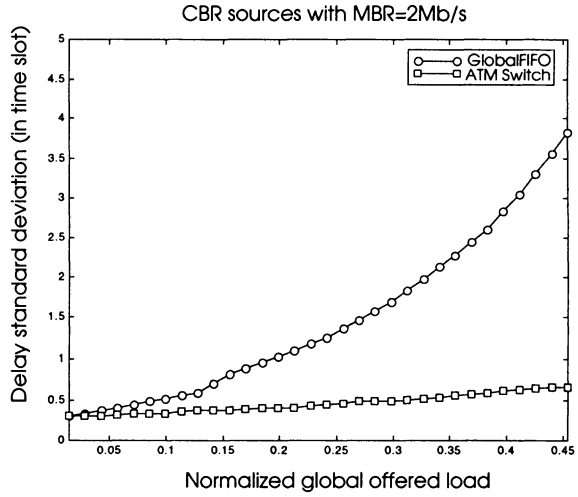

Figure 11 Comparison of cell delay standard deviation between Global FIFO and ATM (CBR traffic).

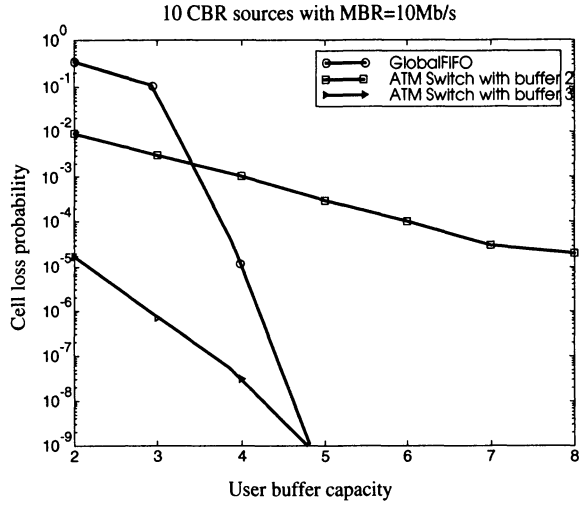

Figure 12 Comparison cell-loss probability between Global FIFO and ATM.

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