5

On-line testing of analog circuits by adaptive filters

M. Negreiros, L. Carro

Universidade Federal do Rio Grande do Sul
Departamento de Engenharia Elétrica
Av. Oswaldo Aranha 103
Porto Alegre - RS - BRASIL
CEP 90035-190
Fax: +55 51 226 11 71
Phone: +55 51 316 35 16
e-mail: carro@iee.ufrgs.br, negreiro@iee.ufrgs.br

Abstract

This papers describes a new technique for on-line testing of analog circuits based on plant recognition by adaptive algorithms. To the authors knowledge, this is the first time such technique is used to on-line testing of analog circuits, allowing complete fault coverage. The paper presents the testing methodology and experimental results showing easy detection of soft, large-deviation and hard faults, with a low cost digital processor. Components variations as low as 10% have been detected, as the comparison parameter (output error power) varied from 300% to 20%.

Keywords

On-line testing, analog circuits, DSP techniques, dedicated test architectures

VLSI: Integrated Systems on Silicon R. Reis & L. Claesen (Eds.)

1 INTRODUCTION AND MOTIVATION

Faults in analog circuits can cause different symptoms at the circuit outputs, from short and opening of components to slow deviation of the operation point caused by a degradation in passive or active component characteristics. On-line analog testing should detect any variation on circuit performance and warn a circuit supervisor. Different techniques regarding on-line testing of analog circuits have been reported ((Chatterjee, 1993), (Vazquez, 1993), (Lubaszewski, 1995)). Most approaches use some sort of analog circuit either to duplicate the analog function or to monitor its output.

In our approach, we observe the output of the analog circuit and compare it with an expected output. The comparison, however, is developed at the digital domain, with an adaptive filter. The function of the adaptive filter is to duplicate the analog behavior of the circuit at the digital domain, and detect any deviations from the operating point in case some fault is present. Any analog function that can be represented in the s plane by a pole-zero polynomial fraction N(s)/D(s) can be tested using this technique. Since we use digital filters, any other analog function expressed in the z-domain as a polynomial N(z)/D(z) can also be tested.

This paper is organized as follows: section 2 presents the overall idea of our approach, with mathematical explanation of its principles. Section 3 analyses a set of examples, were we show the success of the approach by detecting faults with some auxiliary digital hardware. In section 4 we discuss some limitations of the new technique, followed in section 5 by our conclusions and future work.

2 THE ADAPTIVE ALGORITHM APPLIED TO TESTING

2.1 The Adaptive Tester

In (Ben-Hamida, 1996) and (Mielke, 1996) DSP (Digital Signal Processing) techniques have been used to detect misbehaviors of AD converters. Basically, the Fast Fourier Transform was used to identify the presence of harmonics showing signal degradation. In our approach we first recognize the circuit under test as a plant, with all its pole-zero characteristics, like an analog signature. Then, we apply specific algorithms to detect any deviations from this first obtained analog signature.

The theory regarding linear plant recognition is quite settled (Ogata, 1970). Recently, with the advent of fast DSP microprocessors and boosted by digital communication problems, adaptive filtering took place as a good mathematical framework to solve not only line equalization problems, but plant recognition as well. The idea of an analog plant recognition by the use of an adaptive algorithms

is shown in Figure 1. A plant is submitted to an excitation, the same being done with an adaptive filter. Their output is compared, and the amount of error helps the adaptive filter change its coefficients in order to track plant performance.

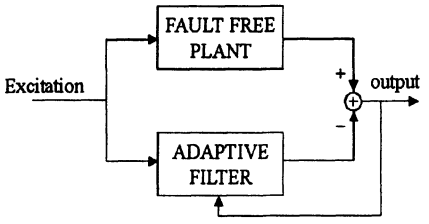


Figure 1 Basic plant recognition structure

After some time, all filter coefficients have stabilized, and the plant has a twin plant implemented in the filter. Now, one has only to change the output of the error signal in order to transform this adapted plant to a tester, as shown in Figure 2. Once we substitute the plant by a circuit to be tested, the previously adapted filter will output an error signal showing how much the new plant is equal to the previous (fault free) one. It is interesting to notice that this explains the robustness of the methodology. The basic idea is an analogy to the detection of variations in a bridge circuit. Any fault in the analog circuit, being it soft, hard or catastrophic, will change the plant under test. In other words, any change in the plant signature (its pole-zero characteristics) will increase the power of the error signal. The tester will detect this change and compare it to a previously defined threshold, according to the tolerated variation of the circuit.

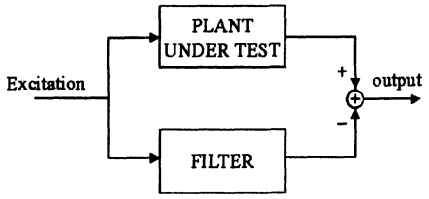


Figure 2 Plant being tested with filter

It is worth mentioning that not only basic components (resistors and capacitors) faults can be checked, but faults in the operational amplifiers used as well. Any deviation from the opamp ideal function will be recorded as another pole-zero signature at the s or z domain. Any fault present at the opamp will change this analog signature, being detected.

2.2 The adaptive algorithm and filter topology

A finite impulse response (FIR) digital filter (Proakis, 1988) can be represented by a polynomial on its input signals delayed by a fixed amount of sampling times, like

$$y(n) = a_0\, x(n) + a_1\, x(n\text{-}1) + a_2\, x(n\text{-}2) + \ldots + a_{m\text{-}1}\, x(n\text{-}m\text{+}1). \qquad (1)$$

In equation 1, $y(n)$ is the output at discrete time n, while m is the number of filter taps. In an adaptive digital filter all coefficients (a_0 ... $a_{m\text{-}1}$) are determined at runtime. The questions to be answered are how to discover the correct set of coefficients, so that the output of the filter performs the desired functions and, also, the depth m of the filter. In case of an adaptive filter, the output should exactly mimic the output of the plant. There are available different algorithms ((Haykin, 1991), (Widrow, 1985), (Mulgrew, 1988)), and their basic trade-off regards the amount of computations that must be performed against the speed of coefficient convergence.

The filter adapts to any plant, provided it has enough taps (pair coefficient-sample) to represent all poles and zeros of the original plant. Actually, the adaptive filter matches the impulse response of the plant. To decide which kind of signal to be used in order to excite the couple filter-plant, one must note that this signal:

1. must last long enough for the filter to converge (the error signal must go below a certain threshold), and
2. must be rich regarding its frequency components, in order to provide excitation of the plant at all frequencies of interest.

In our case, we choose one of the simplest adaptive algorithms, the Least Mean Square or LMS algorithm ((Haykin, 1991), (Widrow, 1985), (Mulgrew, 1988)). The algorithm is described in Figure 3.

```
begin
a_i(0)=0, i = 0...m-1
loop
        y(n)=SUM(a_i(n)*x(n-i)) , i = 0...m-1      /* filter */
        error(n) = d(n) - y(n)                     /* error */
        a_i(n+1) = a_i(n) + μ*error(n)*x(n-i)      /* coefficients */
end
```

Figure 3 LMS Algorithm

Once one knows the plant to be mirrored, the sampling frequency should be determined by an evaluation of the plant fastest response to be tracked by the test. In other words, the frequency response of the plant must be under the Nyquist

limit, fs/2. The maximum sampling frequency is a function of the data acquisition system. Since the goal is to test analog circuits, the number of poles and zeros is known a priori, so the frequency response of the system is already known.

The designer can now define the number of taps to be used by a set of relations shown in equations 2 and 3. To define the number of taps, one should know the sampling frequency (*fs*) and have an estimate for the duration of the plant impulse response (*Tir*).

The μ parameter can be chosen inside its upper and lower bounds, presented in equation 4 ((Haykin, 1991), (Widrow, 1985)), which are related to the power of the input signal applied to the system. The μ parameter can be a trade-off between speed of convergence (large μ) or precision in the error signal (smaller μ).

$$Ntaps = Tir/Ts, \tag{2}$$

$$Ts=1/fs, \tag{3}$$

$$0 < \mu < 2/(\mathrm{SUM}(x(n-i)\, x(n-i))),\ i=0,1,...,m-1. \tag{4}$$

In equation 4, $x(n)$ is the input signal sampled at time n, and m is the number of filter coefficients.

2.3 Adaptive filtering used to on-line analog testing

In order to excite the plant conveniently to detect the largest number of faults, the input signal should be such that all poles and zeros of the plant are properly excited. Any variation in this set of poles and zeros caused by any kind of fault will change the basic plant, and then be detected. The best signal would be one having all frequencies represented in its spectrum.

Our first approach was to use the impulse response of the system, for in an impulse signal all frequencies are present. The impulse response of a circuit applied to circuit diagnosis was partially used in (Su, 1995). The approach of using the impulse response of the circuit, however, is quite dangerous. An impulse can move some linear circuits out of their linear region of operation. Also, defining the correct finite amplitude of a theoretically infinite impulse signal while maintaining linearity could be quite tricky. Since the goal is to develop on-line testing, a better and more easily generated input signal was needed.

White noise has, by definition, an equally distributed power in its frequency spectrum. White noise can be easily generated using a random number generator and a DA converter. This way, white noise was the second natural choice. However, when used to on-line testing of analog circuits, the white noise generator might not be available, because of economical reasons (a DA converter might not be available). In this case, in order to adapt the filter, one might use the same input

that is used to the analog circuit during normal operation to run the adaptive algorithm.

In case of circuits for the audio bandwidth, for example, voice and music signals are extremely rich in their frequency spectrum, so that the filter can be adapted with enough frequency information. On the other hand, in case of instrumentation signals (for example, strain gauges), there is generally interest on a single frequency component. In this case, the on-line filter can adapt to the specific frequency, and any deviations will also be detected, as it will be shown.

An AD converter and a small C25 Digital Signal Processor can tackle the concurrent test to be carried, constituting a low cost on-line tester. In order to program the tester, the designer can take two tracks. The first one is to define a good plant at an abstract level based on his/her design, compute filter coefficients by any mathematical tool (Matlab, Mathcad, etc) and then use this as the reference plant. Another strategy is to develop of a fault free prototype, and then use the system to adapt the filter and save the discovered coefficients to be used during normal operation and concurrent test procedure.

Although all examples in this paper were developed with the C25, some simpler hardware like a dedicated bit-serial filter could also be used, lowering HW costs in the case of full custom integrated circuits solutions.

3 CASE STUDIES

In order to validate the proposed on-line test methodology, two circuits were used. The first one is a simple integrator, used to help the explanation of our methodology, and was just simulated. The Biquad is a little more complex, and was built and tested for different variations in some of its components.

3.1 Integrator

The integrator used is shown in Figure 4. The transfer function of this circuit can be found from elementary circuit analysis to be:

$$H(s) = \frac{-1}{R_1 C} \cdot \frac{1}{S + \frac{1}{R_2 C}} \cdot \tag{5}$$

For the simulation of this plant in the digital domain we take its z-transform ((Ogata, 1970), (Widrow, 1985), (Proakis, 1988)), in series with a zero-order hold:

$$H(z) = \frac{-R_2}{R_1} \cdot \frac{1 - e^{-kT}}{Z + e^{-kT}}, \qquad (6)$$

$$k = \frac{1}{R_2 C}$$

where T is the sampling period. From this equation we have obtained the recursive equations for the simulation of the plant, using the values for the circuit components presented in Figure 4.

The system was simulated using Matlab. We have used the rand function to generate the input to the circuit, and a FIR adaptive filter with 60 taps was adapted for 3000 samples. After conversion, the filter coefficients were stored and a new plant was defined, changing the value of C from 1.0μF to 0.95μF (a -5% variation). The resulting output error of the two cases is shown in Figure 5 (a)(for the identified system) and in Figure 5 (b)(-5% variation). The estimated output error power ratio has been found to be 13.3475 for this case. Both figures are at the same scale.

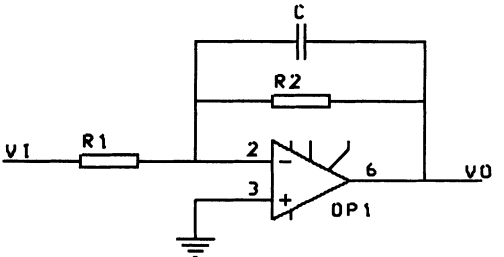
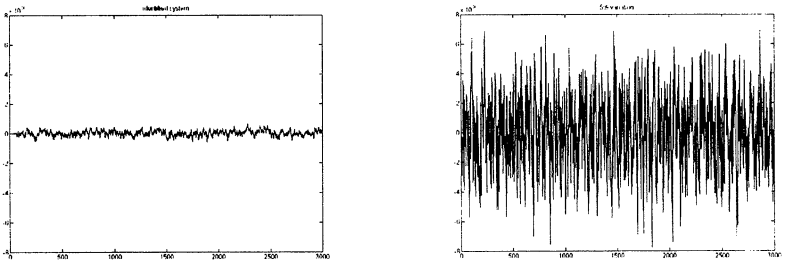


Figure 4 Simple Integrator, where R1=1e3, R2=1e3, C=1e-6 and T=0.1e-3.



(a) (b)

Figure 5 (a)Error output of a good plant (identified system) and (b)error output of the integrator with a variation of 5% in C

3.2 Biquad filter

The Biquad filter was used to validate the methodology and a prototype circuit was built from discrete components. The circuit is shown in Figure 6, with the nominal values that were used.

We have used a PC with a DSP board with an analogue interface (16 bits resolution, with reconstruction filters) as the input generator, and a C25 board with an AD converter (14 bit) as the on-line testing system. The sampling frequency used was 8khz per channel and we used a 48 taps LMS adaptive filter. The C25 board sampled the input and the output of the plant. The analogue interface used a multiplexed AD without anti-aliasing filters. Data was not sampled simultaneously. The experiment block diagram is shown in Figure 7. The output signal was generated from the C25 board using a 8-bit DA converter. Note that all calculations use fixed point arithmetic (16 bits).

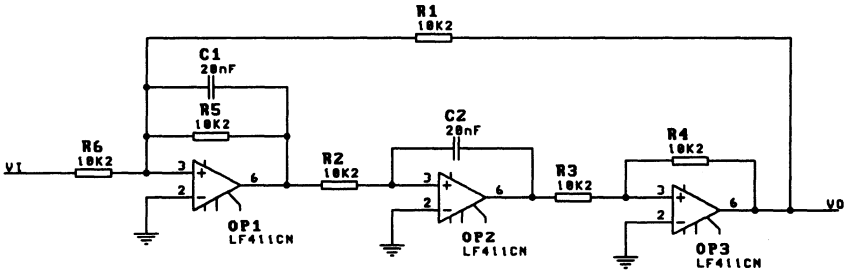


Figure 6 Biquad schematic, with R1,...,R6=10K2, C1,C2=20nF

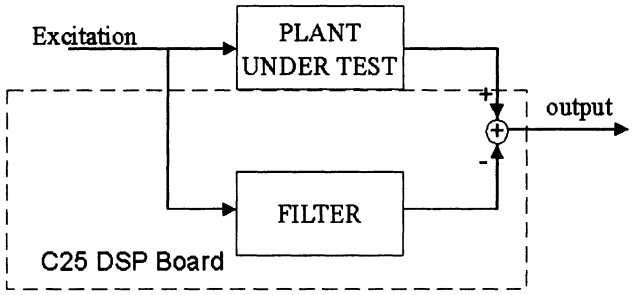


Figure 7 Experiment block diagram

We have used 40 taps for the adaptive filter, and adapted the system during 3000 samples. All data processing after acquisition was made in the C25 board. The processor has a 16 bit multiplier, and all filter coefficients were computed with fixed point multiplications.

The output error, the input signal and the filter output were measured for the identified system, and are shown in Figure 8 (a)(top-down). In this case, the

system tester was adapted with an 4KHz bandwidth limited white noise, emulating some voice or music information. The error for a +10% variation in C2 is shown in Figure 8 (b)(both figures at same scale).

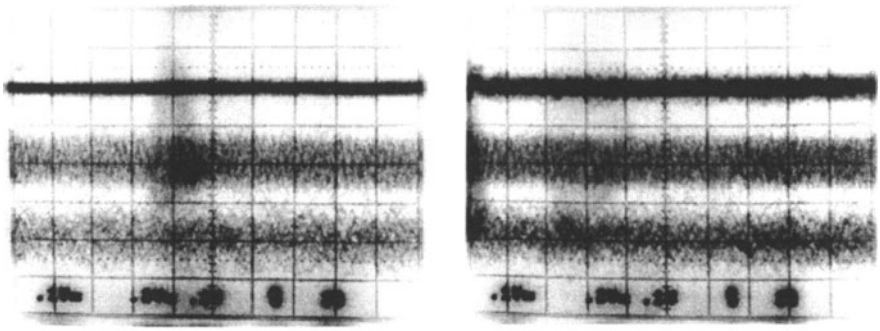


Figure 8 Error signal (100mV/div), input signal (200mV/div) and filter output signal (100mV/div) (a)for the identified system and (b)for a 10% variation in C2

In Figure 9 (a) we have adapted the tester to a single frequency (0.16kHz), emulating the case when the system should be used in some instrumentation process. The same variation was applied to the plant (10%) and the results are shown in Figure 9 (b).

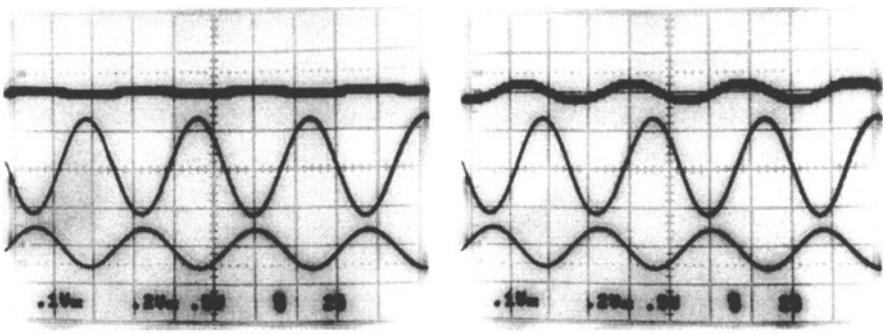
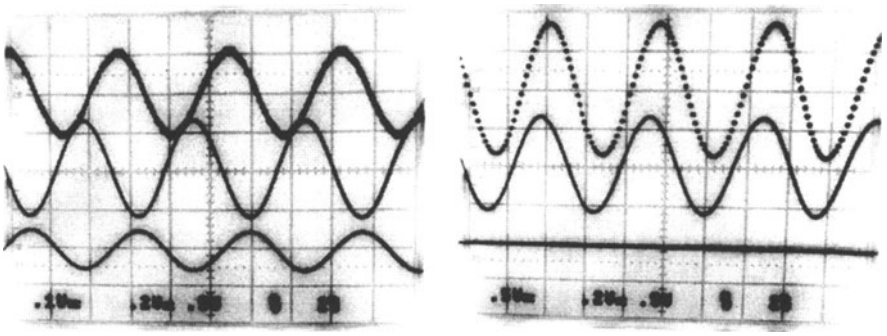


Figure 9 Output error (100mV/div), input signal (200mV/div) and output signal (500mV/div) (a)for an excitation with a single frequency and (b)for an excitation with a single frequency with 10% variation in C2

In case of the Biquad all tests of the proposed methodology detected small component deviations. One should also mention that the test is inherently simple and fast: there is not the need to choose the correct set of input frequencies, neither to verify more than one variable like the gain or phase. Figure 10 (a) shows the

response of the system to a large deviation (50%) of C2, while Figure 10 (b) presents the response of the tester to a catastrophic fault (C2 is shorted - note filter output). Again, the error signal is clearly different from the normal case, and is available either at the digital or analog domain. Notice the scale difference of the error signal between both pictures (0.1 to 0.5 V/div).



(a) (b)

Figure 10 Output error, input signal and filter output (a)for a 50% deviation in C2 and (b)for a short in C2.

4 LIMITATIONS OF THE APPROACH

Although conceptually simple and easy to use, the methodology is based on some assumptions that must be fulfilled. The first is that an AD converter with enough resolution and speed is available. The C25 processor can be considered to be a low cost one, but since we are using it as a simple filter, a custom digital signal filter is not out of reach, even with low cost FPGAs.

Adapting time is quite fast, and even when the filter might have a large number of coefficients to be settled, this is done only once every time a circuit is powered. Alternatively, filter coefficients could be stored in a E2PROM to be always available.

Since adaptive algorithms are mathematically based on the Z transform, they can have a DC component. In our case, however, we still can not detect gain faults separately, since they could be mixed with some low frequency pole or zero variations. Moreover, the concurrent testing procedure we use can not presently detect the faulty component.

Finally, it should be mentioned that for circuits working at very small frequencies one would have to have a huge number of taps. To avoid this, since this means extra processing time to the C25 processor, the designer must use a smaller sampling frequency. Also, at high frequencies, one might have troubles

with the acquisition system. In this case, the acquisition AD converter must have enough bandwidth to respond to all the high frequency poles.

5 CONCLUSIONS AND FUTURE WORK

This paper has shown a new on-line test strategy able to precisely detect soft, hard or catastrophic faults in an analog circuit. Since we use a digital processor, migration from the SW implementation to a dedicated HW is at hand. Bit-serial digital processors are being investigated, in order to reduce filter costs and allowing fast integration of the tester, even with FPGAs.

The method is quite robust, and is able to detect minor component variations or large plant changes caused by shorts or opens, without problems. Since the methodology does not assume any set of particular frequencies, it can be integrated to any analog circuit described as a transfer function in the s-plane or the z-plane. Since we use a digital signal processor to implement the filter, its adaptation to any analog circuit is straight forward, without any redesign need.

In our future work we intend to expand the methodology to include AD and DA converters, as well as DC signal components. Moreover, since a saving in processing power means a lower tester cost, we are investigating the implementation of digital filter only with shifters, and not multipliers. Also, faster algorithms than LMS are to be investigated, as well as low computations ones. Finally, since the original plant is known by the test engineer, the possibility of detecting the specific faulty component by a modification in the convergence algorithm will be investigated.

6 REFERENCES

Ayari, B.; Hamida, B.H.; Kaminska, B. (1995) Automatic Test Vector Generation for Mixed-Signal Circuits. In: European Design & Test Conference, *proceedings...* Paris, France. p.458-463.

Ben-Hamida, N.; Ayari, B.; Kaminska, B. (1996) Testing of Embedded A/D converters in Mixed-Signal Circuit. In: IEEE International Conference on Computer Design, *proceedings...* Austin, Texas. p.135-136.

Chatterjee, A. (1993) Concurrent Error Detection and Fault-Toilerance in Linear Analog Circuits using Continuos Checksums. *IEEE Transactions on VLSI Systems*, v.1, n.2, June. p.138-150.

Haykin, S. (1991) Adaptive filter theory. 2.ed. Englewood Cliffs, N.J.: Prentice-Hall. 854p.

Lubaszewski, M.; Mir, S.; Rueda, A.; Huertas, J.L. (1995) Concurrent Error Detection in Analog and Mixed-Signal Integrated Circuits. In: 38th Midwest Symposium on Circuits and Systems, *proceedings* ... Rio de Janeiro, Brazil. p.1151-1156.

Mielke, J. (1996) Frequency Domain testing of ADCs. *IEEE Design & Test of Computers*, Spring, p.64-69.

Mulgrew, B.; Cowan, C. F. (1988) Adaptive Filters and Equalisers. Kluwer Academic Press.

Ogata, K. (1970) Modern Control Engineering. Prentice Hall. 929p.

Proakis, J.G.; Manolakis, D. G. (1988) Introduction to Digital Signal Processing. Macmillan Publishing Company, New York. 944 p.

Slamani, M.; Kaminska, B. (1995) Multifrequency Analysis of Faults in Analog Circuits. *IEEE Design & Test of Computers*, Summer, p.70-80.

Su, C.; Chiang, S.; Jou, S.-J. (1995) Impulse Response fault model and Fault Extraction for Functional Level Analog Circuit Diagnosis. In: IEEE International Conference on CAD, *proceedings...*,p. 631-636.

Vazquez, D.; Rueda, A.; Huertas, J.L. (1993) On-line error detection for Continuous-time Mosfet-C Filters. In: European Solid-State Circuits Conference, *proceedings...* Sept.

Widrow, B.; Stearns, S.D. (1985) Adaptive signal processing. Englewood Cliffs, N.J.: Prentice-Hall. 474p.

7 BIOGRAPHY

Marcelo Negreiros was born in Porto Alegre, Brasil, on Oct. 27, 1969. He received the electrical engineer degree from the Federal University of Rio Grande do Sul (UFRGS) in 1992, and the M.S. degree in Engineering in 1994. He is now at the Electrical Engineering department /UFRGS. Areas of interest: digital signal processing and adaptive systems.

Luigi Carro was born in Porto Alegre, Brasil, on Sept. 8, 1962. He received the electrical engineer degree from the Federal University of Rio Grande do Sul (UFRGS) in 1985, M.S. and Ph.D. degrees in Computer Science in 1989 and 1996, respectively. He was at ST-Microelectronics R&D center, Agrate, Italia, from 1989-1991. Mr. Carro is a lecturer at the Electrical Engineering department, UFRGS. Areas of interest: VLSI processors and synthesis of complex systems.