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An architecture for a 12 bits, low power integrated CMOS pressure sensor with thermal compensation

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Abstract

The design of a CMOS piezoresistive pressure sensor with mixed-signal circuitry to provide a digital output is described. The on-chip sensor is a monolithic silicon etched diaphragm, built via post-processing, with the strain gauge composed of diffused resistors in an active Wheatstone bridge configuration. The amplifier's bridge is chopped for efficient low frequency noise and amplifier offset cancellations. The A-to-D converter is based on a second-order $\Delta\Sigma$ modulator including 6 bits DAC units for sensor offset calibration. The circuit has temperature compensation of both full output scale and offset. Overall system resolution is 12 bits, corresponding to 72dB dynamic range, while the pressure range is 0 to 50kPa. Pulsed mode operation allows for low power dissipation (<1mW) at 3V supply voltage. This device is intended to be used in biomedical applications such as non-invasive blood pressure measurement and diagnostics.

Keywords

Pressure sensor interface, post-processing, MEMS, active Wheatstone bridge, $\Delta\Sigma$ modulator, temperature compensation

VLSI: Integrated Systems on Silicon R. Reis & L. Claesen (Eds.)

1 INTRODUCTION

Pressure sensors still continue being an important device for the industrial and biomedical fields due to its wide application range. Much work has been done to fabricate pressure sensors monolithically integrated with its necessary on-chip electronic circuitry for signal processing, temperature compensation and parameter calibration, and good results have been presented (Jakob, 1993; J. Dziuban *et al.*, 1994). Nevertheless, characteristics such as area, power consumption, and resolution have not been optimised. This work combines two key ideas to develop a fully integrated pressure sensor. The first one is the conception of an architecture able to attain high resolution, low power consumption and thermal compensation. The second idea is to employ post-processing for the final MEMS structure fabrication. So, it is possible to fabricate a highly reliable, robust device based on standard industrial technologies.

The sensor device consists of a membrane created on a silicon wafer by anisotropic etching from the backside. The target application is blood pressure measurements directly in the patient blood stream. Therefore, pressure and temperature range are 0 to 50kPa and 10 to 45°C, respectively, over which the sensor is calibrated for both offset and sensitivity. The sensor system consists of:

- A chopped active Wheatstone bridge based on a fully differential amplifier that effectively doubles the sensitivity and allows sensor pulsed operation.
- A 12-bit A/D converter implemented via a second order ΔΣ modulator.
- Auxiliary DAC units for offset calibration.
- Digitally programmable compensation of sensor sensitivity (TCS) and offset (TCO) dependencies on temperature.
- Reference voltage and current generators based on a bandgap circuit.

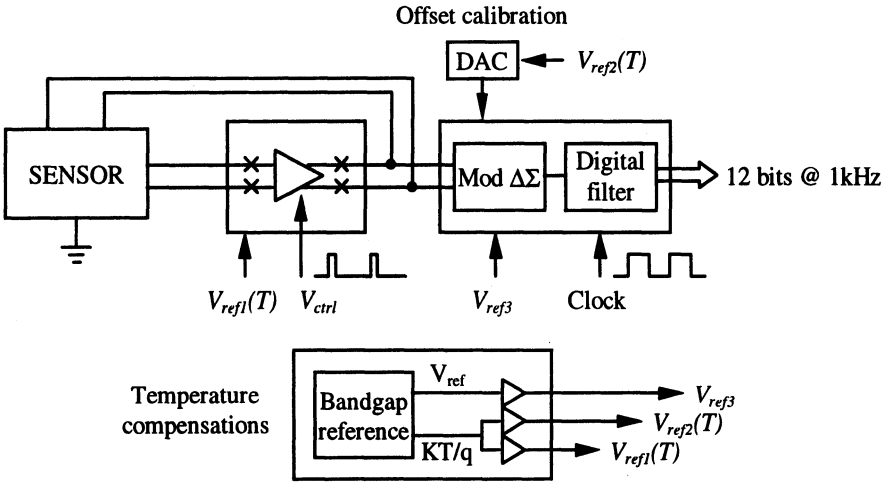


Figure 1 Sensor system architecture.

The sensor system architecture is shown in Figure 1. Section 2 describes the sensor itself as well as its fabrication process; section 3 shows the active bridge architecture; section 4 explains the design of the active bridge amplifier; section 5 shows the A/D converter; and section 6 presents the temperature compensation circuits. Finally, some important conclusions are presented in section 7.

2 SENSOR DEVICE

The sensor device design and final fabrication (post-processing) are done in our laboratory. The sensor contains two resistive networks properly placed in a square silicon diaphragm for optimal sensitivity. Each resistive branch has two diffused resistors of 1KΩ positioned transversal and longitudinally with respect to the diaphragm edges; the membrane thickness is 10μm. This kind of microsensor explores the silicon piezoresisitve effect produced by the membrane deflection as consequence of the applied pressure. The optimum resistor placement is determined using finite element simulations with ANSYS (ANSYS Inc., 1990).

The diaphragm was obtained through anisotropic etch of the silicon bulk. The KOH solution concentration for the anisotropic etch was 27% at 85°C. First, a Si_3N_4-PECVD layer (low temperature process) as passivation mask was deposited. After that, the passivation layer window was obtained via Reactive Ion Etching (RIE) on the Si_3N_4 layer making a normal photolithography process with an Electronic Visions Optical aligner. The surface containing CMOS circuitry was protected against wire bonding pad etching employing a mechanical device. Then, we made a fast dip in HF solution at 1,0W% to strip out the native oxide on the exposed silicon area. Finally, we could sink water in the KOH solution to obtain the pressure sensor diaphragm on the wafer surface.

3 ACTIVE BRIDGE ARCHITECTURE

Looking in Figure 2 (a) and assuming V_{drive} and ε are the voltage applied on the bridge and the relative branch resistance variation, respectively, the output voltage is given by:

$$V_{out} = [\tfrac{1}{2}(1-\varepsilon) - \tfrac{1}{2}(1+\varepsilon)] \cdot V_{drive} = -\varepsilon \cdot V_{drive} \cdot \quad (1)$$

By contrast, the active bridge in Figure 3b effectively doubles the sensor sensitivity due to the resistors works as a feedback network around a fully differential operational amplifier. In this case, the common mode feedback circuit keeps the output common mode voltage equal to the input reference signal:

$$\tfrac{1}{2}(V^+ - V^-) = V_{drive} = V_{ref1}(T) \cdot \quad (2)$$

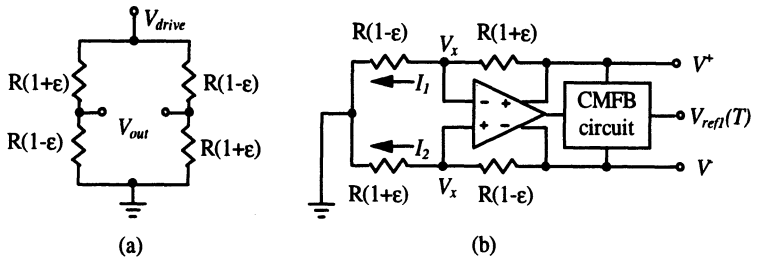


Figure 2 Passive (a) and active (b) piezoresistive bridges.

Considering the amplifier inputs are at the V_x voltage, the branch currents are:

$$I_1 = [V_x/(1-\varepsilon)],\ I_2 = [V_x/(1-\varepsilon)]. \tag{3}$$

Therefore, the output voltages are:

$$V^+ = -[2/(1-\varepsilon)]\cdot V_x,\ V^- = -[2/(1+\varepsilon)]\cdot V_x. \tag{4}$$

And, using equations (2) and (4), we can easily derive:

$$V_{out} = V^+ - V^- = -2\cdot\varepsilon\cdot V_{drive}. \tag{5}$$

For adequate attenuation of both amplifier offset and *1/f* noise, the amplifier is chopped at 250kHz, half of the converter clock frequency. The chopping frequency is chosen high enough so that it lies above the *1/f* corner frequency (f_k in Figure 3(a)) and still permits a low-power amplifier design. On the other hand, besides having doubled sensitivity for the same drive voltage, the active bridge allows for sensor pulsed operation by switching its power supply. This fact can be explored to save power consumption since sampling at the following switched capacitor circuit corresponds to a very short time. However, to reduce overall power dissipation, the duty cycle value should be carefully chosen. As shown in Figure 3 (b), despite resistor consumption is proportional to the duty cycle the amplifier consumption has an opposite tendency due to it charges and discharges the load capacitance. Typical slew rate requirements (50v/μs) will make such power dissipation inversely proportional to the pulse duty cycle. An optimum point exists which is characteristic of the amplifier design and it has been found to be 25%. A general description of the control waveforms is illustrated in Figure 4.

4 ACTIVE BRIDGE AMPLIFIER DESIGN

Figure 5 displays the two stages of the bridge amplifier topology. The second stage, composed of the driver transistors M11 and M12, furnishes the current for

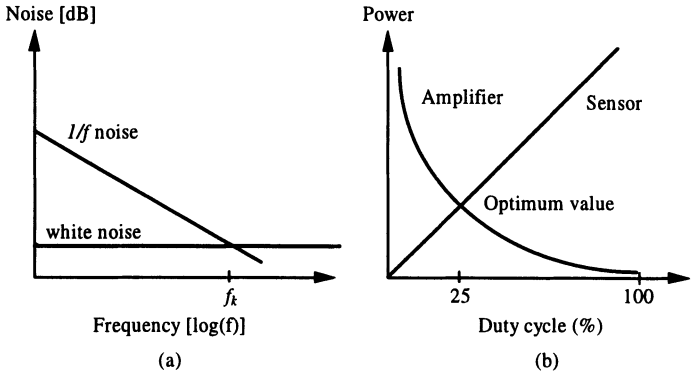


Figure 3 Amplifier noise (a) and power consumption vs. duty cycle percentage.

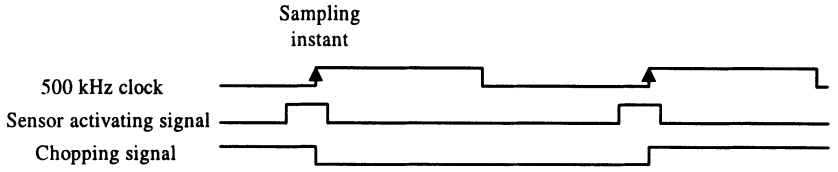


Figure 4 Timing of the control signals.

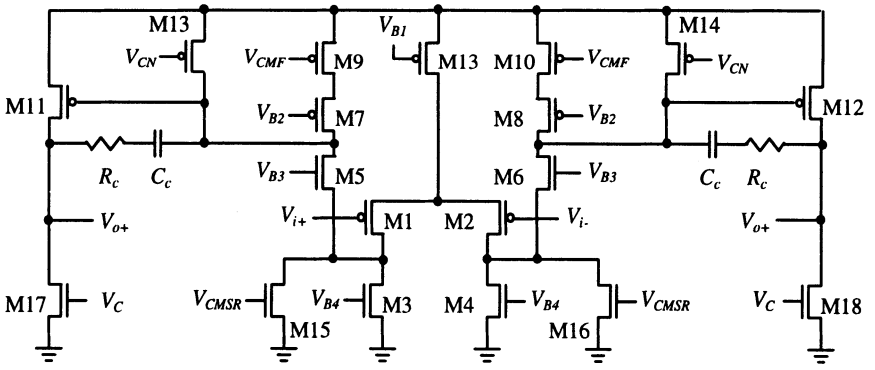


Figure 5 Schematic diagram of the two stages fully differential amplifier.

the sensor resistive branches, which constitute its actual load, with a resulting gain of 28 dB. The first stage is a folded cascode stage thereby providing an overall 98 dB gain at 3V supply voltage (see Figure 6). Design assumes a load capacitance of 5pF taking into account the diaphragm may be placed far from the amplifier although on the same chip. This load determines the transconductance of transistors M11-M12 driven a large sensor bias current (1.25mA). Thus, the remaining amplifier power consumption is negligible. Using the amplifier output stage to provide the sensor current together with the pulsed operation mode are the key issues determining the excellent power consumption level of the system.

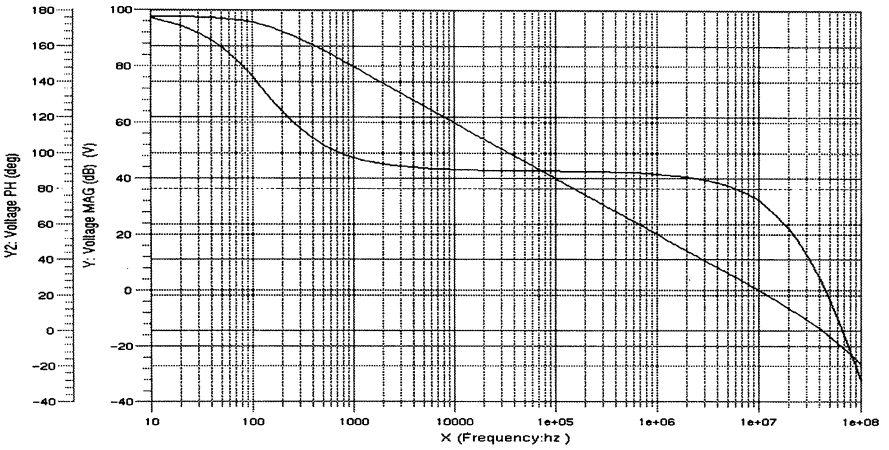


Figure 6 Bridge amplifier gain magnitude and phase responses.

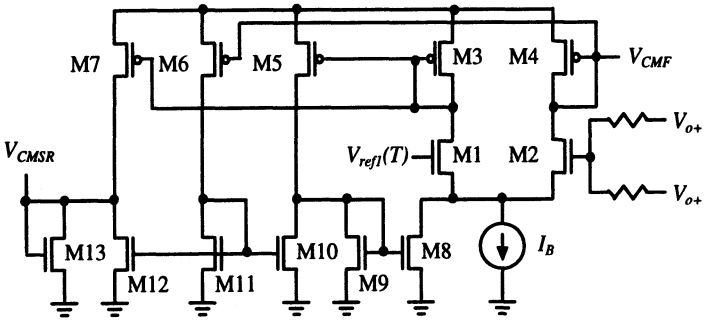


Figure 7 Schematic diagram of the common mode feedback circuit.

Note, in the common mode feedback circuit of the bridge amplifier shown in Figure 7, the reference voltage $V_{refl}(T)$ fix the drive voltage on the resistors, as verified by simulation in Figure 8. The common mode gain-bandwidth product of the CMFB circuit is actually larger than the differential one. It is due to the requirement of properly driving the amplifier through $V_{refl}(T)$, a common mode signal, with a very short pulse. To do that, the amplifier has an adaptive biasing network (Degrawe *et al.*, 1982) controlling its first stage (devices M15 and M16 governed by signal V_{CMSR}, in Figure 5). Also, observe the pulsed mode operation of the bridge amplifier is achieved including the power-on signals V_C and V_{CN}.

5 ANALOG TO DIGITAL CONVERTER

We employ a ΔΣ modulator and its associated digital decimator filter to convert the sensor output voltage in a digital word. First order modulators require a dither

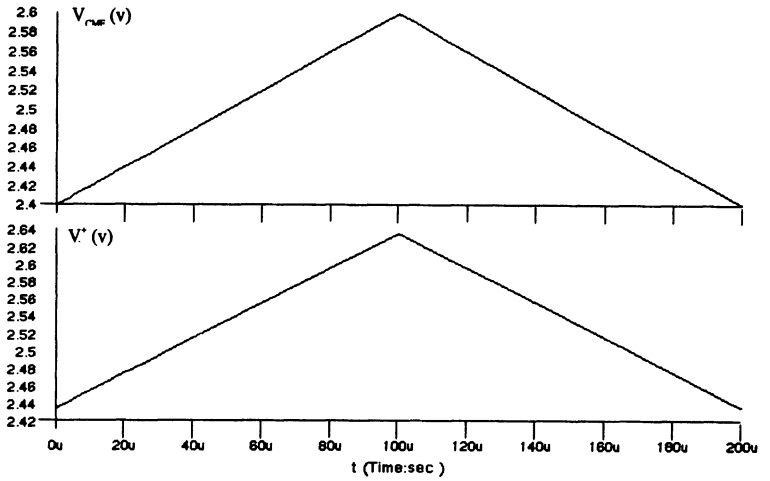


Figure 8 Simulation results of bridge amplifier for a common mode ramp signal.

signal to reduce unavoidable noise tones to acceptable levels, while high-order modulators suffer from potential instability. Hence, 2nd order architecture has become the most attractive option. The performance target in our design is 12 bits resolution, which is equivalent to 72dB dynamic range, over a 500Hz baseband. Using a 2nd order $\Delta\Sigma$ modulator, this performance can be attained with an oversampling ratio (OSR) of only 50 corresponding to 50kHz sampling frequency. However, for proper *1/f* noise cancellation in the chopped active bridge as well as the correlated noise owing to the double sampled 1st integrator, a 500kHz sampling frequency was chosen instead. This value does not unduly increase the overall power dissipation since the switched capacitor values are scaled down by the same factor as the clock frequency increases resulting in similar slew-rate requirements for the amplifiers. A fully differential architecture was adopted, as illustrated in Figure 9, following the same active bridge strategy and ensuring a high power supply rejection ratio and reduced clock feedthrough errors. An additional suppression of the signal-dependent charge injection is obtained using delayed phases for controlling all signal handling switches (Boser *et al.*, 1988). During phase *k1* the 1st integrator input is sampled onto the capacitors C_{I1} simultaneously with the amplifier auto-zeroing. During phase *k2*, the charge stored on C_{I1} is transferred to the integrator capacitance C_I. At the same time, the reference voltage V_{ref3} is either subtracted or added to the integrator depending on the comparator state by appropriately setting phases *x1* and *x2*. This allows to have only one positive reference voltage. The operation at the 2nd integrator is similar without auto-zeroing. Besides, due to the need of having the comparator state stable during the full sampling/transfer period, an additional latch is required whereas phases *x1*, *x2* are delayed by half the clock period respect to *y1*, *y2*. The sensor offset calibration is accomplished via auxiliary DAC blocks coupled with additional switched capacitor branches to the 1st integrator inputs.

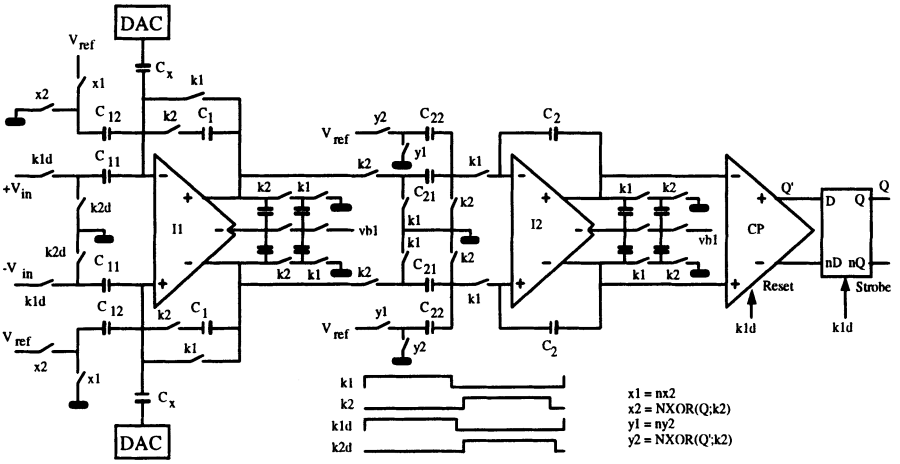


Figure 9 Second order ΔΣ modulator architecture.

Figure 10 shows the ΔΣ modulator amplifier's diagram. It is a single stage mirrored amplifier operating at a low supply voltage with minimum power dissipation (Gray *et al.*, 1993). High gain is obtained using wide channel length devices for output transistors M5-M8, which are biased at large overdrive voltages as allowed by frequency stability, while minimising both thermal and *1/f* noises. Moreover, we employ a switched-capacitor configuration for the common mode feedback circuit (see Figure 9). Finally, the simulated power spectrum for noise and 488Hz sinusoidal input signal is illustrated in Figure 11. Note the 75dB noise floor accomplishes the dynamic range target.

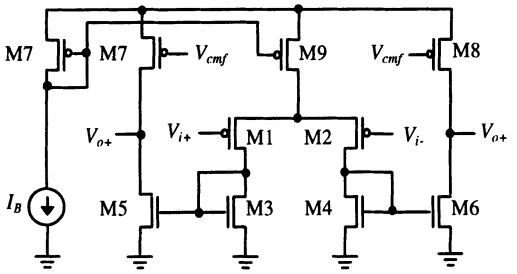
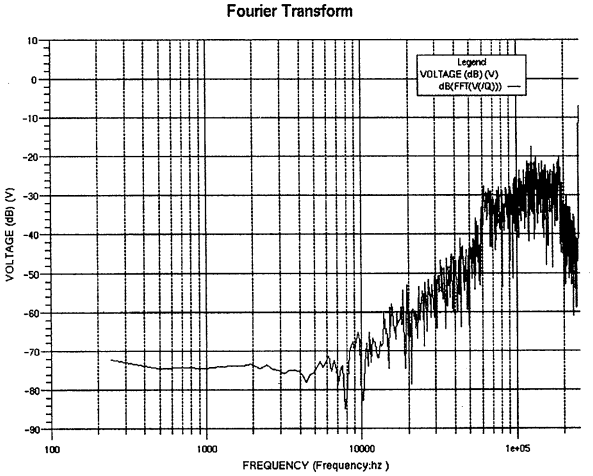


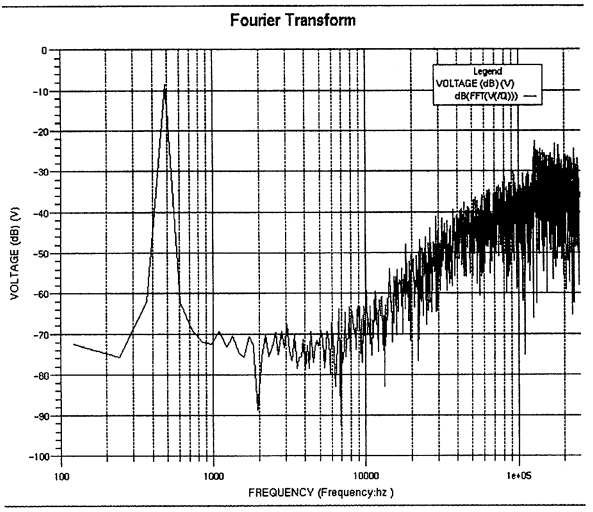
Figure 10 The ΔΣ modulator's amplifier.

6 TEMPERATURE COMPENSATION CIRCUITS

It is well-known diffused resistors have a temperature dependence (TCS) affecting strongly the sensor sensitivity. The main factors responsible for this effect are the temperature dependence of the resistance itself (TCR) and the gauge factor dependence on temperature (TCGF). Typical TCS values for Wheatstone bridges



(a)



(b)

Figure 11 Output spectrum of the ΔΣ modulator without excitation (a), and with a sinusoidal input signal (b).

using diffused resistors ranging from -1100 to -2300 ppm/°C. The most common method for temperature compensation in passive bridges is to modulate the drive voltage with a complementary temperature dependence. Figure 12 presents the block generator of the reference voltages $V_{ref1}(T)$, $V_{ref2}(T)$ and V_{ref3}, where the normalised reference voltage is given by:

$$[V_{ref}(T)/V_{ref}] = [1-(G/N)] \pm [2 \ln 8(k/q)]T \ . \qquad (6)$$

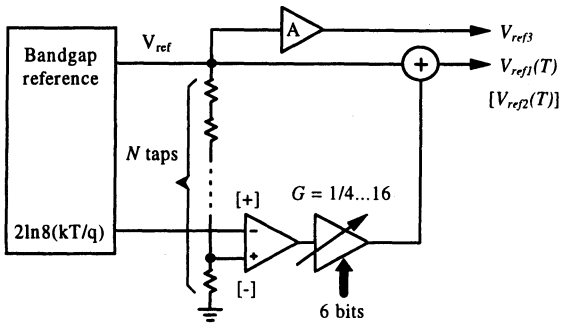


Figure 12 Diagram of the reference voltage circuit for temperature compensation.

where G is the gain of the programmable amplifier, and N is the number of the tap resistance. We employ positive temperature dependence in (6) to compensate TCS via $V_{ref1}(T)$, and negative dependence to compensate TCO via $V_{ref2}(T)$. The circuit in Figure 12 can neutralize sensitivity variations at different temperatures with 6 bits accuracy (64 steps) throughout the programmable gain amplifier. Likewise, it maintains the same output reference voltage V_{ref3}, defined at ambient temperature, independently of the amplifier gain.

7 CONCLUSIONS

A novel architecture, the most important subsystems and characteristics, and an approach for a full integration of a piezoresistive pressure sensor have been exposed. In accordance with our experimental results, we found it is feasible to make the MEMS structure (sensor element and signal processing circuitry) using the post-processing method. The membrane was built onto a substrate with similar characteristics encountered in the foundry wafers. The new architecture approach provides higher sensor sensitivity dissipating low power, permits obtaining the digital output employing a high performance AD converter, and includes thermal effect compensation techniques. The architecture characteristics indicate it is suitable in developing piezoresistive pressure sensors with high performance. The device has been designed for biomedical applications, specifically blood pressure measurements. However, the basic mixed-mode interface may support a wide variety of sensors and MEMS devices.

8 ACKNOWLEDGMENTS

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10 BIOGRAPHIES

Fernando Chavez received the B.S.E.E. degree from Valle University, Colombia, in 1985. In 1987 he was a visiting researcher at the Twente University, Netherlands. He joined to the Microelectronics Laboratory of the Valle University in 1988. During 1991-1993 he worked for the Information Technological Centre at Campinas, Brazil. In 1995 he received the M.S.E.E. degree from University of Campinas, Brazil. Nowadays, Mr. Chavez is working towards his PhD degree at University of São Paulo, Brazil. His main interest areas are sensor development and mixed-mode circuit design.

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Edgar Charry was born in Cali, Colombia. He received the M.Sc. degree in Electrical Engineering from the National Politechnique Inst., Mexico, in 1970, and the Ph.D. degree in Electrical Engineering from the University of São Paulo, Brazil, in 1974. From 1975 to 1980 he was head of the Microelectronics Laboratory's MOS Division at University of São Paulo. In 1987 he created and led the Microelectronics Laboratory of the Valle University, Colombia. He has been involved in all the microelectronics fields: device modelling, process technology, integrated circuit design, and test with both devices CMOS and HEMT. His current research interests are in high performance and high frequency analog integrated circuits for telecommunications and signal processing. Also, he is working with MEMS technology, specifically in silicon sensors.

Carlos Azeredo Leme graduated in Electrical Engineering at IST, Lisbon, in 1986. In 1990, he received the M.Sc. degree in Electronic Engineering from the same university. In 1991 he joined to the Physical Electronics Laboratory at ETH, Zurich, where he was involved in design of CMOS sensor interfaces. He obtained his Ph.D. degree from ETH in 1993. Since 1994, he is with the Group of Integrated Circuits and Systems at IST, Lisbon. His main areas of interest are high resolution A/D conversion and mixed-signal circuits for telecommunications.