A Quantum Hydrodynamic Simulation of Strained Nanoscale VLSI Device

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Abstract. Strained silicon field effect transistor (FET) has been known for enhancing carrier mobility. The stained Si channel thickness, the $Si_{1-x}Ge_x$ composition fraction and the $Si_{1-x}Ge_x$ layer thickness are three crucial parameters for designing strained Si/SiGe MOSFET. Mobility enhancement and device reliability may be unnecessarily conservative. In this paper, numerical investigation of drain current, gate leakage and threshold voltage for strained Si/SiGe MOSFET are simulated under different device profiles. According to our results, the optimal combination of parameters are as follows: stained Si channel thickness is 7 nm, Ge content is 20%, and the $Si_{1-x}Ge_x$ layer thickness should be chosen between 20~50 nm.

1 Introduction

The introduction of strained Si and SiGe in CMOS technology is a means of improving the performance of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) in the deep submicron era [1-2]. A general approach to introduce biaxial tensile strain is using a virtual substrate of SiGe [1-2]. The underlying SiGe layer serves as an anchor to constrain the lattice of the strained silicon on top. Therefore, the electron mobility, and hence nMOSFET drive current performance, is enhanced. The stained Si channel thickness (T_{Si}), the $Si_{1-x}Ge_x$ composition fraction (x) and the $Si_{1-x}Ge_x$ layer thickness (T_{SG}) are three crucial parameters for designing strained Si/SiGe MOSFET. In this study, computer-aided design (CAD) approach is used to optimize the structure of strained Si/SiGe device. Drain current, gate leakage and threshold voltage are simulated and discussed.

2 Quantum Transport Models

The density-gradient (DG) model is considered to couple with the classical transport models. The hydrodynamic model (HD) [3] provides a very good compromise of velocity overshoot and the impact ionization generation rates. For the sake of saving computing time, DD model is used while drain bias (V_D) is low (< 0.1). For high-drain bias, hydrodynamic model is considered. The DD model is given as

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$$\nabla\varepsilon \cdot \nabla\phi = -q(p - n + N_D - N_A), \quad (1)$$
$$q\,\partial n/\partial t - \nabla \cdot \mathbf{J_n} = -qR, \quad (2)$$
$$q\,\partial p/\partial t + \nabla \cdot \mathbf{J_p} = -qR, \quad (3)$$

where $\mathbf{J}_n = -qn\mu_n\nabla\phi_n$ and $\mathbf{J}_p = -qp\mu_p\nabla\phi_p$ are the electron and hole current densities. $\phi_n = -\nabla\phi - \nabla n(kT/\mu_n)$ and $\phi_p = -\nabla\phi + \nabla p(kT/\mu_n)$. R is the generation-recombination term. In the hydrodynamic model, the carrier temperatures T_n and T_p are not assumed to be equal to lattice temperature T_L, together with DD model, up to three additional equations can be solved to find the temperatures, which are

$$\partial W_n/\partial t + \nabla \cdot \mathbf{S_n} = \mathbf{J_n} \cdot \nabla E_C + dW_n/dt\,|_{coll}, \quad (4)$$
$$\partial W_p/\partial t + \nabla \cdot \mathbf{S_p} = \mathbf{J_p} \cdot \nabla E_V + dW_p/dt\,|_{coll}, \quad (5)$$
$$\partial W_L/\partial t + \nabla \cdot \mathbf{S_L} = dW_L/dt\,|_{coll}, \quad (6)$$

where $\mathbf{J}_n = \mu_n(n\nabla E_C + k_BT_n\nabla n + f_n^{td}k_Bn\nabla T_n - 1.5nk_BT_n\nabla\ln m_e)$ and $\mathbf{J}_p = \mu_p(p\nabla E_V - k_BT_p\nabla p - f_p^{td}k_Bp\nabla T_p - 1.5pk_BT_p\nabla\ln m_h)$ are current densities. $\mathbf{S_L}$, $\mathbf{S_n}$ and $\mathbf{S_p}$ are energy fluxes and $dW_n/dt\,|_{coll}$, $dW_p/dt\,|_{coll}$ and $dW_L/dt\,|_{coll}$ are the collision terms.

According to DG method, an additional potential Λ is introduced into the classical density formula, which reads: $n = N_C\exp((E_F - E_C - \Lambda)/k_BT)$. In this study, Λ is given as $\Lambda = \gamma\hbar^2\beta\left[\nabla^2(\phi + \Lambda) - \beta(\nabla\phi + \nabla\Lambda)^2/2\right]/12m$ [4]. The quantum transport systematic equations are discretized by the box discretization [5] and solved. After the drain current (I_D) is obtained, the gate leakage (I_G) and threshold voltage (V_{TH}) are determined.

3 Simulated Results and Discussion

In the numerical studies, a 40 nm strained Si/SiGe nMOSFETs is simulated. The device profile and simulated scenario are given in Fig. 1. According to previous experimental studies [1-2], the effects of interface trap are also considered in the numerical simulation.

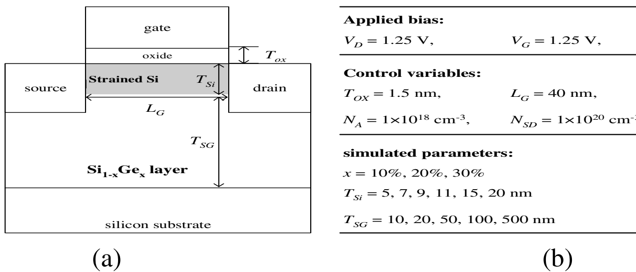

Fig. 1. (a) Simulated strained Si/SiGe nMOSFET and (b) scenario of simulation

Figures 2 and 3 illustrate part of the results to show the dependence of I_D and I_G on T_{SG}, T_{Si} and x, respectively. Fig. 2(a) demonstrates increasing device performance with increasing Ge content in the SiGe layer due to higher strain in the Si channel. However, a higher Ge content also induced higher gate leakage, which is caused by mismatch of lattice and diffusion of Ge. I_G is shown in Fig. 3(a). Fig. 2(b) and Fig. 3(b) illustrate I_D and I_G under different T_{Si} with x = 20% and T_{SG} = 20 nm. A thinner T_{Si} performs a larger I_D. The reason is that a thin strained Si channel can prevent the stress relaxation and present a better performance. The lattice mismatch proportionally decreases with increasing T_{Si}. In another word, the relaxation of tensile stress in the strained Si channel could be suppressed by decreasing T_{Si}, *i.e.*, the mobility enhancement would be larger in the thin T_{Si} device than in the thick T_{Si} device. The observation in the nanoscale device is different to long-channel devices. Unfortunately, a thin T_{Si} may induce large interface trap caused by Ge diffusion. In this study, I_D and I_G of T_{Si} = 5 nm is the largest. I_G of T_{Si} = 7, 9, 11 and 15 do not show much difference. Fig. 2(c) and 3(c) demonstrate I_D and I_G dependence on T_{SG}. A thicker T_{SG}

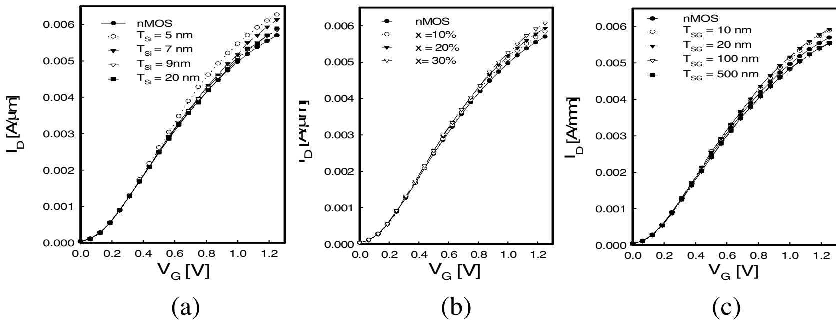

Fig. 2. Simulated I_D-V_G curves for (a) T_{SG} = 20 nm, x = 20 %, (a) T_{SG} = 20 nm, T_{Si} = 9 nm and (c) T_{Si} = 9 nm, x = 20 %

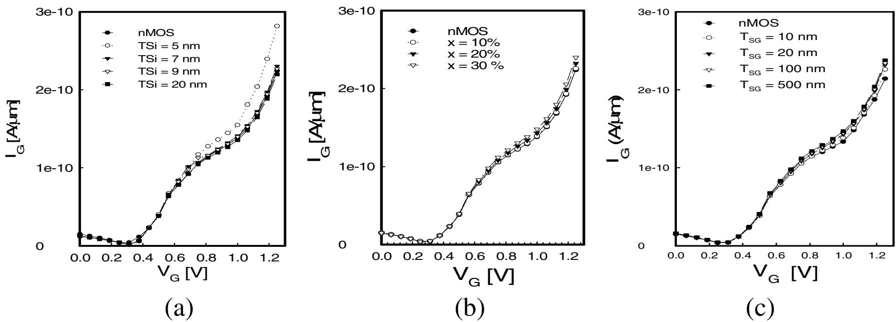

Fig. 3. Simulated I_G-V_G curves for (a) T_{SG} = 20 nm, x = 20 %, (a) T_{SG} = 20 nm, T_{Si} = 9 nm and (c) T_{Si} = 9 nm, x = 20 %

provides a larger stress, but a larger number of lattice mismatches is also induced. Moreover, a thicker T_{SG} may increase Ge diffusion to MOS interface, which contributes to an increased interface state.

For further discussion, Fig. 4 illustrates the V_{TH} shift (V), I_D enhancement (%) and $\Delta I_G/I_G$ (%) of the whole simulation scenario. According to the figure, if $T_{Si} \geqq$ 14 nm, V_{TH} shift may be larger than 0.01 V. As $T_{Si} \leqq$ 14 nm, V_{TH} shift is small enough to be neglected. From Fig. 4 (b), the largest I_D enhancement is achieved by T_{Si} = 5 nm, T_{SG} = 20 nm and $Si_{70\%}Ge_{30\%}$. However, the I_G induced by the interfacial state is too large to be accepted. T_{Si} = 5 nm presents a sudden increase of interfacial states. $\Delta I_G/I_G$ is given in Fig. 4(c). T_{Si} = 7 nm is chosen. Although x = 30% may have a better improvement of drain current, it also have a serious problem of Ge diffusion. Therefore, x = 20% is suggested. Since a thin SiGe layer cannot provide enough stress to improve drain current, the best case occurs between T_{SG} = 20 ~ 50 nm.

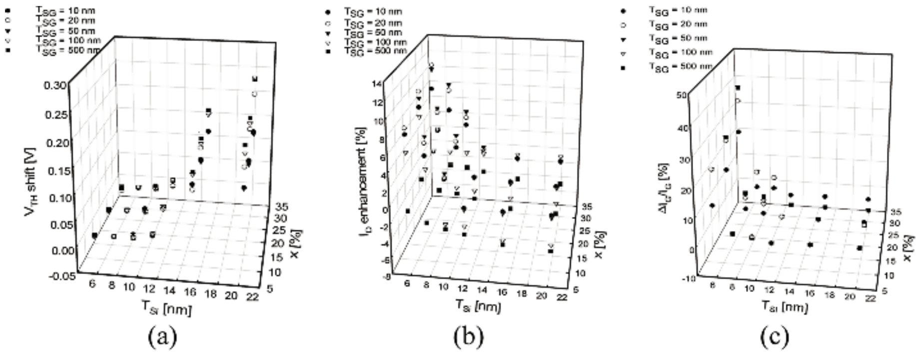

Fig. 4. (a) V_{TH} shift (V), (b) I_D enhancement (%), and (c) $\Delta I_G/I_G$ (%) for the simulated scenario

4 Conclusions

In this study, optimal profile of strained Si/SiGe device is suggested by numerical simulation. Hydrodynamic model is employed and the effect of interface state is considered in the simulation. Considering the improvement of performance and reliability, we suggested that the optimal stained Si channel thickness is 7 nm, Ge content is 20%, and the $Si_{1-x}Ge_x$ layer thickness is between 20~50 nm. The optimal design may obtain an 8~11% improvement of performance and maintain the same level of gate leakage for a 40 nm nMOSFET.

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