EFFECT OF POWER OPTIMIZATIONS ON SOFT ERROR RATE

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Abstract Due to technology scaling, devices are getting smaller, faster and operating at lower voltages. The reduced nodal capacitances and supply voltages coupled with more dense and larger chips are increasing soft errors and making them an important design constraint. As designers aggressively address the excessive power consumption problem that is considered as a major design limiter they need to be aware of the impact of the power optimizations on the soft error rates(SER). In this chapter, we analyze the effect of increasing threshold voltage and reducing the operating voltages, widely used for reducing power consumption, on the soft error rate. While reducing the operating voltage increases the susceptibility to soft errors, increasing the threshold voltages offers mixed results. We find that increasing threshold voltage (V_t) improves SER of transmission gate based flip-flops, but can adversely affect the robustness of combinational logic due to the effect of higher threshold voltages on the attenuation of transient pulses. We also show that, in certain circuits, clever use of high V_t can improve the robustness to soft errors.

Keywords: Low Power VLSI, Power Optimizations, Soft Errors, Single Event Upset, Reliability, Noise Immunity,

1. Introduction

As silicon industry enters the nanometer regime, it is facing new challenges on several fronts. In the past, aggressive technology scaling has improved performance, reduced power consumption, and helped the industry obey Moore's law. In the sub-130nm regime, supply voltage is also scaled down to reduce the power consumption. To compensate for the lower supply voltage, the threshold voltage of the device is also reduced. This increases the subthreshold leakage [8]. In addition, the ultra thin gate oxides increase the tunneling probability of the electrons, thus increasing the gate leakage. Furthermore, the dense integration of the transistors along with increased leakage currents makes power density an important concern in newer technologies. Hence power, by many, is

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regarded as the most significant road block in realizing the benefits of scaling for next generation. Consequently various optimizations for reducing power consumption have been proposed [29, 25]. This chapter will mainly examine the impact of higher threshold voltage devices and supply voltage scaling techniques, used for reducing power, on soft error rates(SER).

The direct consequence of the lower supply voltage is lower signal to noise ratio (SNR). This results in increased susceptibility of circuits to noise sources like soft errors. In contrast, the effect of the higher V_t devices is not straight forward. Soft errors are transient circuit errors that are induced by external radiations. Radiation from cosmic rays or packaging material induces a localized ionization which, can lead to spurious pulses or upset the internal data states. While these errors cause a transient pulse, the circuit itself is not damaged. In combinatorial logic, if this transient pulse is latched by a memory element like a latch or a register, the transient pulse translates to a soft error which corrupts the computation. In memory elements like SRAM, latches and registers, these errors change the stored values of the bits. In SRAM based FPGAs, the configuration is stored in the SRAM cells, which when upset causes a change in the configuration and hence leads to an error in firmware. This error, though correctable, will lead to wrong computation until the configuration is reloaded. Conventional ways of reducing the soft error rates include adding redundancy, increasing nodal capacitance and using error correcting codes. In this work, we analyze the effect of increasing the threshold voltage (V_t) of the device and supply voltage scaling on soft errors in standard memory elements like SRAMs and flip-flops and on combinational circuits like inverters, nand gates and adders, which represent the most common CMOS logic styles. We believe such an analysis is very important because it helps us in making intelligent design choices that reduce leakage power consumption and improve the reliability of the next generation circuits.

The chapter is organized as follows: Section 2 presents the background on soft errors. Section 3 presents the experimental methodology that is used to examine soft errors in circuits. Section 4 focuses on the impact of supply voltage scaling and high V_t devices on SER. It also discusses the detailed results of the experimental analysis of SER on different circuits. It also presents guidelines to implement delay balancing to reduce power and improve robustness to soft errors at the same time. Section 5 presents the conclusions.

2. Soft Errors

When energy particles hit a silicon substrate, the kinetic energy of the particle generates electron hole pairs as they pass through p-n junctions. Some of

the deposited charge will recombine to form a very short duration current pulse which causes a soft error. In memory elements, these can cause bit flips, but in combinational circuits they can cause a temporary change in the output. In combinational logic such a pulse is naturally attenuated, but if a transient pulse is latched, it corrupts the logic state of the circuit [7, 10].

There are three principle sources of soft errors: alpha particles, high-energy cosmic ray induced neutrons, and neutron induced boron-10(^{10}B) fission. Alpha particles are emitted from decaying elements like Lead present in the packaging materials. Alpha particles are also created due to the interaction of cosmic ray thermal neutron with ^{10}B present in the P-type regions of the devices [6]. A single alpha particle can generate anywhere from 4 to 16fC/m over its entire range.

The galactic flux of primary cosmic rays (mainly consisting of protons) is very large, about 100,000 particles/m^2s as compared to the much lower final flux (mainly consisting of neutrons) at sea level of about 360 particles/m^2s [30]. Only few of the galactic particles have adequate energy to penetrate the earth's atmosphere. The intensity of these neutron radiations depends on altitude, geomagnetic region and solar cycles [30]. The primary reaction by which cosmic ray induced neutrons cause SER is by silicon recoil. The impinging neutrons knock off the silicon from its lattice. The displaced silicon nucleus breaks down into smaller fragments each of which generates some charge. The charge density for silicon recoils is about 25 to 150fC/m, which is more than that from alpha particle strike. So it has a higher potential to upset the circuit.

The third significant source of ionizing particles is from the neutron induced ^{10}B fission. ^{10}B, an isotope of p-type dopant (about 19.9%), is unstable and on impact from neutron it absorbs the neutrons and breaks apart with the release of an alpha particle and ^{7}Li (Lithium). Both these by-products are capable of inducing soft errors. To reduce SER due to alpha particle induced soft errors, one can use ^{10}B free materials and shield the circuit so that components with higher alpha emission rates are physically isolated from the sensitive circuits. Such solutions though effective for alpha generated soft errors, are generally ineffective against the neutrons as they are highly penetrative.

The issue of soft errors was studied in the context of scaling trends of microelectronics as early as in 1962 [28]. Interestingly, the forecast from this study that the lower limit on supply voltage reduction will be imposed by soft errors is shared by a recent work from researchers at Intel [9]. However, most works on radiation effects, since the work in 1962, focused on space applications rather than terrestrial applications. As earth's atmosphere shields most cosmic

ray particles from reaching the ground and charge per circuit node used to be large, soft errors on terrestrial devices has not been important until recently. Recent works [14, 15, 26] have shown the effect of technology scaling on soft errors. In [30], a study on radiation flux noted that particles of lower energy occur far more frequently than particles of higher energy. So it can be seen that as CMOS device sizes decrease, they are more easily affected by these lower energy particles, potentially leading to a much higher rate of soft errors.

According to [15], the soft error rate of memory element is expressed as Equation 1:

$$SER \propto N_{flux} * CS * exp\frac{-Q_{critical}}{Q_s} \quad (1)$$

where,

N_{flux} is the intensity of neutron flux,
CS is the area of cross section of the node,
Q_s is the charge collection efficiency,
$Q_{critical}$ is the charge that is stored at the node and hence is equal to $VDD * C_{node}$, where VDD is the supply voltage and
C_{node} is the nodal capacitance.

Hence any reduction in supply voltage or nodal capacitance increases the soft error rate. The soft error rate is also proportional to the area of the node CS. Smaller devices have lesser area and hence are less susceptible for an upset. But lower $Q_{critical}$ coupled with higher density of the devices and larger dies ensures an increase in soft errors for each new generation [27, 26, 15].

In combinational circuits soft errors are dependent on many factors. A transient glitch due a radiation event at a node alters the execution and generates a computation error only if the resultant glitch causes a change in the output and also such a change in the output is latched by a register. These factors derate the soft errors rates in logic. Hence in logic circuits, the

$$SER \propto N_{flux} * CS * Prob_G * Prob_P * Prob_L \quad (2)$$

Where,

$Prob_G$ is the probability that an transient pulse is generated for a particle strike at that node,
$Prob_P$ is the probability that the generated transient pulse propagates through the logic network,
$Prob_L$ is the probability that the transient pulse is latched at the output.

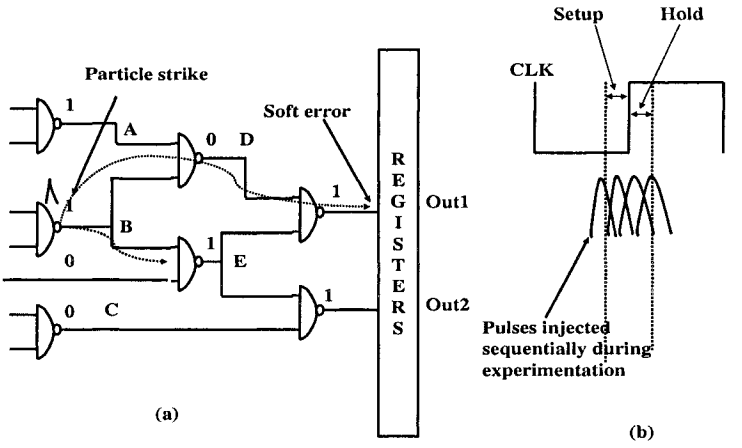

Figure 1. Circuit level evaluation of soft errors in logic circuit

For static CMOS logic, all the factors except $Prob_G$ are dependent on the circuit structure, inputs to the circuit, operating voltage and technology.

3. Methodology for circuit level analysis of soft errors

For a soft error to occur at a specific node in a circuit, the collected charge Q at that particular node should be greater than $Q_{critical}$. $Q_{critical}$ is be defined as the minimum charge collected due to a particle strike that can cause a change in the output. If the charge generated by a particle strike at a node is more than $Q_{critical}$, the generated pulse is latched, resulting in a bit flip. This concept of critical charge is generally used to estimate the sensitivity of SER. The value of $Q_{critical}$ can be found by measuring the current required to flip a memory cell and derived using Equation 3. The particle strike itself is modeled as a piece wise linear current waveform where the waveform's peak accounts for funneling charge collection and the waveform's tail accounts for diffusion charge collection. By changing the magnitude of the peak of the waveform and appropriately scaling the waveform, we try to find the minimum height for which the wrong value is stored in the memory element. A similar approach has been used in prior work [26].

In a logic circuit, a transient change in the value of the circuit does not affect the results of a computation unless it is captured in a memory element like a

flip- flop. A logic error can be masked by logical masking, electrical masking and latching- window masking [16]. This is illustrated in the Figure 1(a). In the Figure 1(a), the error pulse generated at the node *B*, will translate into an error at node *Out1* on the path *B-D-Out1*, but not on the node *Out2* using the path *B-E-Out2*, this is called *logical masking*. Next the magnitude of the electrical pulse reaching the output is usually damped by the electrically properties of the gates, such damping is referred to as *electrical masking*. In addition, such a pulse reaching the input of the register should also satisfy the register's timing constraints namely, the pulse should arrive within the hold and setup time of the register. If the error pulse violates these timing constraints, the pulse is not captured by the register, this is masking is called *latching window masking*. For our study, the circuits were setup such that an error pulse generated by an injected current pulse is always translated to an error at the output. Hence, the circuits were setup to prevent the masking effects. For memory elements, the internal nodes, where the logical value is stored as charge, were chosen for injecting the current pulse.

The actual magnitude of the charge is given by Equation 3.

$$Q_{critical} = \int_0^{T_f} I_d dt \tag{3}$$

Where, I_d is the drain current induced by the charged particle. T_f is the flipping time and in memory circuits it can be defined as the point in time when the feedback mechanism of the back-to-back inverter will take over from the incident ion's current. For logic circuits, T_f is simply the duration of the pulse. We inject a pulse such that it reaches the input of the register within the latching window and repeat this procedure such that we sweep the entire latching window, as shown in Figure 1(b). Among these pulses, we choose the pulse which can be injected closest to the hold time and still cause an error. Next we attempt to change the magnitude of this pulse to determine the minimum value of the pulse that can cause a error. The $Q_{critical}$ of the pulse is determined using the formulation provided by Equation 3. In this work, we focus primarily on $Q_{critical}$ in comparing the SER of our designs, since the other parameters, such as charge collection efficiency are quite similar across designs. In [12, 22] we have characterized SER of different SRAM and flip-flop designs using similar procedure. In our study we use two types of designs; memory elements which include 6T-SRAM, asymmetric SRAMs(ASRAM), flip-flops, and logic elements which include 6-inverter chain, 4-FO4 nand chain, 1-bit transmission gate (TG) based adders. All the circuits are custom designed using 70nm Berkeley predictive technology [1] and the netlists are extracted. The netlists are simulated using Hspice. The normal V_t of these devices is 0.22V, and the supply voltage of 1V is used. V_t is changed using *delvto* option of Hspice [3].

Delvto changes the V_t of the transistors by the amount specified. We analyzed all circuits by changing V_t by 0.1V and 0.2V for both PMOS and NMOS.

4. Power and Soft Errors

Power consumption is a major design constraint towards building more powerful chips and systems. Supply voltages have continued to scale down with feature size with every technology generation. The transistor threshold voltage has been scaled down commensurate with the supply voltage scaling in order to maintain a high drive current to avoid performance penalties. However, the threshold voltage scaling results in the substantial increase of the subthreshold leakage current [8]. Hence, as technology scales, the leakage power consumed in circuits increases. On the other hand, even though the operating voltage is reduced the dynamic power increases due to higher operating frequency of the new generation circuits. Subsequently, there have been several efforts spanning from the circuit level to the architectural level at reducing the energy consumption (both dynamic and leakage). Circuit mechanisms include adaptive substrate biasing, dynamic supply scaling, dynamic frequency scaling, and supply gating [29, 25]. Many of the circuit techniques have been exploited at the architectural level to control leakage at the cache bank and cache line granularities. These optimizations influence the susceptibility of the circuits to soft errors. The subsequent sections will present the effect of two of the widely used power reduction techniques namely, reducing supply voltage using clustered voltage designs and increasing the threshold voltage, on soft error rates. In the Section 4.3, we will also address the issue of delay balancing in the context of high V_t devices.

4.1 Impact of supply voltage scaling in clustered voltage designs on soft error rate

Voltage scaling is a very common technique to reduce dynamic and leakage power consumption. Dynamic power of the circuit is proportional to the square of the supply voltage. Hence, supply voltage is decreased to reduce the power consumption of the circuit. To maximize the gains from this technique, it is a common practice to employ clustered voltage design. In clustered voltage design, parts of a circuit operate at a lower voltage. Figure 2, provides a schematic view of the clustered voltage design. Voltage level converters are used to move from one voltage cluster to another [19]. While no level convertering logic is needed to move from a high voltage cluster to a low voltage cluster, a level convertering circuit is need to when we move from a low voltage cluster to a high voltage cluster. Level converters are needed in the second case because in this case low voltage based devices need to drive high voltage based devices. In clustered voltage designs, the error can be generated in either

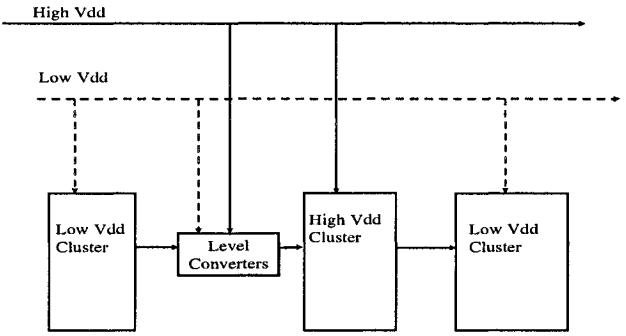

Figure 2. Clustered voltage design

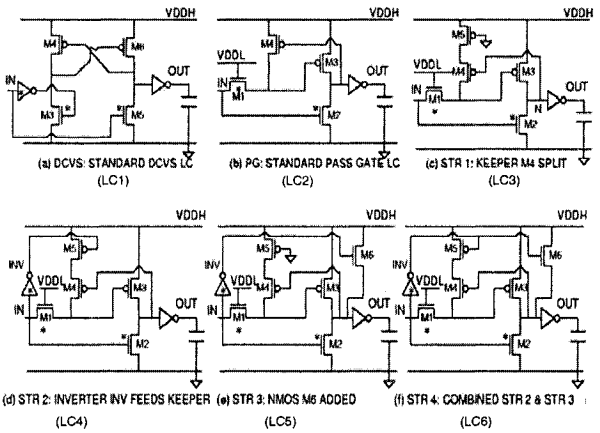

Figure 3. Level converters for clustered voltage design

the clusters or the level converters. Based on Equation 1 we know that SER increases exponential with reduction in $Q_{critical}$. $Q_{critical}$ is proportional to the supply voltage. Hence, the SER is exponentially dependent on supply voltages.

To examine the effect of supply voltage scaling in clustered voltage designs on SER, we analyzed the soft error susceptibly of six level converters. The level converters are shown in Figure 3. The effect of voltage scaling on the soft error susceptibility of six level converters is presented in Figure 4. We find that the $Q_{critical}$ of these level converters is linearly dependent on the supply voltage. Next we analyze the influence of voltage scaling in adders circuits on SER. The adder circuit can be considered as an example of a circuit representing the cluster. We find that, similar to level converters, the adders consume less power at a lower voltage but their $Q_{critical}$ is also reduced. Figure 5, presents the $Q_{critical}$ of a 4-bit Kogge-Stone adder at the output nodes for a transient pulse generated at the carry-in node. In comparison with Brent-Kung adders, Kogge-Stone adders are shown to have lesser $Q_{critical}$ and higher soft error rate [21]. While there are differences due to structural variations, in absolute $Q_{critical}$ values, the $Q_{critical}$ reduces as voltage reduces for both designs.

Supply voltage scaling is also employed to reduce the leakage energy. It is a common practice to reduce the supply voltage of the circuit when the circuit is not active and the overheads do not facilitate turning off the supply. For example in caches, when a cache line is not in use, the supply to the cache line can be reduced while still ensuring that the line retains the values [13]. On examining a custom designed cell, we found that a cell designed to operate at a voltage of 1V, can retain the values when the supply is reduced to 300mV. At 300mV the leakage is reduced by 70% but the $Q_{critical}$ also reduces by 65% [12, 20]. Hence there is a trade off between the power saved and the immunity to soft error. Based on the above results it can be seen that even though voltage scaling reduces the dynamic and static power, there is also a loss of immunity to soft errors.

4.2 Impact of high threshold voltage devices on SER

There are two distinct factors that affect soft error rates due to increase in threshold voltages. First, due to the physical properties of high V_t silicon, higher energy is requires to create electron-hole pairs in the substrate. This effect can potentially reduce SER. Second, higher V_t increases the gain and delay of circuits. This affects attenuation of the transient pulse.

4.2.1 Charge creation under high threshold voltages . This subsection gives a simplified theory of the semiconductors and we use this analysis to explain the phenomenon of charge creation under high V_t. Equation 4 represents the factors on which the threshold voltage depends.

$$V_t = V_{fb} + V_b + V_{ox} \tag{4}$$

where,

V_t is the threshold voltage of the MOS device

V_{fb} is the flat band voltage

V_b is the voltage drop across the depletion region at inversion

V_{ox} stands for potential drop across the gate oxide

When we change the threshold voltage of a device we change the flat band voltage(V_{fb}) of the device. Flat band voltage is the built in voltage offset across the MOS device [11]. It is the workfunction difference θ_{ms} which exists between polygate and silicon. By increasing the threshold voltage, we increase the energy required to push the electrons up the valence band. This is the same reason for which the device slows down. Consequently, when we increase the threshold voltage, the charge creation and collection characteristics change.

4.2.2 Logic attenuation due to high threshold voltage device . The transient pulses attenuate, when they propagate through pass-transistors and transmission gates, due to V_t drop across the devices. However, static CMOS sees different trends. In static CMOS, the gain of the circuit is positive. The gain of an inverter is given by Equation 5

$$GainG = \frac{1+r}{(V_m - V_t - V_{dsat}/2)(\lambda_n - \lambda_p)} \tag{5}$$

where, r is a ratio which compares the relative driving strength of NMOS transistor in comparision with PMOS transistor, V_M is the switching threshold (usually V_m is half of the supply voltage), V_{dsat} is drain saturation current, and λ_n, λ_p are channel length modulation factors for an n-channel and p-channel respectively. We can see that due to higher gain, when V_t is increased, a transient pulse will propagate in a system for a longer time and travels more logic stages.

4.2.3 Effect of V_t on SER of SRAM and Flip-flops. Table 1 presents the $Q_{critical}$ of the SRAM and Asymmetric SRAM cell. From Table 1, we observe that the threshold change does not affect $Q_{critical}$ of the standard 6T SRAM significantly. By increasing V_t by 0.2V, we do not notice any significant change in $Q_{critical}$. Because the threshold voltage of both PMOS and NMOS in the back-to-back inverter configuration was changed, the regenerative property of the circuit ensures that there is no loss of charge and hence relatively no gains in terms of $Q_{critical}$. However, when we analyze an ASRAM [4] optimized for leakage while storing a preferred logic state, we observe a different trend.

	ΔV_t	$Q_{critical}$ /C	*Leakage* /W
ASRAM	0	4.75e-14	2.20e-07
	0.1	6.58e-14	9.10e-09
	0.2	7.58e-14	3.42e-10
SRAM	0	4.75e-14	2.40e-07
	0.1	4.04e-14	9.66e-09
	0.2	3.82e-14	9.46e-10

Table 1. $Q_{critical}$ and leakage power of SRAM and ASRAM with different V_t. Nominal V_t was 0.22V

	ΔV_t	$Q_{critical}$ at input /C	$Q_{critical}$ at most susceptible node /C
SDFF	0	6.06e-21	1.24e-20
	0.1	5.08e-21	1.33e-20
	0.2	-	-
C^2MOS	0	3.69e-20	7.12e-21
	0.1	5.64e-20	7.12e-21
	0.2	1.68e-19	-
TGFF	0	1.99e-20	7.36e-21
	0.1	1.77e-19	7.36e-21
	0.2	3.87e-17	7.36e-21

Table 2. $Q_{critical}$ of different flip-flops. Nominal V_t was 0.22V

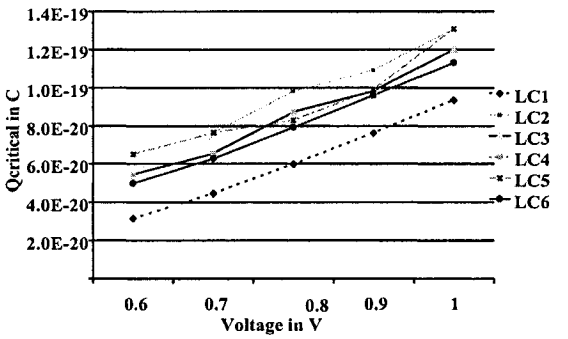

Figure 4. $Q_{critical}$ vs the supply voltage for different level converters

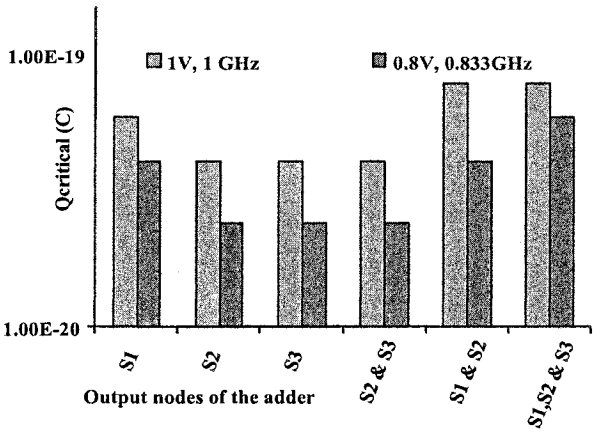

Figure 5. Effect of frequency and voltage scaling on 4-bit Kogge Stone adder

Figure 7 shows a circuit schematic of ASRAM optimized for reducing leakage when storing a 0. In ASRAM, the threshold voltage of transistors in the leaky path of circuit is increased to reduce leakage. For a stored value of 0, the transistors in the leaky path are shown. The V_t of these transistors are increased to reduce the leakage. The $Q_{critical}$ of this SRAM in its preferred state (i.e, when storing a 0) increases significantly, however for the non preferred state it remains the same. Specifically, when V_t is increased by 0.2V, $Q_{critical}$ increases by 59%. This is due to the fact that if we try to charge the node to

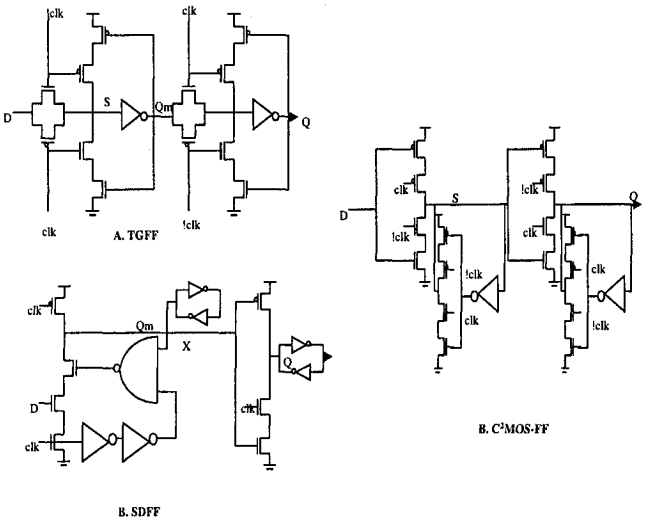

Figure 6. Flip-Flops evaluated for SER

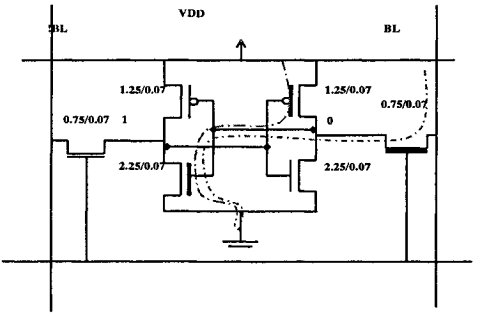

Figure 7. Asymmetric SRAM: Optimized for 0

1, the PMOS due to its high V_t will not be able to provide necessary feedback to quickly change the bit. However, if a value of 1 is stored, and we attempt to discharge it, then $Q_{critical}$ does not change as the NMOS is still at normal V_t. A similar behavior is also observed for an ASRAM designed for storing a preferred state of 1.

We characterize three different flip-flops, transmission gate flip flop(TGFF), C^2MOS flip-flop(C^2MOS), and semi-dynamic flip-flop (SDFF). In each case we estimate the effect of increasing threshold voltages on $Q_{critical}$. Figure 6 shows detailed schematics of these designs. The blank fields in the table represents the points where the flip-flop became unstable and could not latch the input data. There are two different aspects that should be investigated with respect to the effects of threshold voltages and susceptibility of soft errors on flip-flops. First, the soft error rate of the flip-flop itself could change. This is found by evaluating $Q_{critical}$ at the most susceptible node [22]. Second the ability of the flip-flop to latch onto an error at its input could change. This effect will be useful in analyzing its behavior in a datapath. Hence Table 2, lists the $Q_{critical}$ at both the nodes for all the flip-flops.

From Table 2, we can note that, for a TGFF, $Q_{critical}$ at the input node, when V_t is increased, while the $Q_{critical}$ at the node S is same. We ascribe this trend to the presence of to the transmission gate present at the input. On the other hand for the node S, the higher gain of the inverter cancels out the effect of the transmission gate at the slave stage and hence the $Q_{critical}$ remains almost constant. Similar testing was done on a C^2MOS flip-flop which also has master-slave stages similar to that of the transmission gate flip-flop. Since C^2MOS flip-flop does not have any transmission gate based structures it has a lower $Q_{critical}$ compared to the TGFF. We also investigate one of the pulse triggered designs SDFF for it's $Q_{critical}$. SDFF has few large sized devices in its feedback path thus resulting in a much higher $Q_{critical}$ at the most susceptible node (X) as compared to the other flip-flops considered. Since this node feeds back into a NAND gate, when the threshold increases, due to the increase in delay of the NAND gate and 2 inverters, $Q_{critical}$ increases. Thus the flip-flop by itself has a higher $Q_{critical}$ as threshold voltage increases. At the input the larger overlap time helps pull down the voltage at node X and hence reduces the $Q_{critical}$.

4.2.4 Effect of V_t on Combinational Logic . We analyze three kinds of logic circuits: chain of 6-inverters, chain of 4-nand gates and transmission gate based full adders. For all of these circuits we check for an error by latching the transient pulse at the end of the logic chain. A transmission gate flip-flop (TGFF) was used to latch the values. TGFF was chosen as it is one of

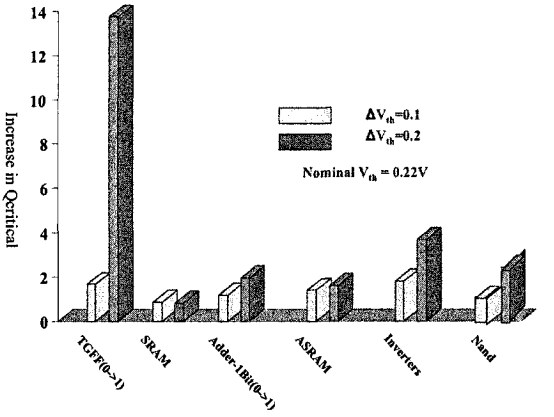

Figure 8. Increase in $Q_{critical}$ of different designs with respect to operating nominal V_t of o.22V

the most commonly used flip-flop. From Table 3, we note that the $Q_{critical}$ of the circuit is increasing for increasing threshold voltages. For TG based adders, the threshold drop across transmission gates accounts for the increase in $Q_{critical}$ as the V_t increases. However, for static logic this is counter intuitive. Based on the pulse propagation characteristics, the $Q_{critical}$ of the circuits should be lower. This can be accounted for the robustness of flip-flops. In Figure 8, we find that the $Q_{critical}$ increase for the flip-flop is many orders of magnitude higher than the others. To confirm our observations we simu-

	ΔV_t	$Q_{critical}$ /C	*Leakage* /W
Nand	0	1.31e-20	22.56e-07
	0.1	2.26e-20	9.92e-09
	0.2	2.83e-20	4.90e-10
Inverters	0	1.28e-20	2.20e-07
	0.1	2.3e-20	4.90e-10
	0.2	4.73e-20	41.99e-11
TG Adder	0	4.60e-20	1.18e-07
	0.1	1.35e-19	3.42e-08
	0.2	5.87e-17	3.40e-08

Table 3. $Q_{critical}$ and leakage power of various designs with different V_t. A high V_t TGFF was used at the output of the logic chain

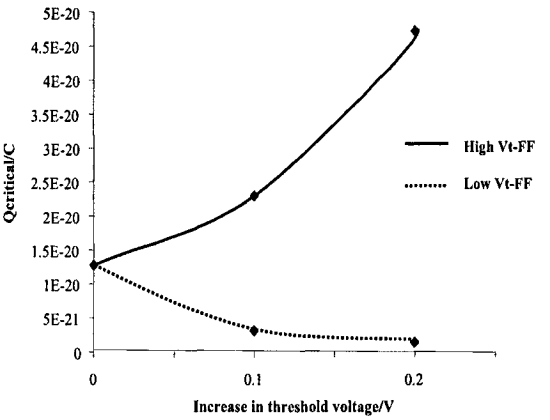

Figure 9. $Q_{critical}$ of typical inverter chain with either high V_t or low V_t flip-flop at the output of the chain. Nominal V_t was 0.22V

lated the 6-inverter chain again, but this time we used normal-V_t flip-flops at the output of the logic chain and we found that as the V_t increased, the $Q_{critical}$ values decreased. The results are presented in Figure 9. In the next section we show how this fact can be leveraged to reduce power and increase robustness of the circuit.

4.3 Effect of delay balance using high V_t devices on soft errors

Figure 10 shows a typical pipeline. The logic between pipeline stages is distributed across slow and fast paths, with the slowest path determining the clock frequency. Thus, slow paths become critical paths and fast paths become non-critical paths. It is an accepted practice to use high V_t devices on non-critical paths. Since these are not delay sensitive, we achieve high leakage power savings with minimal performance penalty. This is some times referred to as *delay balancing*. To examine the effect of delay balancing on $Q_{critical}$, we simulate two circuits, one with a 6-inverter chain which forms the critical path and the other with a 3-inverter chain. Figure 11, shows the $Q_{critical}$ of the 6-inverter chain as compared to the $Q_{critical}$ of the 3-inverter chain with both low and high V_t TGFFs. If we perform delay balancing on this logic with low V_t TGFF, and high V_t 3-inverter chain, we can observe the $Q_{critical}$ of 3-inverter

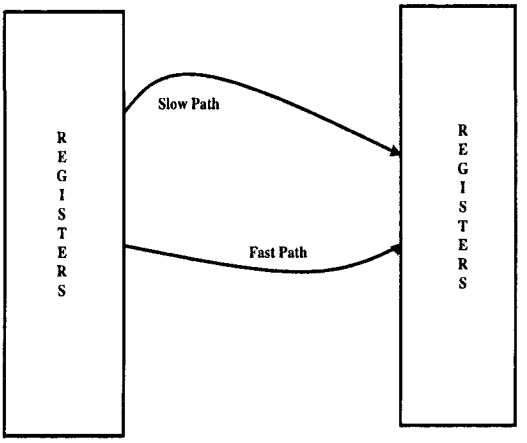

Figure 10. Delay Balancing

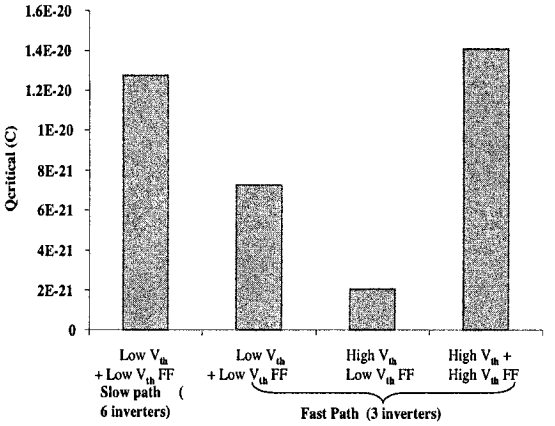

Figure 11. Effect of delay balancing

chain reduces. Thus, we see that this path now becomes more vulnerable to soft errors. Consequently, if a high-V_t flip-flop is used for latching, the $Q_{critical}$ of

the 3-inverter chain (relative to the 6-inverter chain) is still high. So, while performing delay balancing it is recommended to use high V_t flip-flops at the end of the logic chain to improve the immunity to SER.

5. Conclusion

In this work, we examine the effect of the high threshold voltages and voltage scaling on SER. We find that for certain designs like transmission gate based designs SER reduces while for static logic SER deteriorates as V_t is increased. Also we show that, as in ASRAM, using high V_t cleverly can reduce both SER and leakage power. Finally we find that the use of high V_t for delay balancing can potentially increase SER, but the reliability can be bought back by the use of high V_t flip-flops. In general, we showed that use of high V_t devices not only reduces leakage but also affects the reliability of circuit. In contrast, voltage scaling almost always increases the susceptibility to SER.

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