Research Article

Selective harmonic elimination (SHE) based 3-phase multilevel voltage source inverter (VSI) for standalone applications

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Abstract
The breakthroughs in power electronics semiconductor technology have led to the raised in popularity of Multi-level Voltage Source Inverters, which is the reason industries and researchers are relentlessly working towards extending it to both medium and high-power applications. Consequently, this paper presents a modified Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) controlled three-phase 5-level Multi-level Inverter (MLI) topology. The work is an extension of a single-phase topology proposed by the authors. The uniqueness of the proposed topology is that it comprises of six Cascaded H-bridge modules (two modules per phase) that are powered through a single direct current (DC) source, hence eliminating the need for multiple DC sources. In addition, conventional 5-level MLI has two switching angles (n = 2), which restricts its harmonic elimination capability to one (n = 1) lower order harmonics. This study removes that restriction by utilising the concept of multiple switching per step, resulting in the superimposing of 12 notches (n = 12) on the output voltage at the 3/9 distribution ratio. With the fundamental switching SHE-PWM, twelve non-linear, transcendental equations are generated, and they are optimally solved using the Hybrid Coded Genetic Algorithm to eliminate 11 (n – 1) lower-order harmonics. The low-switching frequency results in less electromagnetic interference as well as reduced switching loss, which improves the overall inverter efficiency. The topology has less output Total Harmonics Distortion, fewer components, and lower weight and cost than conventional topologies. The circuit was designed and validated through simulations performed in PSIM software.

Keywords Total harmonic distortion (THD) · Selective harmonic elimination (SHE) · Reduced device count · Multi-level inverter

1 Introduction

The advent of enhanced power electronic devices coupled with the demand for clean, sustainable and friendly energy sources, has resulted in a rapid research surge in renewable energy conversion technology. The ability of a Multilevel inverter (MLI) to concatenate smaller voltages to attain the required high voltage value has been the reason for its recent prominence and dominance in the field of energy conversion [1–3]. In the ordinary conventional two-level inverter, the output total harmonic distortion (THD) is reduced by increasing the inverter switching frequency, which is at the detriment of the switching losses. Unlike the two-level, the MLI medium voltage step reduces voltage stress on the power switches. Its low switching frequency makes it generate less electromagnetic interference (EMI), and its modular nature simplifies its control strategy and provides easy maintenance and the possibility of incorporating redundancy along with fault tolerance operation [3, 4].

The commonly known MLI topologies are broadly classified into Diode Clamped (DiC) [5], Flying Capacitor (FC)

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[6] and Cascaded H-bridge (CHB) with multiple DC sources [7]. They are popularly referred to as conventional converters because they form the basic building block of almost all the modified and hybrid topologies. MLI converters utilise low power switches to generate any required output voltage level, making them suitable for medium and high power applications. Each topology has its own merits and demerits. For instance, DiC has an unequal voltage sharing problem across the switches and its number of clamping diodes increases with output levels [8], while the FC output level increases with an increase in the number of capacitors. This results in a need for an additional feedback control mechanism that monitors and regulates the capacitor voltage level, which further complicates and increases the bulkiness of the system. Its high frequency of operation results in higher switching losses which deteriorate the inverter efficiency [5]. In the case of CHB topology, similar to the FC, the output level increases with more H-bridge modules and independent DC sources [7].

Quite a number of researchers have developed various MLI topologies to address the issue of the increased number of H-bridge modules and multiple DC sources in CHB converters. However, unfortunately, most of them ended up making the circuit bulky and complicating the control strategy, which results in reduced efficiency and increased output THD in the system [9–11].

A new converter topology was proposed by Kang et al. [12] to realise higher voltage step with a reduced number of power electronic switches [12]. The author uses three H-bridge modules along with a specially designed transformer having three primary windings and cascaded secondary with multiple turns ratio of 1:1, 1:1 and 1:3, respectively. Two of the h-bridge modules were controlled at fundamental frequency to synthesize the output component, while the third module is run at a slightly higher frequency to generate a series of notches that compensate for the voltage level step transition, therefore minimizing the harmonic output content [7]. The topology was able to increase the voltage output steps and reduced the THD level. The drawbacks are the transformer size that is attributed to the low frequency and turns ratio as well as the poor THD quality it exhibits at light load since output harmonics were only suppressed not wholly eliminated. In a similar work published in [13], the same circuit configuration was used but with a different transformer turns ratio and PWM control function. The frequency of operation was increased, which results in a reduction of the physical transformer size and turns ratio by the scale of half (1:0.5). The drawback is that the switching frequency increases which affects the power electronic switch lifespan and results in high switching losses. Rao et al. [14] proposed a new topology that incorporates additional DC sources and switches to achieve higher voltage steps (m) [14]. For an "m" number of steps, the topology requires m + 3 power electronic switches per phase, which is a 50% switch reduction in the conventional CHB and FC topologies. The drawback of the topology is the need for additional DC sources, sophisticated control circuity, high switching and uneven voltage distribution across the power switches. Gobinath et al. [15] developed a three-phase reduced switch MLI topology that is capable of generating seven levels using seven power switches and three DC sources per phase. Another positive feature of this topology is its ability to operate in three modes, namely powering, freewheeling and regenerative modes. Its drawbacks are similar to that of the previous, i.e. increased DC sources, complex control circuitry and uneven voltage distribution across the power electronic switches [15].

In an effort to proffer the solution to a similar problem, this study develops a five-level three-phase reduced switch MLI topology, which is controlled by using multiple notches (3/9) per step and SHE-PWM. A conventional five-level MLI has two voltage steps per quarter, which is equivalent to two (n = 2) switching angles per quarter. Based on the SHE-PWM theorem, for 'n' switching per quarter, 'n − 1' harmonics will be eliminated. Hence, for 'n = 2' only one lower order harmonics is eliminated. Therefore, introducing multiple switching per quarter increases the MLI ability to eliminate lower order harmonics, which eliminates the need to increase the output step. In view of this, the hybrid coded genetic algorithm optimization technique reported in [16] is used to solve the switching angles that eliminate the 11 (n − 1) lower order harmonics optimally. This idea is implemented in the single-phase topology published in [1]. The topology contains two H-bridges connected in parallel with a single DC source. Each of the module terminals is connected to the primary side of a cascaded secondary side transformer having a 1:1 turns ratio. The SHE-PWM fundamental switching reduces the output THD while at the same time, it maintains a better efficiency due to switching loss reduction. This study extends the same topology to three-phase applications. It comprises six H-bridges that are all powered through a single DC source, with transformers connected at each module terminal to prevent short-circuits within the power switches as well as load isolation. In a three-phase system, even and triplen harmonics cancel each other out in the output; therefore, only the 11 odd non-triplen harmonics are targeted for elimination. The switching angles are the same as those used in the single-phase [1] with subsequent phases shifted by 120° and 240°, respectively.

2 Converter topology

This section explains the inverter topology modes of operation, how the switching angles were obtained, and the switching function used to realise the 5-level voltage waveform.

2.1 The proposed 3-phase converter topology and its circuit operations

The number of voltage steps in an MLI circuit determines the number of harmonics it is capable of eliminating. In a conventional Cascaded H-bridge topology, its major drawback is that to increase its output step, an additional H-bridge module with independent DC source is required. This result in increased in circuit complexity and size, which also affects the overall system efficiency, weight and cost. The proposed 3-phase multilevel inverter, shown in Fig. 1 below tries to address this drawback by using a single DC source along with the concept of multiple switching per quarter to selectively eliminate the output lower harmonics. The topology comprises of a total of six cascaded H-bridge modules (two per phase), each of the module has four power electronic switches, making a total of 8 power electronic switches per phase. All the three phases are connected in parallel across a single DC input source. Each of the module output terminals is connected to the primaries of a cascaded transformer having two independent primaries and series-connected secondary and 1:1 turns ratio. The transformer prevents the DC source from being short-circuited as well provides an effective load isolation. The switches are denoted by S_{xyt}, where 'x' represents the module number within a phase, which could be either 1 or 2. Whereas 'y' stand for the switch number within a module and is between 1 and 4. The subscript 't' denotes the switch phase and are represented by alphabet a, b and c. With appropriate switching function, the inverter generates stable five and nine voltage steps in the phase and line respectively. The concepts of multiple notches per steps enable the topology to eliminate ten extra harmonics than the usual conventional one. Moreover, it has cut down the number of DC sources from six to one, which has a significant impact on the inverter size, weight, cost and complexity.

In order to synthesize the five level voltage waveform at the output terminals, the gating signal of each IGBT needs to be generated based on the calculated switching angles. The phase A IGBT switches conduction states for the positive and negative half-cycles are given in Table 1. There are five different voltage ($0 \pm E \pm 2E$) steps, with 0 V and $\pm EV$ having alternative switching combination. It is worth noting that switches on the same leg (S11a and S12a) nare operated complementarily to avoid shortening the dc source.

2.2 Mathematical modelling of the proposed 3-phase topology

To model an inverter output voltage using SHE-PWM modulation technique, the expected phase voltage waveform showing the output steps and the switching angle distribution ratio needs to be properly sketched [17, 18]. Therefore, Fig. 2 depicts the rough sketch of the targeted

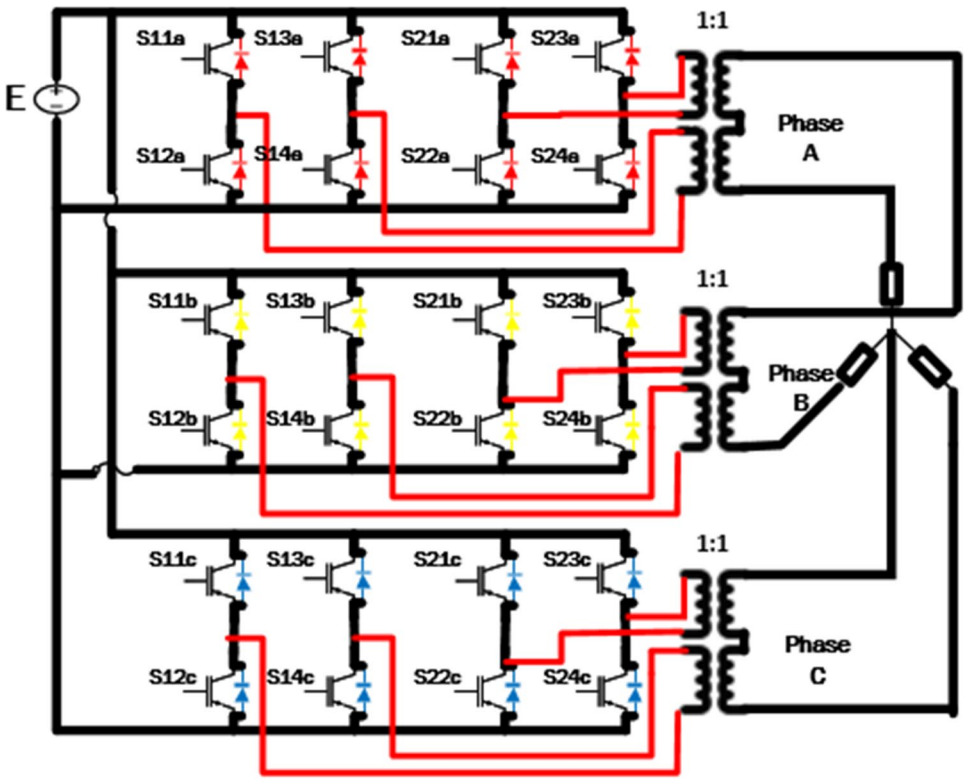

Fig. 1 Proposed inverter topology configuration

Table 1 Switching combinations

Voltage	Switching states							
	S_{11a}	S_{12a}	S_{13a}	S_{14a}	S_{21a}	S_{22a}	S_{23a}	S_{24a}
0	1	0	1	0	1	0	1	0
+E	1	0	0	1	1	0	1	0
+E	1	0	1	0	1	0	0	1
0	0	1	0	1	0	1	0	1
−E	0	1	1	0	1	0	1	0
−E	1	0	1	0	0	1	1	0
+2E	1	0	0	1	1	0	0	1
−2E	0	1	1	0	0	1	1	0

terminal voltage waveform with the twelve switching angles (*α*1 *to α*12) per quarter cycle. It is assumed that it obeys both half and quarter-wave symmetry theorem. The top waveform represents the inverter phase voltage, which is the summation of the phase H-bridge modules terminal voltages *V*1 and *V*2. Based on the terminal voltage *V*1, it appears the majority of the notches are generated by module 1, signifying that module 1 power switches are subjected to more switching stress than that of module 2. Module 2 produces terminal voltage *V*2, which is used for power transfer to the load side. Hence, making it switches to experience high conduction losses. However, this research is not aimed at ensuring equal power distribution and losses within the inverter modules and its power switches.

The uniqueness of this MLI is the switching strategy employed, were series of notches are superimposed on the conventional waveform at pre-determined angles to extends its harmonic eliminating ability. The proposed waveform has twelve ($n = 12$) switching angles per quarter wave with 3/9 distribution ratio. Therefore, based on SHE-PWM theorem, eleven ($n - 1$) lower-order dominant harmonics will be eliminated. Equation (1) is the Fourier Series expansion used to model the output waveform mathematically, leading to the generation of twelve non-linear transcendental equations. The equations comprise of a fundamental component and eleven lower-order harmonics. Since we are dealing a three-phase system, it means only the first eleven odd non-triplen harmonics are of concerned to us, i.e. (5th, 7th, 11th, 13th, 17th, 19th, 23rd, 25th, 29th, 31st, 35th) [1, 19, 20].

$$f(x) = a_0 + \sum_{n=1}^{\infty} \left(a_m \cos \frac{m\pi x}{l} + b_m \sin \frac{m\pi x}{l} \right) \tag{1}$$

The inverter output is an odd function, as such, it only has the sinusoidal component (b_m) of the expansion series. Both the DC (a_0) and Cosine (a_m) components are zeros. i.e. $a_0 = 0$ and $a_m = 0$ for all integer values of m. The expression is reduced to Eqs. (2) and (3).

$$V_{out}(x) = \sum_{m=1}^{\infty} b_m \sin(mx) \tag{2}$$

$$b_m = \frac{1}{l} \int_{-l}^{l} f(x) * \sin\left(\frac{m\pi x}{l}\right) dx \tag{3}$$

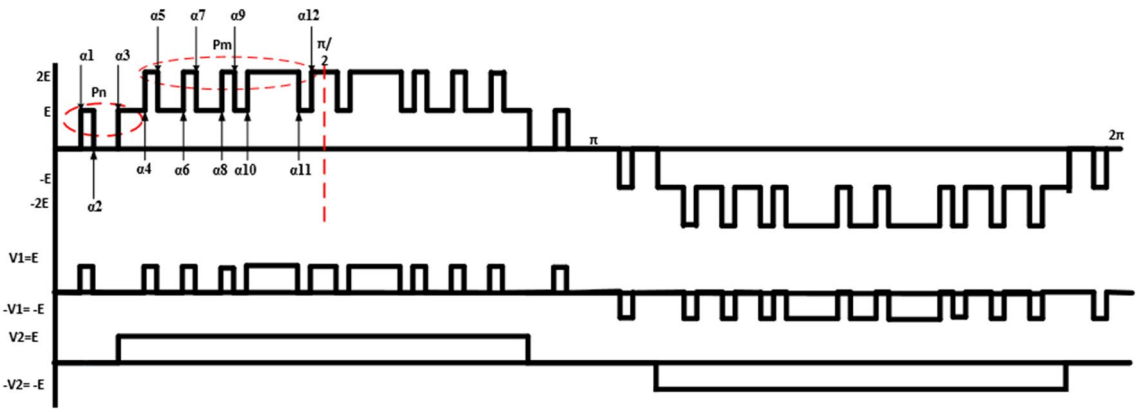

Fig. 2 Per-phase waveform with 3/9 distribution ratio

Due to both half and quarter-wave symmetry of the output waveform, 1/4th representing 0–90 range of the waveform is enough to model the entire waveform.

With the assumptions that period "P" = 2l = 2π, l = π. The general expression for the co-efficient of the sinusoidal output component obtained using Eq. (3) is given by Eq. (4):

$$b_m = \frac{1}{\pi}\int_{\alpha_1}^{\alpha_2} \mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_3}^{\alpha_4} \mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_4}^{\alpha_5} 2\mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_5}^{\alpha_6} \mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_6}^{\alpha_7} 2\mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_7}^{\alpha_8} \mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_8}^{\alpha_9} 2\mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_9}^{\alpha_{10}} \mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_{10}}^{\alpha_{11}} 2\mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_{11}}^{\alpha_{12}} \mathrm{E}^* \sin(mx)\delta x + \int_{\alpha_{12}}^{\pi/2} 2\mathrm{E}^* \sin(mx)\delta x \tag{4}$$

The above expression needs to be solved. For the sake of simplicity, 'm' being the harmonic order is considered to be one (m = 1), which means the fundamental component expression given by:

$$b_1 = \frac{\mathrm{E}}{\pi}\begin{bmatrix} -\cos x\downarrow_{\alpha_1}^{\alpha_2} - \cos x\downarrow_{\alpha_3}^{\alpha_4} - 2\cos x\downarrow_{\alpha_4}^{\alpha_5} - \cos x\downarrow_{\alpha_5}^{\alpha_6} - 2\cos x\downarrow_{\alpha_6}^{\alpha_7} - \cos x\downarrow_{\alpha_7}^{\alpha_8} \\ -2\cos x\downarrow_{\alpha_8}^{\alpha_9} - \cos x\downarrow_{\alpha_9}^{\alpha_{10}} - 2\cos x\downarrow_{\alpha_{10}}^{\alpha_{11}} - \cos x\downarrow_{\alpha_{11}}^{\alpha_{12}} - 2\cos x\downarrow_{\alpha_{12}}^{\pi/2} \end{bmatrix}$$

$$= \frac{\mathrm{E}}{\pi}\begin{bmatrix} -\cos\alpha_2 + \cos\alpha_1 - \cos\alpha_4 + \cos\alpha_3 - 2\cos\alpha_5 + 2\cos\alpha_4 - \cos\alpha_6 \\ +\cos\alpha_5 - 2\cos\alpha_7 + 2\cos\alpha_6 - \cos\alpha_8 + \cos\alpha_7 - 2\cos\alpha_9 + 2\cos\alpha_8 \\ -\cos\alpha_{10} + \cos\alpha_9 - 2\cos\alpha_{11} + 2\cos\alpha_{10} - \cos\alpha_{12} + \cos\alpha_{11} + 2\cos\alpha_{12} \end{bmatrix}$$

$$= \frac{\mathrm{E}}{\pi}\begin{bmatrix} \cos\alpha_1 - \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4 - \cos\alpha_5 + \cos\alpha_6 - \cos\alpha_7 + \cos\alpha_8 \\ -\cos\alpha_9 + \cos\alpha_{10} - \cos\alpha_{11} + \cos\alpha_{12} \end{bmatrix} \tag{5}$$

After the integration, the generalized expressions for both the fundamental and harmonic coefficient can be written as:

$$b_m = \frac{\mathrm{E}}{m\pi}\begin{bmatrix} \cos m\alpha_1 - \cos m\alpha_2 + \cos m\alpha_3 + \cos m\alpha_4 - \cos m\alpha_5 + \cos m\alpha_6 - \cos m\alpha_7 + \cos m\alpha_8 \\ -\cos m\alpha_9 + \cos m\alpha_{10} - \cos m\alpha_{11} + \cos m\alpha_{12} \end{bmatrix} \tag{6}$$

The entire modelled output voltage waveform across the period is given by:

$$V_{out}(wt) = \sum_{m=1}^{\infty} \frac{4\mathrm{E}}{m\pi}\begin{bmatrix} \cos m\alpha_1 - \cos m\alpha_2 + \cos m\alpha_3 + \cos m\alpha_4 - \cos m\alpha_5 + \cos m\alpha_6 \\ -\cos m\alpha_7 + \cos m\alpha_8 - \cos m\alpha_9 + \cos m\alpha_{10} - \cos m\alpha_{11} + \cos m\alpha_{12} \end{bmatrix} \sin(m\alpha_n) \tag{7}$$

$$b_n = \frac{4E}{m\pi}\sum_{m=1,5,7,\ldots}^{3m-1}\left[\sum_{K=1}^{Pn}(-1)^{K+1}\cos(m\alpha_K) + \sum_{Pn+1}^{Pm}(-1)^{K}\cos(m\alpha_K)\right] \tag{8}$$

From Fig. 2, *Pn* and *Pm* represent the number of the switching angles per distribution ratio and ranges from 1–3 to 4–12, respectively, and K is an integer representing the switching angle number. Thus, substituting them reduces the expression to:

$$b_n = \frac{4E}{m\pi}\sum_{n=1,5,7,\ldots}^{3m-1}\left[\sum_{K=1}^{3}(-1)^{K+1}\cos(m\alpha_K) + \sum_{K=4}^{12}(-1)^{K}\cos(m\alpha_K)\right] \tag{9}$$

With the above expression, the twelve non-linear transcendental equations comprising of the fundamental component and the eleven targeted lower harmonics are given by Eqs. (10)–(13). Equation (10) represents the fundamental amplitude, while the remaining are for the harmonics. As mentioned earlier, only the odd non-triplens harmonics are to consider for elimination. The harmonic coefficient order to be eliminated is found using the expression 3K − 1 and 3K − 2 for even and odd values of K respectively. To find the angles that satisfy the harmonic conditions, all the expressions except for Eq. (10) are equated to zero.

$$b_1 = \frac{4E}{\pi}\left[\begin{array}{c}\cos n\alpha_1 - \cos n\alpha_2 + \cos n\alpha_3 + \cos n\alpha_4 - \cos n\alpha_5 + \cos n\alpha_6 - \cos n\alpha_7 + \cos n\alpha_8 \\ -\cos n\alpha_9 + \cos n\alpha_{10} - \cos n\alpha_{11} + \cos n\alpha_{12}\end{array}\right] \tag{10}$$

$$b_5 = \left[\begin{array}{c}\cos 5\alpha_1 - \cos 5\alpha_2 + \cos 5\alpha_3 + \cos 5\alpha_4 - \cos 5\alpha_5 + \cos 5\alpha_6 - \cos 5\alpha_7 + \cos 5\alpha_8 \\ -\cos 5\alpha_9 + \cos 5\alpha_{10} - \cos 5\alpha_{11} + \cos 5\alpha_{12}\end{array}\right] = 0 \tag{11}$$

$$b_7 = \left[\begin{array}{c}\cos 7\alpha_1 - \cos 7\alpha_2 + \cos 7\alpha_3 + \cos 7\alpha_4 - \cos 7\alpha_5 + \cos 7\alpha_6 - \cos 7\alpha_7 + \cos 7\alpha_8 \\ -\cos 7\alpha_9 + \cos 7\alpha_{10} - \cos 7\alpha_{11} + \cos 7\alpha_{12}\end{array}\right] = 0 \tag{12}$$

$$\vdots$$

$$b_{35} = \left[\begin{array}{c}\cos 35\alpha_1 - \cos 35\alpha_2 + \cos 35\alpha_3 + \cos 35\alpha_4 - \cos 35\alpha_5 + \cos 35\alpha_6 - \cos 35\alpha_7 \\ +\cos 35\alpha_8 - \cos 35\alpha_9 + \cos 35\alpha_{10} - \cos 35\alpha_{11} + \cos 35\alpha_{12}\end{array}\right] = 0 \tag{13}$$

The fundamental equation can be re-arranged to obtain the following expression: $Ao = \frac{\pi m_i}{4}$, and $m_i = \frac{Vf}{E}$, where m_i is the modulation index, Vf and E are the fundamental and DC value components, respectively.

$$f(\alpha_1, \alpha_2, \alpha_3 \ldots \alpha_{12}) = \left[\begin{array}{c}(b_1 - A_0)^2 + b_5^2 + b_7^2 + b_{11}^2 + b_{13}^2 + b_{17}^2 + b_{19}^2 + b_{23}^2 \\ b_{25}^2 + b_{29}^2 + b_{31}^2 + b_{35}^2\end{array}\right] \tag{14}$$

Equation (14) above represents the objective function to be minimized using the HCGA algorithm under the following constraint $\alpha_1 < \alpha_2 < \cdots < \alpha_k < \frac{\pi}{2}$. The solutions obtaineprovis the optimized switching angle combinations, that produce minimum harmonic content while maintaining the fundamental component value. Figure 3 below depicts both the explorationnd exploitation stages of the HCGA optimization process.

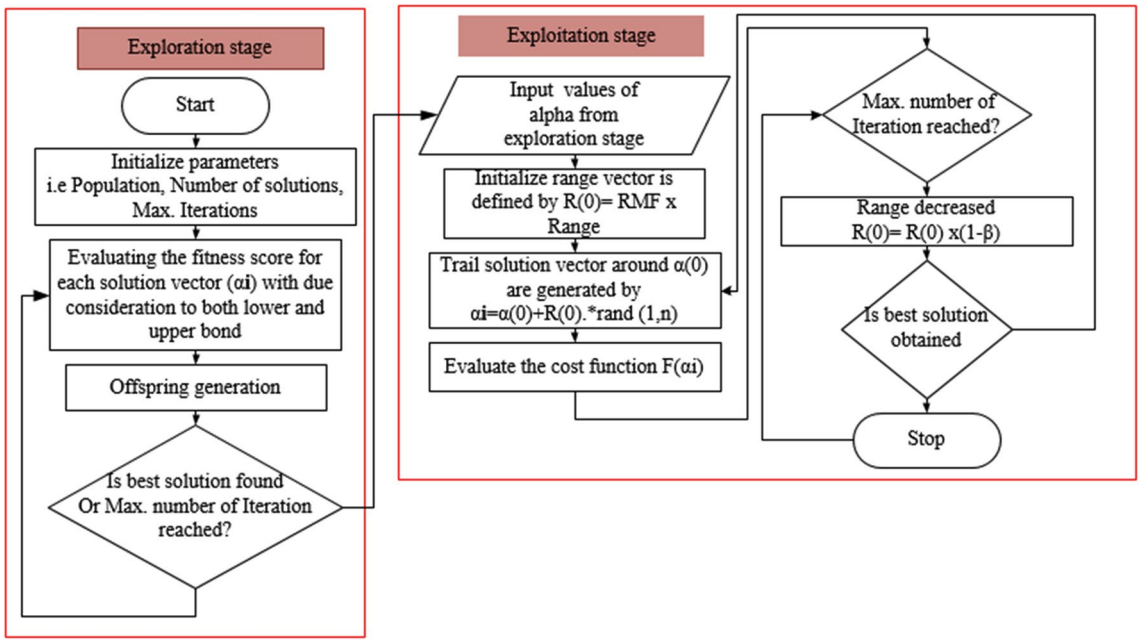

Fig. 3 HCGA Algorithm Flow Chart

3 Results and discussion

This section presents the optimized switching angle solutions, the simulated output voltage waveforms along with it Fast Fourier Transforms FFT, conventional topologies component device comparison, the THD and efficiency comparison of the proposed and conventional CHB topology.

3.1 Switching angle solutions

Table 2 below provides the solution of the non-linear transcendental equations at M = 1.8. Twelve switching angles for Phase A were obtained, which are then used to compute the remaining switching points using the quarter and half-wave symmetry principles. Phase B and C switching angles were found by delaying Phase A by 120 and 240° respectively. The simulation is carried out in PSIM software with the switching angles fed into the twelve Pulse generating blocks to drive the IGBT's. The same legged switches are operated in a complementary manner, so a NOT gate was placed to invert the pulses. The same method was also applied to the remaining two phases.

Table 2 Optimized switching angles

s/n α_n	Phase A	Phase B	Phase C
1	13.40246	133.40246	253.40246
2	15.67567	135.67567	255.67567
3	19.61681	139.61681	259.61681
4	35.50001	155.50001	275.50001
5	37.80673	157.80673	277.80673
6	46.26136	166.26136	286.26136
7	48.24797	168.24797	288.24797
8	54.85481	174.85481	294.85481
9	58.37752	178.37752	298.37752
10	61.01313	181.01313	301.01313
11	83.87128	203.87128	323.87128
12	86.01930	206.0193	326.0193

3.2 Simulation results

The input DC voltage was set to 100 V, all the transformers to 1:1 turn ratio, the 3-phase resistive load was set 100Ω and a simulation control sampling rate of 1 μ seconds. Figure 4 shows the two H-bridge terminal voltages *V*1 and *V*2 for Phase A, while Fig. 5 depicts their corresponding gating signals with switch *S*11*a* to *S*14*a* controlling module 1 and *S*21*a* to *S*24*a* for module 2. Both terminal voltages and switching signals correspond with the sketch made during the design procedure. The two voltages *V*1 and *V*2 add up to produce the required five level waveforms with 3/9 switching distribution ratio. Moreover, the gating signals satisfies the inverter switching combination provided in Table 1. In the same manner, the other terminal voltages and gating signals for Phase B and Phase C were generated with 120 and 240° out of phase with Phase A.

Figure 6 depicts Phase A (Vab) nine-level line voltage waveform along with the corresponding five-level (Va) and (Vb) phase voltages. As expected Vb is 120° out of phase with Va. Figure 7 shows all the 3-phase unfiltered nine-level voltage waveforms (Vab, Vbc and Vca). The inverter is lightly loaded in order to have a defined shape of the waveforms and the harmonic properties.

Figure 8 shows the Fast Fourier transform (FFT) of all the three-phase voltage waveforms over the range of 5 kHz. It appeared SHE-PWM has successfully eliminated all the 11 lower-order odd non-triplen harmonics within the

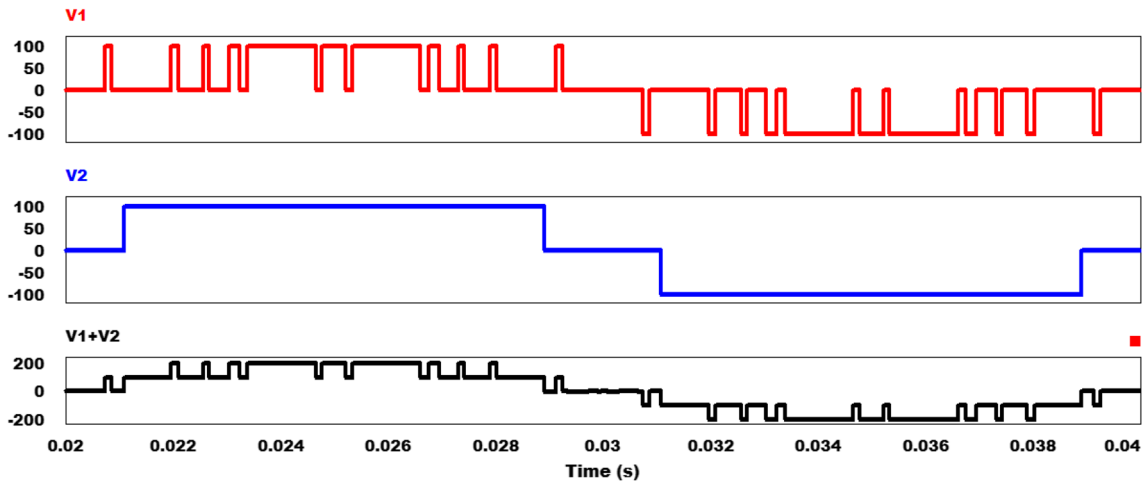

Fig. 4 Phase A terminal voltages

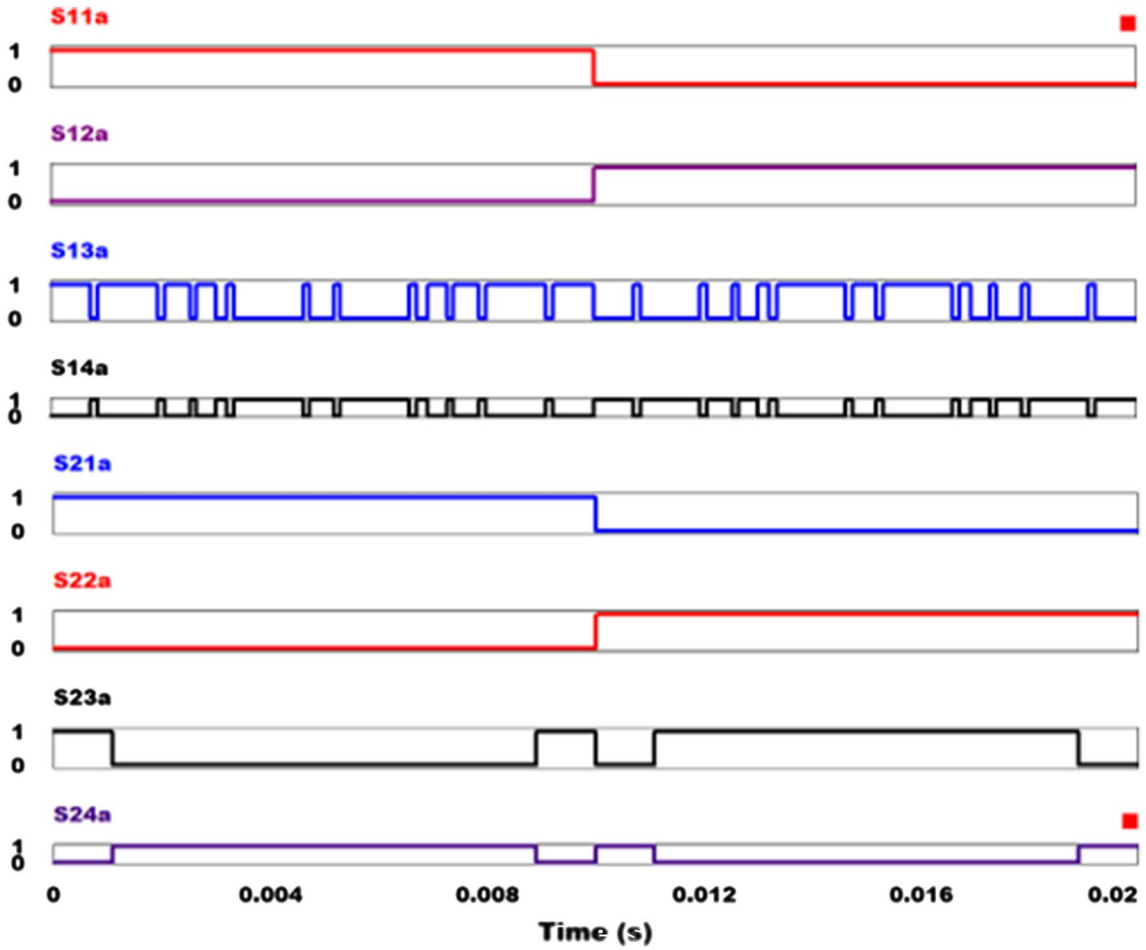

Fig. 5 Phase A gating signal

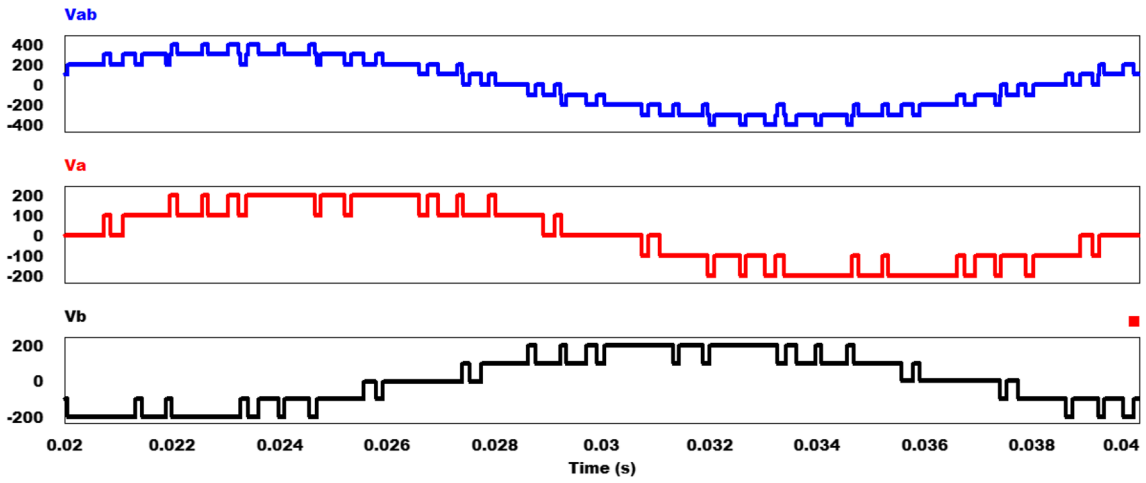

Fig. 6 Per-phase waveforms

elimination band of 1.75 kHz which is the 35th order. The visible harmonics are within the 1.75 kHz are the triplens (3rd, 9th, 15th, 21st, 27th, 33rd) which are expected to be eliminated in the Line to Line voltages (Vab, Vbc and Vca). The spectrum becomes full with harmonics outside the elimination band, i.e. from 1.85 kHz (37th order) onward.

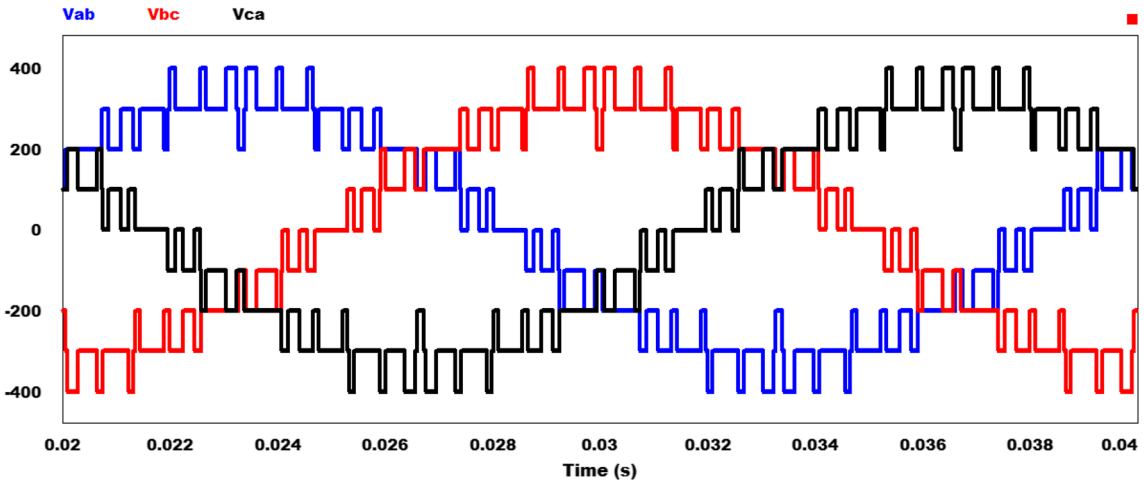

Fig. 7 Three-phase waveforms

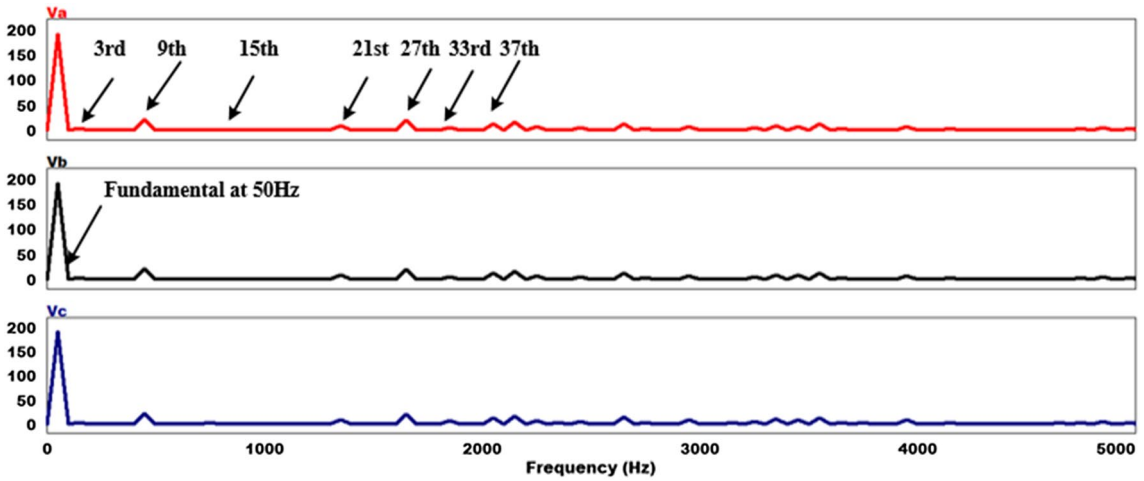

Fig. 8 FFT Spectrum of the phase waveform

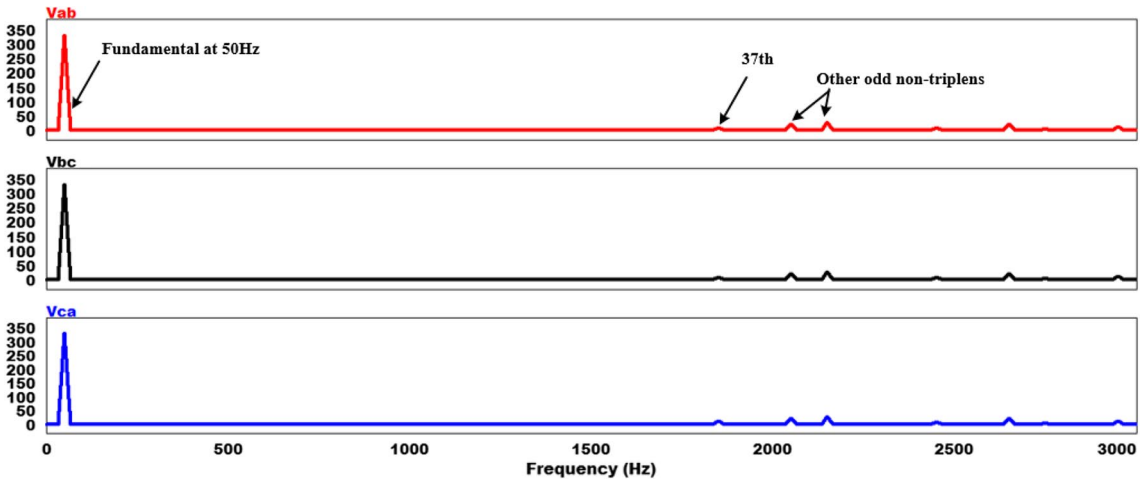

Fig. 9 FFT Spectrum of the Line to Line waveform

Figure 9 shows the FFT of the three-phase line to line voltages; all the triplens harmonics in the spectrum cancel each other in the line voltage, which conforms with the existing literature [3].

Without the filtering circuit, the output total harmonic distortion (THD) of to the 49th harmonic order (2.5 kHz) was measured to be 11.25%, which is not close to the acceptable IEEE 5% standard. However, since the harmonics are at a higher frequency, a small-sized low pass filter will be sufficient. As such to minimize the THD, an LC filter is designed for the inverter topology. An 8.3nF capacitor and 1mH inductors were used for the filtering circuit. Figure 10 shows the three-phase filtered output voltage waveforms, which appear to be almost a pure sinusoidal output waveform.

Figure 11 shows the superimposed the FFT spectrum of the filtered three-phase waveforms. The LC filter has successfully eliminated all the higher-order harmonics, leaving behind only the fundamental component. The THD over the entire spectrum stood at 1.25% at 2 kW loading. Hence, satisfy the IEEE standard THD requirement of less than 5%.

3.3 Topologies device counts comparison

Table 3 presents the power switches and DC source expressions of seven different converter topologies [5–7, 21, 22]. The expressions have the number of output steps (k) as the variable. Figure 12 is the histogram plot comparing the number of power electronic switches in the seven topologies. It shows that the proposed converter has less number of power electronic switches compared with the said topologies except for the one in [21] that has the same number, while the one in [23] has lesser. Majority of the topologies shows a proportional relationship between the output voltage step and the number of DC sources in the

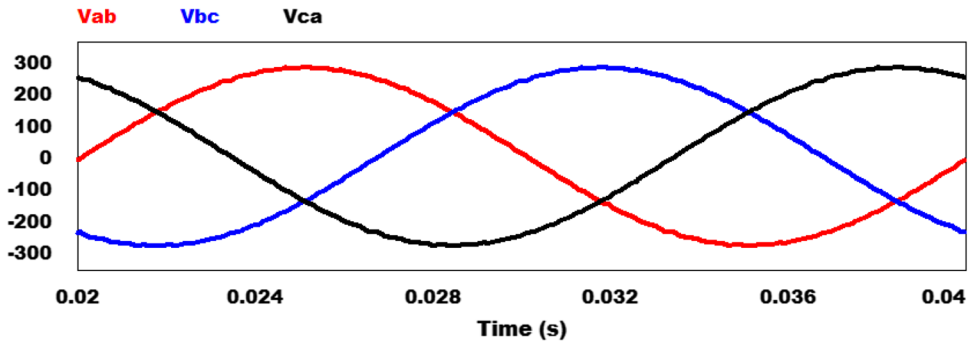

Fig. 10 Filtered output waveform

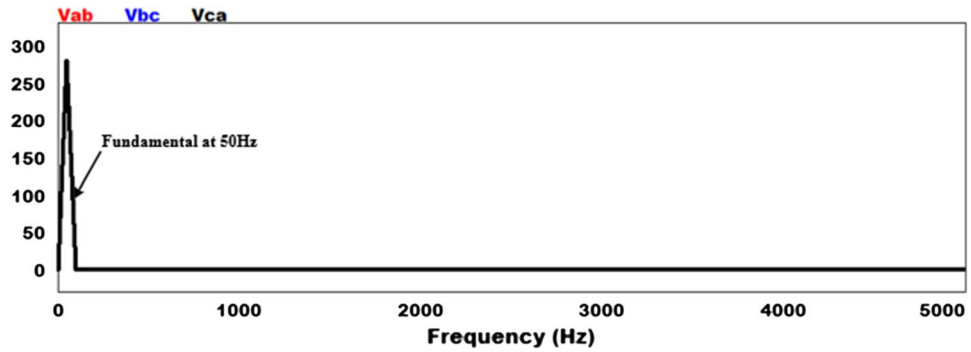

Fig. 11 FFT of the filtered output waveforms

Table 3 Components comparison between conventional 9-level Multilevel inverter topologies and the proposed

Topology type	No of switches	Dc-Bus
Diode-clamp (DiC) [5]	6(K − 1)	(K − 1)
Flying capacitor (FC) [6]	6(K − 1)	(K − 1)
Cascaded H-bridge (CHB) [7]	6(K − 1)	0.5(K − 1)
New MLI with reduced count (NMLTRC) [21]	12 + 1.5(K − 1)	1.5(K − 1)
New MLI with self-balancing level (NMLISBL) [22]	3(K + 1)	0.5(3K + 1)
Novel MLI with minimum switch number (NMLIMSN) [23]	12 + 1.5(K − 3)	0.5(K − 1) + 3
Proposed topology	6(K − 5)	1

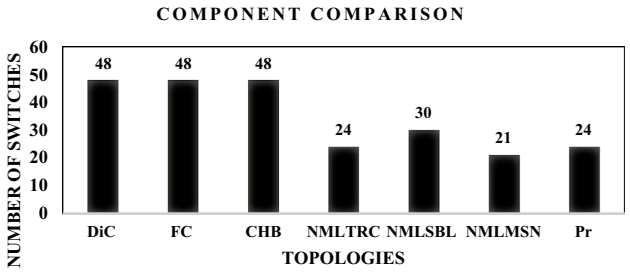

Fig. 12 Component comparison

circuit. Figure 13 shows a plot comparing the DC sources in each topology against the standard MLI output steps (7, 9, 11, 13 etc.). The plot shows that NMLTRC has the highest number of DC inputs with increasing output steps. This further verified the existence of a relationship between the number of DC sources and the output steps of an MLI topology. Only the proposed topology denoted by (Pr) remains constant at all output steps. Therefore, combining both the number of power switches and the DC sources, it can be drawn that the proposed topology has the minimum number of components.

3.4 Comparison between conventional and proposed topology

To ascertain the performance of the proposed topology, it is compared against the conventional three-phase cascaded H-bridge converter. Figures 14 and 15 shows the conventional 3-phase nine-level output waveform and its FFT plot respectively. From the FFT it can be seen that the

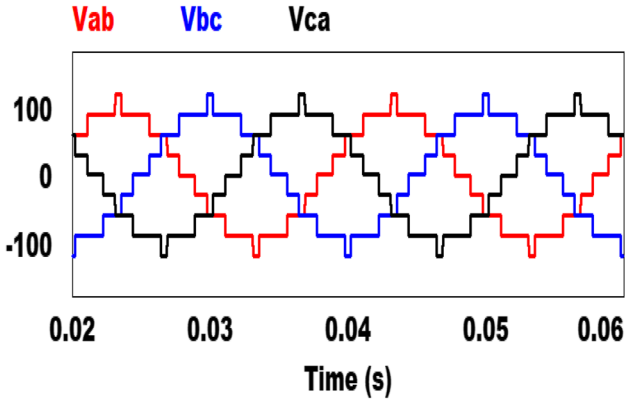

Fig. 14 Conventional 3-phase output waveform

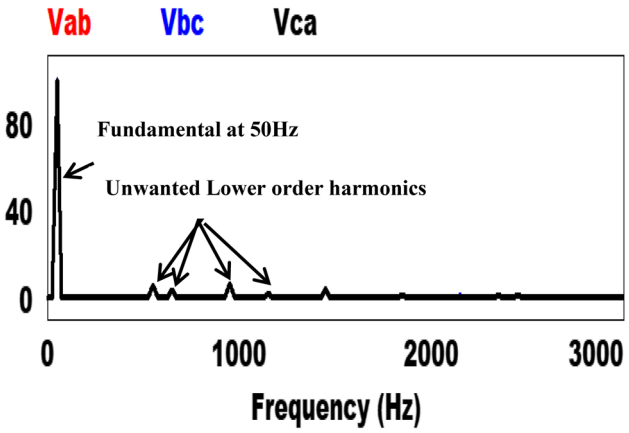

Fig. 15 FFT spectrum of the un-filtered conventional line to line waveform

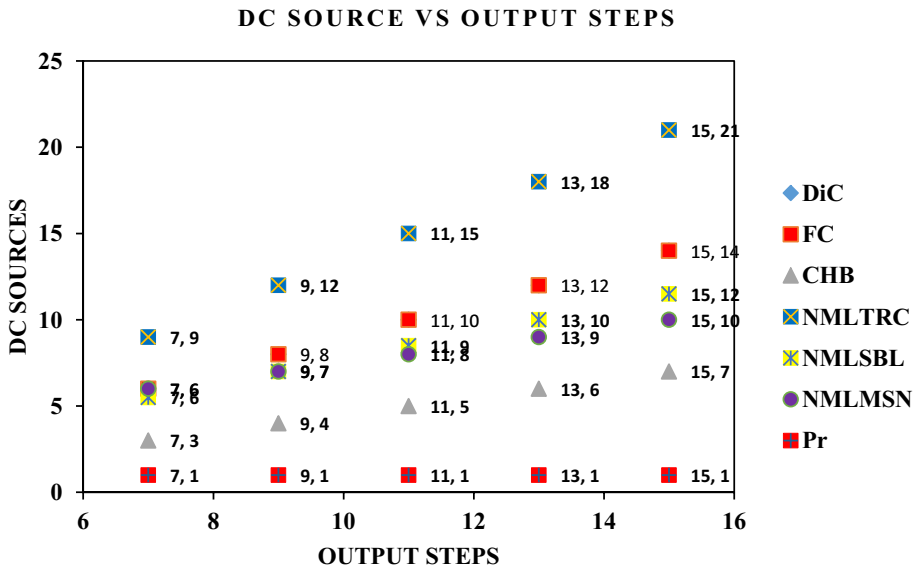

Fig. 13 DC source comparison. *FC* flying capacitor, *DiC* diode clamp, *CHB* cascaded H-bridge, *NMLTRC* new MLI with reduced count, *NMLISBL* new MLI with self-balancing level, *NMLIMSN* novel MLI with minimum switch number, *Pr* proposed topology

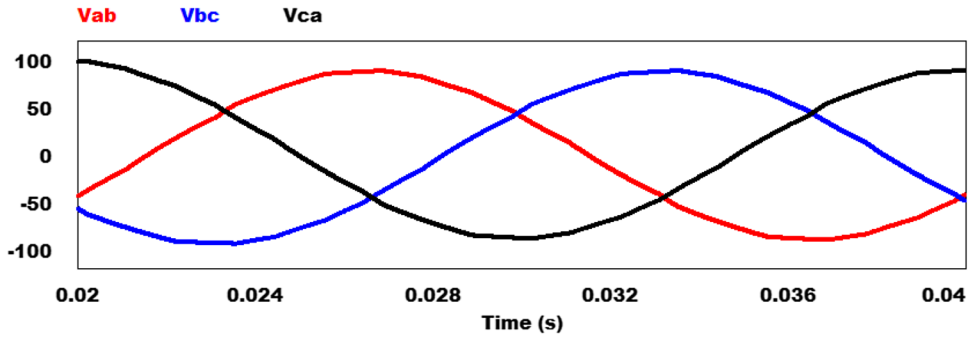

Fig. 16 Filtered conventional waveform

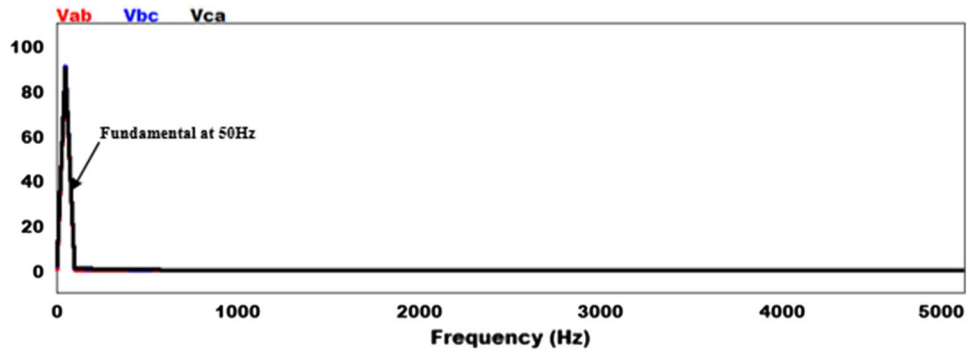

Fig. 17 FFT Spectrum of the filtered conventional line to line waveform

conventional is not capable of eliminating the harmonics completely, but rather suppresses them. The THD value obtained at 2 kW is 13.01% which is far above the IEEE 5% standard. Therefore, the topology requires the need for a filter.

A filter is designed for the conventional converter at the same frequency as the proposed topology. Figure 16 shows the three-phase filtered output voltage waveforms, while Fig. 17 shows the FFT. From the FFT it can be seen that the visible harmonics in the unfiltered are either suppressed or eliminated. The THD at 2 kW stood at 2.73%.

Figure 18 shows the Total Harmonic Distortion (THD) and output power plot of both the proposed and conventional 3-phase Cascaded H- bridge MLI. Usually, as the output power of an inverter increases the THD is expected to decay exponentially [12, 13]. As seen both converter topology exhibits the same characteristics. From the plot, the proposed converter has less amount of THD than conventional topology. At 500 W the proposed topology has 4.99% THD which satisfies the below 5% standard as compared to the 7.91% of the conventional at the same loading. This shows the effectiveness of the proposed topology in eliminating harmonics.

Figure 19 is the efficiency vs output power plots for the proposed and conventional topologies. Both curves follow the normal inverter efficiency curve which has transient and steady-state portions. Based on the graph, the

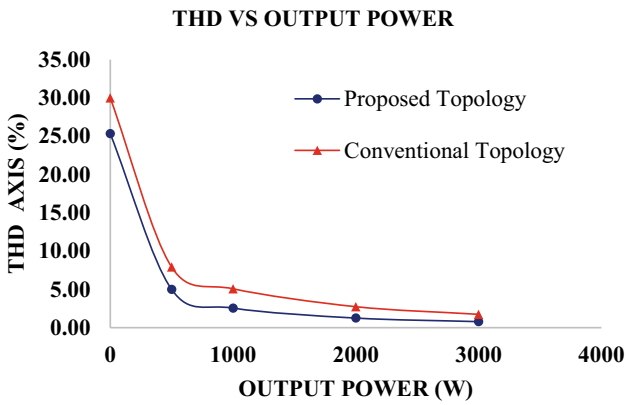

Fig. 18 THD comparison

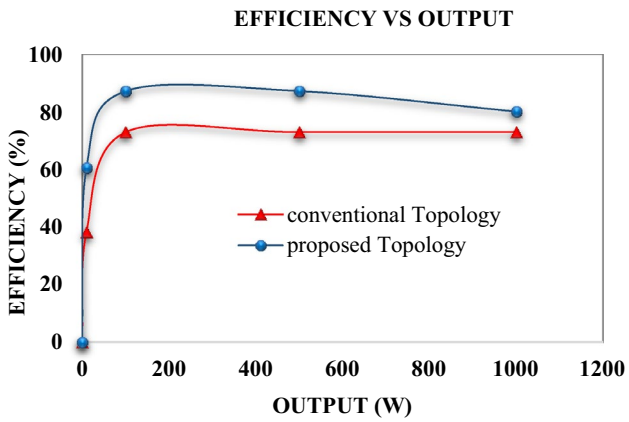

Fig. 19 Efficiency comparison

proposed topology exhibits better efficiency than the conventional at all power output level. This further ascertains the viability of the proposed topology and the control technique involved over it conventional counterpart.

4 Conclusion

The objective of this research is to develop an inverter with less output harmonics and reduced device count. Therefore, a 3-phase five-level MLI output waveform was realized using a single Dc source and a modified cascaded H-bridge topology. The inverter was controlled using selective harmonic elimination technique where the nonlinear transcendental equations were solved using an optimized genetic algorithm to obtain the switching angles. The harmonic contents obtained over a range of output power satisfies the IEEE standards. The number of power electronic switches and the DC source for the proposed topology was compared against six other topologies, where it turns out to have the least number of components. Efficiency and THD of the proposed topology were compared against a conventional 3-phase H-bridge having the same number of output level. The proposed appeared to have better efficiency and has the least output harmonic distortions. Therefore, it can be concluded that the control strategy and the proposed topology are suitable for fixed frequency applications standalone applications. For future recommendations, fault-tolerant control can be employed on the topology to exploit its modularity and redundant switching. In addition, different optimizers and modulation techniques can be used on the topology to assess its performance. Different transformer turns ratio as well as switching angle distribution can be used to increase the inverter output steps and harmonic eliminations capabilities.

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Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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