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Solution-Processed Insulators for Flexible Metal-Insulator-Metal Structures

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Repeatable switching hysterisis in metal-insulator-metal devices is commonly attributed to the motion of oxygen vacancies under a sufficiently large external electric field. The resulting memristive behaviour has become a compelling alternative to traditional non-volatile memory device architectures. A room-temperature process for the fabrication of a metal-insulator-metal structure employing niobium pentaoxide (Nb_2O_5) as the active layer has been developed, without any annealing of the oxide film. Electrical characterization of the devices shows sharp switching of resistivity. The developed process is very simple, cost-effective and can be implemented on flexible substrates.

Key words: MIM structures, sol–gel, spin coating, non-volatile memory, flexible electronics

INTRODUCTION

Flexible and implantable systems with sensor applications often require the application of non-conventional processing methods.[1,2] Low-cost, low-operating voltage and low-power memory are emerging needs for data storage in such implantable devices that measure body vitals, perhaps as implants. Fabrication of these devices has been demonstrated using distinct precursors as well as pre-synthesized nanomaterials by printed techniques.[3,4] However, deployment of unusual device components like solar cells, energy efficient displays,[5] etc. in these systems makes it challenging to realize full advantages of traditional integration like reduced parasitics, overall weight and size.

The incomplete fourth quadrant of passive elements linking basic quantities: charge, voltage, current, and flux, was addressed in 1971.[6] Performance parameters like low power consumption7, high endurance, good retention ratio (low resistive state (LRS) versus high resistive state (HRS)), high device yield, long retention times and multilevel logic/memory[8] are desirable in addressing requirements for non-volatile memory devices. Pinched current–voltage (I–V) hyteresis loops observed in these devices are understood to be a result of motion of oxygen vacancies.[9] Switching states between HRS to LRS are observed in bistable mode on application of bias voltage. The switching state changes to the other state only after application of a minimal bias (switching voltage), resulting in non-volatile memory.

Organic semiconductor based thin film structures were one of the early exemplars for storage of multilevel states[10] in stacks of metal-insulator-metal(MIM) structures. Conventional memristors involve a combination of active and inert metal electrodes, while binary oxides like TiO_2, ZnO, CuO, HfO_2, Nb_2O_5[11–13] are the usual sandwiched insulator layers. Commonly used deposition techniques like atomic layer deposition, electron beam evaporation, pulsed laser deposition, anodic oxidation and ion-assisted sputtering[14–16] are used to deposit the

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insulating layer. Memristors with high retention ratio, repeatable switching hysteresis, and high endurance have been demonstrated. However, these fabrication processes employ high temperature annealing, which adds to the processing cost and limits applicability to rigid substrates exclusively.[17] Solution-processed memristor devices suggest an alternate processing pathway.[18]

Binary metal oxides like Nb_2O_5[16] have been used as thin film layers[19,20] in diverse device applications. These can be used as dispersible functionalized inks[3] for printing on the flexible substrates. Removal of the bonded functional groups in the dried film can pose a challenge. We have developed a solution-processed Nb_2O_5 deposition technique at room temperature to obtain repeatable thin films for MIM structures on flexible substrates.

MATERIALS AND METHODS

The precursors used for sol synthesis of Nb_2O_5 were $Nb(OC_2H_5)_5$ dissolved in a mixture of ethanol and acetonitrile, which were continuously stirred, to make a homogeneous solution and stirring continued for another 3h.[21,22] This turbid sol solution was later used for deposition of the devices. To confirm the phase purity of Nb_2O_5, a portion of the product was calcined at 750°C for 3h in air. The collected product was characterized by powder x-ray diffraction study (PXRD) on a Bruker D8 Advance using Ni filtered Cu-Kα radiation (Fig. 1), using scans recorded with a step size of 0.02° and a step time of 1 s. Kα2 reflections were removed to obtain accurate lattice constants. The result was analyzed and found to have crystallized in the orthorhombic

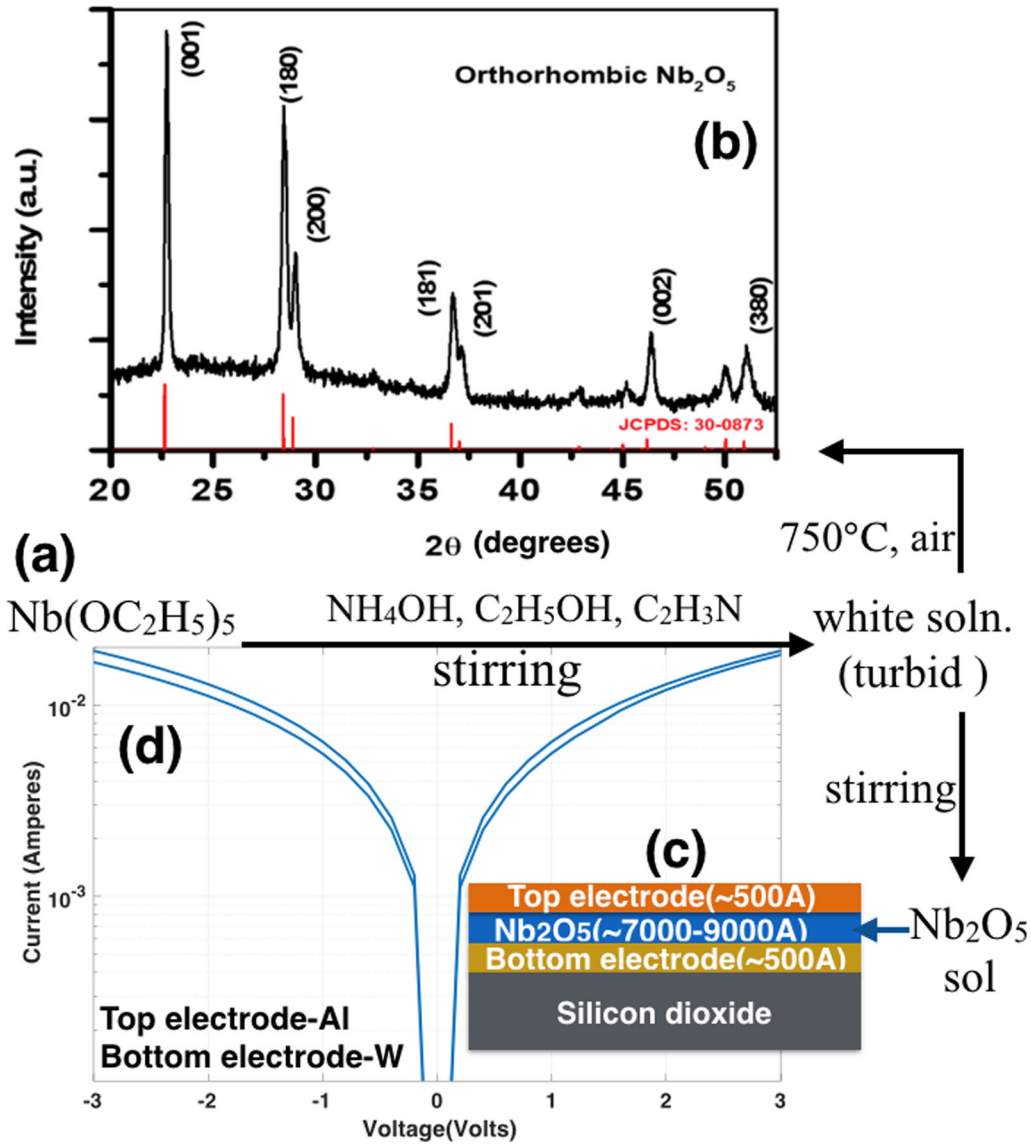

Fig. 1. (a) Nb_2O_5 sol synthesis, and process steps. Insets: (b) Powder XRD data confirming the formation of Nb_2O_5, (c) device schematic, and (d) current voltage characteristics of initial devices with W and Al contacts.

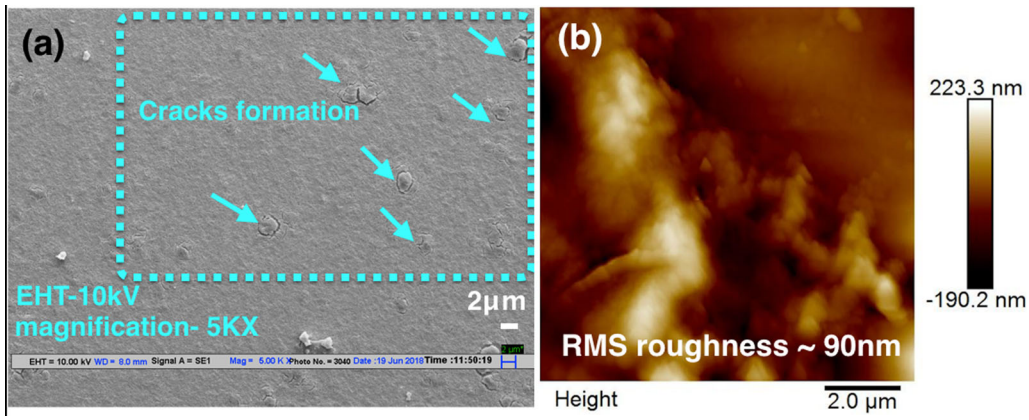

Fig. 2. Nb_2O_5 film morphology: (a) high resolution scanning electronic micrograph in the deposited Nb_2O_5 film exhibiting cracks and pinholes in the film at low thicknesses, and (b) atomic force microscopy scan of the Nb_2O_5 thin film after multiple depositions.

system (JCPDS-300873).[19] The elemental composition of niobium (V)oxide was confirmed using energy dispersive x-ray spectroscopy (EDX).

The devices were fabricated using Nb_2O_5 as an insulating film on a commercial silicon dioxide substrate (University Wafers) with a thickness of 500μm. Bottom electrodes (W (500 Å) or Cr/Au(200 Å/500 Å)) were grown using DC sputtering at a pressure $\sim 10^{-7}$ kPa chamber integrated into a glove box (Angstrom Engineering). The bottom electrodes (W and Cr/Au) were chosen to avoid oxidation during subsequent processing. The prepared sol was deposited using spin coating (spin NXG-P2) at <3000 rpm, and vacuum dried. Spin-coating was repeated after each drying step several times to obtain a uniform layer (thickness $\sim$ 7000–9000 Å) with minimum cracks and pin-holes as shown in Fig. 2. A sample of the sol deposited thin film was analyzed using atomic force microscopy (AFM) scans over an area of 1μm by 1μm to obtain a surface roughness of 900 Å (Fig. 2). Finally, the devices were completed with a thermally evaporated top electrode (Al (500 Å) or Ag (500 Å)) to form a crossbar geometry (Fig. 3, device area: 1 mm $\times$ 1 mm).

RESULTS AND DISCUSSION

It was found during subsequent testing that devices with W/Al contacts developed high contact resistance. As a result, devices with Au/Ag contacts (yield $\sim$ 60%) were characterized. The fabricated device was characterized by applying a DC bias using a semiconductor parametric analyzer (Agilent B15000). Electroforming process was initiated by the application of DC bias that created switching centres in the device. Depending upon the voltage polarity, electroforming can be positive or negative. In this process, the top electrode (Ag) is biased with respect to the bottom electrode (Au), which was grounded. The pristine device is assumed to be in a high resistive state (HRS). For electroforming the device, an initial bias from 0 V to + 5 V (positive

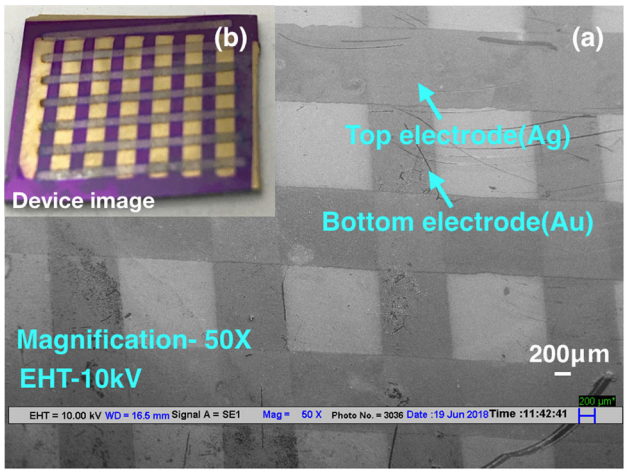

Fig. 3. (a) Scanning electron micrograph showing the cross-bar geometry of the devices. Inset: (b) image of the device.

electroforming) was applied, during which an electroreduction process takes place, followed by vacancy creation. This helps the pristine device obtain resistive switching behaviour[23] before hitting the compliance current. After electroforming, which involves an increase of current, corresponding to a low resistive state (LRS), was observed, which sets the lower limit of the bias voltage range of the device. On application of bias from + 5 V to 0V (set process), the device switches from LRS to HRS. During testing, the reset and set process is repeated from 0 to − 5 V and − 5 V to + 5 V, respectively. Reliability of fabricated devices is tested over 1030 write-read cycles with minimal degradation of the device. For test devices reported here, after initial switching (set and reset process), bias from + 5 V to − 5 V in the dual sweep mode is applied to obtain resistive switching.

Current voltage characteristics (Figs. 1 and 4) were measured repeatedly from + 5 V to − 5 V and exhibit clear hysteresis. This bistable, non-volatile and switching behaviour is comparable[18,24] to

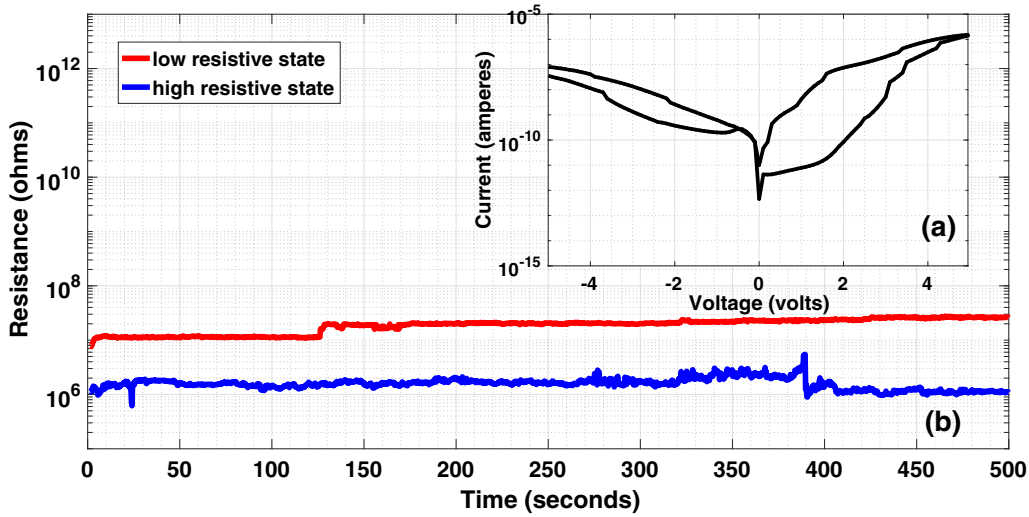

Fig. 4. Electrical characterization: (a) current–voltage characteristics of the device with Au and Ag contacts, (b) retention characteristics.

earlier reports. LRS ($\sim$ 1MΩ) and HRS ($\sim$ 10MΩ) retention characteristics (Fig. 4) were obtained for 500 s by switching the device in LRS and HRS seperately and measuring current versus time at a constant step voltage. The resulting retention ratio (= 10) is obtained by averaging over at least ten cycles.

The observed electrical characteristics are consistent with the theoretical memristor behaviour[24,25] showing drift of oxygen vacancies in niobium pentoxide under the application of bias.[16,26–29] This tunneling behavior of the oxygen vacancies leads to the obtained pinch hysteresis loop. The motion of oxygen vacancies changes when the bias polarity is reversed. Vacancy drift occurs through the formation and rupture of conducting filaments.[30,31] Bistable electrical characteristics are expected to be a result of filament switching[32] because of dissimilar top and bottom electrodes.

Although the Nb_2O_5 film was deposited using a sol gel method at room temperature that is expected to result in the formation of amorphous films, the electrical characteristics obtained are comparable to the memristors fabricated by conventional techniques like sputtering and anodic oxidation. Unlike other reports cited earlier, reported devices do not involve heating of the substrates during deposition or post-annealing (reports vary from 60°C[33] to 800°C[34,35]). This makes the process employed in the fabrication of these devices compatible with flexible electronics,[17] and sensor systems integrated on flexible substrates. Work is ongoing on reduction of the switching voltages by thinning the active layer through a better control of film morphology through surface treatment and post-deposition processing at room temperature.

CONCLUSION

MIM device structures using a Nb_2O_5 dielectric layer were fabricated via the sol gel route at room temperature, with sputtered (bottom) and evaporated(top) contacts. DC I–V characteristic measurements show reproducible, bistable electrical response that is consistent with memristive behaviour at low operating voltages from + 5 V to − 5 V. Since this method does not involve any heat treatment, it can be implemented on flexible substrates like polymide, polycarbonate, polyethylene terephthalate (PET), etc. Potential applications include wearable electronics, bioimplantable soft devices, large area sensors, and integrated memory devices in flexible electronic systems.

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CONFLCIT OF INTEREST

The authors declare that they have no conflicts of interest.

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