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Editorial

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Similar to the previous issue, this one also contains 11 articles. This time the focus is 3D-stacked devices (1), reversible logic (1), product quality (1), memory test (2), signal integrity (1), and hardware security (3). We also have two *JETTA Letters*.

The first article discusses testing of 3D-stacked devices. Their manufacturing involves wafer processing, bonding of wafers or chips, and packaging. Testing at each step has costs and benefits. The proposed test flow selection algorithm (TFSA) considers the available test hardware, test time and yield for various steps to optimize the overall testing process. Contributors are SenGupta, Nikolov and Larsson from Lund University, Lund, Sweden and Dash from Linköping University, Linköping, Sweden.

The second paper develops an automatic test pattern generation (ATPG) algorithm for various types of bridging faults in reversible logic circuits. The number of tests is kept to a minimum and all faults are detected. Authors are Handique and Deka from Indian Institute of Technology, Guwahati, Assam, India and Biswas from Indian Institute of Technology, Bhilai, Chhattisgarh, India.

The third paper proposes a repeated testing method for improving the product quality. During a test, the measured values of signals depend upon the timing accuracy of the automatic test equipment (ATE). To account for the measurement inaccuracy, a guard band prevents majority of bad devices from passing test. This, however, introduces pessimism in the pass/fail decision, failing some good devices and reducing tester yield. If we relax the guard band then fewer good devices will fail raising the tester yield, but more bad devices will pass lowering the quality. In repeated testing, only the device passing every time is taken as good. For a given ATE timing accuracy, proper choices of guard band and number of test repetitions can simultaneously enhance both product quality and tester yield. This work is contributed by Yeh and Chen from National Central University, Jhongli City, Taoyuan County, Taiwan.

Next, we have two papers on memory test. The first is authored by Princy and Sivamangai from Karunya Institute of Technology and Sciences, Coimbatore, India. The use of transient current measurement has been proposed for detection of data retention faults (DRF) in static memories. But the reliability of this method is affected by process variation. This paper shows that wavelet analysis of the transient current measured at the power supply terminal of the memory can improve the fault detection accuracy.

The second memory test paper, the fifth in this issue, addresses the problem of DRF in dynamic RAM. DRAM cells retain data for limited time and should be refreshed. To account for cell-to-cell variation of data retention time, cells with identical retention time form refresh clusters. Any cells that cannot be refreshed must be excluded from the memory operation. The authors, Lu and Huang from National Taiwan University of Science and Technology, Taipei, Taiwan, Hsu and Sun from Industrial Technology Research Institute (ITRI), Taiwan and Miyase from Kyushu Institute of Technology, Fukuoka, Japan, propose address remapping for improved clustering. Claimed benefits are reduced refresh power and higher yield.

The sixth paper examines crosstalk among high speed interconnects on a multilayer printed circuit board (PCB). The authors consider impedance mismatch, reflection, and S-parameters for interconnect pairs. Time domain reflectometry (TDR) is employed to analyze and design interconnects. Contributors of this work are Kavitha from Veltech Multitech Dr. Rangarajan and Dr. Sakunthala Engineering College, Avadi, Chennai, Tamilnadu, India, Sekhararao from Anna University, Tamilnadu, India, Swaminathan from Godavari Institute of Engineering Technology, Rajamundry, Andhra Pradesh, India and Ahemedali from Sasi Institute of Technology and Engineering, Tadepalligudem, Andhra Pradesh, India.

The seventh, eighth and ninth papers are on hardware security. In the seventh paper, Lambić, from Ton Duc Thang University, Ho Chi Minh City, Vietnam, analyzes shortcoming

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of the pseudorandom number generator (PRNG) that uses a piecewise logistic map. An improved version of this PRNG is also proposed.

In the eighth paper, Liu, He, Ma and Zhao from Tianjin University, Tianjin, China propose the use of a golden layout model instead of actual golden chip hardware. Their Trojan detection method uses side channel analysis.

In the ninth paper, Kokila and Ramasubramanian, from National Institute of Technology, Tiruchirappalli, India, devise physically unclonable function (PUF) based authentication hardware for various systems.

In the first *Letter*, Kang, Chae and Jeong from Samsung Electro-Mechanics, Suwon, Gyeonggi-do, Republic of Korea, provide a method for testing interconnects of a system-in-package (SiP) after components have been mounted. In the second *Letter*, Zhang, Li and Zheng from University of Electronic Science and Technology of China, Chengdu, China, discuss radio frequency (RF) testing.