Journal of Electronic Testing
https://doi.org/10.1007/s10836-019-05805-z

Editorial

Vishwani D. Agrawal[1]

Received: 10 May 2019 / Accepted: 10 May 2019

There are 11 articles in this issue. They focus on hardware security, delay test, mixed-signal test, radio frequency (RF) test, fault tolerance and reliability. The eighth article is a detailed version of a paper that appeared at the Nineteenth IEEE Latin American Test Symposium (LATS) held during March 12–16, 2018 in Sao Paolo, Brazil.

The first of two papers on hardware security surveys the literature on logic locking. *Logic locking* is a design for security technique in which a circuit intentionally works incorrectly unless a specified signal, called secret key, is applied to certain inputs. Authors, Dupuis and Flottes from LIRMM, Université de Montpellier, CNRS, France, list 78 references summarizing the research of a decade.

The second paper provides a method for detecting the presence of Trojans from the measurement and analysis of temperature distribution on the chip. Authors are Tang, Liang and Li from National University of Defense Technology, Changsha, Hunan, China.

The third paper discusses delay testing in the context of adaptive voltage scaling (AVS), which has become popular for power and performance tradeoff or optimization. This contribution comes from Zandrahimi and Al-Ars of Delft University of Technology, Delft, Netherlands, and Debaud and Castillejo of STMicroelectronics, Grenoble, France. Their research shows that path delay testing provides the most effective guidance for implementing AVS when manufacturing process variation is present.

In the fourth paper, Kundu from Intel Corporation, Santa Clara, CA, USA, and Su and Goteti from Intel Corporation, Folsom, CA, USA address mixed-signal test. They examine concurrent (in operation) testing of mixed-signal circuits. Because of varying operating conditions, anomalous behavior (transient or intermittent error) is observed, which is analyzed by learning techniques to diagnose faults in the circuit.

Next, we have three papers on radio frequency (RF) test. In the fifth paper, Shafiee from Broadcom and Ozev from Arizona State University, Tempe, AZ, USA examine the state of the art of testing phased array antennas embedded in communications devices. They present a contactless test method based on near-field measurement, though a requirement is that a known good device is available.

The sixth paper illustrates an analytical procedure to find an optimal test signal for a given radio electronic system under test and a measurement test system, assuming the presence of Gaussian noise. Authors are Herasimov, Pavlii and Tymoshchuk from Ivan Kozhedub Kharkiv National Air Force University, Karkiv, Ukraine; Yakovlev from National Academy of the National Guard of Ukraine, Karkiv, Ukraine; Khaustov, Ryzhov and Nastishin, from Hetman Petro Sahaidachnyi National Army Academy, Lviv, Ukraine; and Sakovych from National Technical University of Ukraine, Kyiv, Ukraine.

In the seventh paper, Al-kanan, Yang and Li, from Portland State University, Portland, OR, USA, use the Saleh model to represent the behavior of a power amplifier (PA). They compute the model parameters from the gain and third order intercept point of the PA. The model then allows determination of a predistortion function that linearizes the gain characteristic of the PA.

The last four papers follow themes of fault-tolerance and reliability. In the first of these, Rodrigues, Barros and Kastensmidt from Federal University of Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, Pouget from CNRS, France, and Bosio from Ecole Centrale de Lyon, Lyon, France assess the reliability of successive approximation algorithms. They execute the algorithm on a processor while injecting faults by striking the cache with laser beam. The paper reports useful results about several types of faults.

In the next paper, Geetha and Amritvalli from Coimbatore Institute of Technology, Coimbatore, India design error tolerant adders using the gate-diffusion input (GDI) logic technology. Depending on the acceptable error-tolerance permitted by the particular application, parts of the carry propagation circuit are simplified to save power, reduce hardware and enhance

✉ Vishwani D. Agrawal
agrawvd@auburn.edu

[1] Auburn University, Auburn, AL 36849, USA

Published online: 18 May 2019

speed. These advantages further amplify with the use of the GDI logic.

Next, a paper by Hajian and Safari from University of Tehran, Iran offers an efficient method to determine the soft error rate (SET) of near-threshold (low voltage) circuits due to single event transients (SET). The authors make use of various types of neural networks to achieve speed up of nearly 20 times over a compute intensive simulation alternative. In addition, the procedure is inexpensive compared to exposing the circuit to high-energy ions and measuring the error rate.

The eleventh and the final paper is authored by Li and Xiao from Harbin Institute of Technology, Harbin, China, and Reviriego from Universidad Carlos III de Madrid, Spain. Discussing multiple cell upsets in a memory, they argue that the use of more complex error correcting codes increases the complexity of encoders and decoders, slowing down the memory. They present techniques to reduce the decoding delay of a 3-bit burst error correcting code.