Chapter 5
IO Buffers

We have designed the circuit that realizes the desired functionality, but how do we exchange signals with the outside of our chip? We simply connect lines on the circuit diagram, but it probably isn’t so easy in reality…

5.1 Signal Path Between Chips

When chips are connected to each other and signals are exchanged, as shown in Fig. 5.1, the signal is output from the pad connected to the interior of the chip, which goes through the bonding wire, the lead frame of the package, and the transmission line on the board, which then goes through the other chip’s lead frame, bonding wire, and pad, to finally arrive at the receive circuit as input.

These channels have impedances which are a complicated combination of resistances, capacitances, and inductances. Therefore, to transmit and receive signals cleanly through these kinds of channels, it is necessary to estimate the impedances of these channels and design corresponding input-output circuits.

5.1.1 Pads

In a chip layout as in Fig. 5.2a, rectangular shapes in rows on the chip periphery can often be observed. These are called the pads (or IO pads). In recent processes, the pad pitch is about 60 μm. Also, because these take up a large area, they have a parasitic capacitance with the substrate surface of several hundred fF ~ 1 pF.

The chip surface is covered by a layer called passivation film so that dust and moisture do not enter the inner parts of the chip. Polyimide is often used as the material for the passivation layer. Here, the passivation has a window of opening for
the pads, and signals are transmitted and received between the inside and outside of the chip through this window.

The cross section of pads is shown in Fig. 5.2b. The uppermost layer of metal is called the pad metal and is used as pads. Underneath the pads, all routing layers connected by vias could be placed (digital pads), or nothing could be placed at all (RF pads). RF pads can be used for the input and output of fast signals, because RF pads have smaller parasitic capacitances to the substrate. However, as indicated in Fig. 5.2b, RF pads are more vulnerable to damage during bonding, so digital pads that have higher structural integrity are also used often. Although the parasitic capacitance will increase, this is better than malfunctions.

### 5.1.2 Packages and Bonding Wires

Packages come in many shapes and forms, such as quad flat package (QFP), small outline package (SOP), ball grid array (BGA), and so on. As for the material, there are ceramic packages that use ceramics and plastic packages that use plastic. In general ceramic packages have multiple functionalities and options, such as built-in transmission lines, added capacitance to the package internals, and structures with removable covers. However, these can become very expensive, and a single package can cost around 100USD. Plastic packages on the other hand do not have such capabilities but are priced at several cents a piece.
5.1 Signal Path Between Chips

A photograph of a ceramic QFP and plastic SOP that were at hand is shown in Fig. 5.3. The cover of the ceramic package is opened so that the bonding wires and lead frames are also visible. Gold wires with diameters of tens of μm are typically used for the bonding wires.

Now, it can be readily imagined that the lead frame and bonding wires have some impedance. As a rule of thumb, it is good to remember “1 nH per 1 mm.” Of course there are also resistance and capacitance components, but these are negligible compared to the inductance. In Fig. 5.3, the inductance is several nH. Inductance needs to be suppressed, because otherwise the waveforms of fast signals can become distorted or large supply noise can be generated due to internal switching. Also, package sizes are large relative to chip sizes, and this becomes a hindrance to miniaturization of instruments. To solve these issues, strategies such as chip-size package (CSP) or flip chip bonding, which does not use packages (Fig. 5.4), are sometimes used.

However, because handling the chips is difficult with flip chip bonding, in recent years, multi-chip packages as illustrated in Fig. 5.5 are also being used. By doing so, a low impedance connection between chips exchanging fast signals can be made possible by placing them in the same package, while achieving miniaturization as well.

Fig. 5.3 Photograph of packages

Fig. 5.4 Flip chip bonding. (a) forming bumps, (b) bonding
5.1.3 Transmission Lines

5.1.3.1 Characteristic Impedance

When a voltage $V_0$ is applied to resistances $R_s$ and $R_L$, which are connected by a “long” wire, as shown in Fig. 5.6a, what happens? Would the current become $V_0/(R_s + R_L)$ from the instant the voltage rises? When and how would the current know that a resistance $R_L$ exists at the end of this “long” wire?

If the resistance of the wire is ignored, all wires (regardless of whether the wire is “long” or not) contain inductance and capacitance as indicated in Fig. 5.6b. If $L$ and $C$ are the inductance and capacitance per unit length,

$$Z_0 = \sqrt{\frac{L}{C}}$$

(5.1)

is called the characteristic impedance. The current, which does not know what is connected at the end of the long wire, will enter the wire believing that the characteristic impedance $Z_0$ is connected at the end, as indicated in Fig. 5.6c. That is, a current of $I = V_0/(R_s + Z_0)$ initially starts to flow. This current reaches the resistance $R_L$ at the speed of light $c$. In spite of the current’s belief that $Z_0$ was connected, it will discover that in fact $R_L$ is connected, and . . . then what?

5.1.3.2 Termination and Reflection

Various phenomena occur by adjusting the impedance connected at the end of the “long” wire. This is called “termination.”

The initial current that flows into the wire $I_{if}$ and initial voltage $V_{if}$ are $I_{if} = \frac{V_0}{R_s + Z_0}$ and $V_{if} = \frac{Z_0}{R_s + Z_0}V_0$, respectively. When the wire is terminated by $Z_0$ ($R_L = Z_0$), the current that came along the wire believing that there is a $Z_0$ at the end actually finds the $Z_0$ and flows directly into $G_{ND}$. This is called matched termination or impedance matching.
On the other hand, if there is not a $Z_0$ but a $Z_L$ that is connected, then part of the current will “reflect” and come back, as indicated in Fig. 5.6d. If the reflectance is $\Gamma_L$, then the reflected current and voltage $I_{1b}$ and $V_{1b}$ are $I_{1b} = \Gamma_L I_{1f}$ (left is the positive direction) and $V_{1b} = \Gamma_L V_{1f}$, respectively. The current that does not reflect back but enters $Z_L$ is $I_{1L} = (1 - \Gamma_L)I_{1f}$. Here, the voltage at the right end is $V_{1L} = V_{1f} + V_{1b}$, and this is equal to the voltage that is generated on the termination $Z_L$. That is,

$$V_{1f} + \Gamma_L V_{1f} = (1 - \Gamma_L)I_{1f}Z_L$$

(5.2)

and the reflectance $\Gamma_L$ can be derived from this equation and $V_{1f} = I_{1f}Z_0$ as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}.$$ 

(5.3)
The current that reflected and came back is reflected again as shown in Fig. 5.6e:

\[ \Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \]  

(5.4)

and a portion flows to the right. These reflections are repeated until the currents and voltages settle to their final values (the equations converge when \(|\Gamma_s, \Gamma_L| < 1\)).

Here, for example, in Fig. 5.6e, the current going to the right is \(I_{1f} - I_{1b} + I_{2f}\), and the voltage is \(V_{1f} + V_{1b} + V_{2f}\). Be aware that the current changes signs depending on whether it is traveling right or left, whereas the voltage has no sign.

The reflecting signals are schematically indicated in Fig. 5.7a. The traveling signals are indicated on the horizontal axis, and the vertical axis indicates time. At time \(T_p\), the signal arrives at the rightmost point (receiving end), and the voltage at that time is \(V_{1f} + V_{1b}\). The reflected wave \(V_{1b}\) is again reflected at the leftmost point (transmitting end), and at time \(3T_p\), the re-reflected wave arrives at the receiving end. The voltage at that time is \(V_{1f} + V_{1b} + V_{2f} + V_{2b}\). According to Eq. (5.3), the reflection coefficient is positive when the termination impedance is greater than the characteristic impedance (\(Z_L - Z_0 > 0\)) and negative when the termination impedance is less than the characteristic impedance (\(Z_L - Z_0 < 0\)). Therefore, there are four possible combinations of the impedances of the transmitting and receiving ends being greater than or less than the characteristic impedance. For each situation,
the voltage waveform at the receiving end is shown in Fig. 5.7b–e. The voltage can asymptotically approach the final voltage monotonically or by oscillating.

As an extreme example, when $Z_s = Z_0$ (matched termination) and $Z_L = \infty$ (open termination), the situation is in between Fig. 5.7b, c, and $I_{if} = V_0/(2Z_0)$, $V_{if} = V_0/2$, $\Gamma_s = 1$, $I_{ib} = \Gamma_L I_{if} = I_{if}$, $V_{ib} = \Gamma_L V_{if} = V_{if}$, $\Gamma_s = 0$, $I_{2f} = 0$, and $V_{2f} = 0$. That is, the voltage at the receiving end is zero until the signal arrives, and at time $T_p$ becomes $V_0/2$, but the arrival and reflection occur simultaneously and the voltage becomes $V_0$ ($V_{if} = V_{ib} = V_0/2$, $V_{if} + V_{ib} = V_0$). The current traveling right is zero until the signal arrives, and the moment the signal arrives, it becomes $I_{if}$, but the arrival and reflection occur simultaneously and the current becomes zero ($I_{if} = I_{ib}$, $I_{if} - I_{ib} = 0$). The voltage at the transmitting end is $V_0/2$ until the reflected wave arrives and becomes $V_0$ when the reflected wave does arrive. The current traveling right at the transmitting end is $I_{if}$ until the reflected wave arrives and zero after the reflected wave does arrive. Another reflection does not occur ($\Gamma_s = 0$).

5.1.3.3 Lumped Parameter Circuits and Distributed Parameter Circuits

Strictly speaking, all wires are transmission lines, and as shown in Fig. 5.8a, even when an inverter drives the next inverter stage inside an LSI, a steady state is reached after repeating such reflections within the wire. However, reflections are not observed because the wire is short and the period of reflection is short. Thus, as shown in Fig. 5.8b, there is no problem approximating this wire as a resistance and capacitance, and this is called a lumped parameter circuit. Meanwhile, as in Fig. 5.6, circuits with elements distributed throughout are called distributed parameter circuits. As a rule of thumb, when the wire length is less than $1/6$ of the wavelength, the circuit can be treated as a lumped parameter circuit, whereas if the wire length is greater than $1/6$, then the wire must be treated as a transmission line, which is a distributed parameter circuit. For example, with 10 GHz signals, the wavelength in vacuum is 3 cm, and $1/6$ of that is 5 mm. Thus, for LSI operating at 10 GHz, wires longer than 5 mm (50 cm if 100 MHz) must be treated as transmission lines.

![Fig. 5.8 Distributed and lumped parameter circuits](image-url)
5.1.3.4 50 Ω

50 Ω is most often used as the characteristic impedance. Some people say that this standard came about as a round number that is between 30 Ω that is easy to use from a power transfer perspective and 75 Ω which is easy to use from the signal loss perspective.

5.1.4 Termination Methods

As shown in Fig. 5.9, there are many methods for termination. For the following, the transmitting and receiving circuits are both CMOS inverters, and $Z_0 = 50$ Ω:

(a) This is the situation with no termination and is used when the signal line is short relative to the transmission rate, or in other words the wire can be treated as a lumped parameter circuit. The signal levels are at full swing between $V_{DD}$ and $GND$.

(b) This is called parallel termination and is the simplest form of termination. When the input impedance of the receiving circuit is infinite, the termination is a resistance of $R_T = Z_0$ (e.g., when the input of the receiving circuit is connected to the gate of a MOS, the gate leakage current is negligible, and the impedance of the gate capacitance is much greater than 50 Ω: $|1/j\omega C| \gg |Z_0|$). Inputs of measurement equipment such as oscilloscopes mostly employ this type of structure, and at the research and development level, this is used often from the compatibility with laboratory measurements. However, there are drawbacks, such as a large power consumption, dependency of the power consumption on the signal level H/L ratio (the power consumption is higher when the percentage of H is higher), and an imbalance in the sense that the L level goes all the way

![Fig. 5.9](image-url) (a) No termination, (b) parallel termination, (c) Thevenin termination, (d) series termination, (e) AC termination, (f) complementary parallel termination
down to $G_{ND}$, but the H level only goes up to $R_T V_{DD} / (R_o + R_T)$. Here, $R_o$ is the output impedance of the transmitting circuit.

(c) This is called the Thevenin termination and is designed so that $R_{T1} / R_{T2} = 50$. Also, $R_{T1}, R_{T2}, V_I$ can be adjusted according to the output impedance of the transmitting circuit to adjust the output signal level. In addition, the power consumption does not change while transmitting H or L. However, there are problems such as the increase in the number of elements for termination, the necessity of a $V_I$ voltage source, and a power consumption even when the output is floating.

(d) This is called the series termination, and $R_s$ is determined as $R_o + R_s = 50$. Here, the voltage at A is the instant after the signal output is $V_{DD}/2$. When this signal arrives at the receiving end, the signal reflects with reflectivity $\Gamma_L = 1$ (assuming the receiving end is open), so the voltage at the receiving end becomes $V_{DD}$. When the reflected voltage returns to the transmitting end, no further reflections occur and the signal is absorbed by the transmitting circuit because this end is terminated with 50Ω. This method has a low power consumption and is often used in 1:1 communication, but cannot be used in 1:N communication.

(e) This is called AC termination and is used for fast signal transmission where $1/joC_T \ll 1$. This has a low power consumption because there is no DC current flow, but for slower signals, $C_L$ will appear as a load capacitance which may slow down the signals. Also, this can only be used if the H and L are equally likely to occur, and there are no long continuous streams of 1’s or 0’s. In addition, there is an increase in cost and difficulty in implementation due to the need to separately use a $C_T$.

(f) This is called the complementary parallel termination. When the two lines always transmit a 0/1 or 1/0 complementary signal, then point B at the receiving end becomes a virtual ground and the voltage does not fluctuate. Therefore, when each transmission line is terminated by 50Ω to point B, the circuit becomes the parallel termination of (b), but because point B is virtual ground, it simply suffices to terminate between the two lines with a resistance of 100Ω. This is used widely in the transmission of complementary signals.

### 5.1.5 Voltage Levels

When transmitting signals, several voltage levels have been standardized, such as H:V$_{DD}$/L:GND or H:1.425V/L:1.075V. Here, things can get difficult if the transmitting side and receiving side use different processes and the supply voltages are different. For example, when a 65 nm 1.2 V chip and a 0.35 μm 3.3 V chip communicate with each other, the 65 nm chip must use a 3.3 V high-voltage transistor just for the IO. Some examples of the standards are low-voltage differential swing (LVDS), pseudo emitter-coupled logic (PECL), low-voltage PECL (LVPECL), and current mode logic (CML), and these voltage levels are summarized in Table 5.1. High-speed signal transmission standards are descendants of the previously popular
Table 5.1 IO voltage levels

<table>
<thead>
<tr>
<th></th>
<th>LVDS</th>
<th>PECL(5 V)</th>
<th>LVPECL(3.3 V)</th>
<th>CML</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX $V_H$</td>
<td>1.425 V</td>
<td>4.0 V</td>
<td>2.3 V</td>
<td>$V_{DD}$</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>TX $V_L$</td>
<td>1.075 V</td>
<td>3.2 V</td>
<td>1.6 V</td>
<td>$V_{DD} - 0.8$ V</td>
<td>$G_{ND}$</td>
</tr>
</tbody>
</table>

emitter-coupled logic (ECL: H levels at $-0.9$ V, L levels at $-1.7$ V) for bipolar transistors with supply voltages of $-5.2$ V, and PECL can be thought of as a replacement by CMOS.

5.2 ESD

We all have the experience of the shock when touching a doorknob while wearing a sweater during a dry winter. Here, it is said that a voltage of thousands of volts exists momentarily. This is called electrostatic discharge (ESD). What would happen if this discharge was not with a doorknob but with an LSI chip? Certainly, the chip would be destroyed.

5.2.1 ESD Models

For this ESD, there are several standard discharge models, as shown in Fig. 5.10.

(a) This is a model called the human body model (HBM) and is a model where a person with electrical charge touches a chip. The experiment is conducted by applying a voltage of several hundred to several thousand volts, with $C_D = 100$ pF and $R_D = 1.5$ kΩ. The high voltage is applied over a period of several ns.

(b) This model is called the machine model (MM) and is a model where a machine with electrical charge touches a chip. A charged $C_D = 200$ pF capacitor is brought into contact with the chip without a resistance. A voltage of 100~400 V is applied. The high voltage is applied across several ns.

(c) This model is called the charged-device model (CDM) and is a model where the chip with electrical charge touches a conductor and discharges. This can also be thought of as a variant of MM. A voltage of several hundred volts is applied, across several ns.
5.2 ESD

To prevent chip destruction due to ESD, it is a basic practice to use wrist bands connected to $G_{ND}$ so that ESD does not occur. However, ESD is something that occurs in unexpected situations, such as during chip bonding or transportation. Thus, it is necessary to embed ESD protection circuitry within the IO buffers, which are the points of contact between the chip and the outside world, so that the chip does not break even when ESD occurs.

As indicated in Fig. 5.11a, the gate oxide film of transistors $M_1$ and $M_2$ will be destroyed when ESD is applied. A representative ESD protection circuit is indicated...
in Fig. 5.11b. By allowing the injected ESD pulse to pass through the resistance $R_{e0}$, the voltage is reduced. At the same time, by allowing the charge to escape to $V_{DD}$ and $G_{ND}$ through diode-connected transistors $M_{e1}$ and $M_{e2}$, the application of a high voltage onto transistors $M_1$ and $M_2$ is prevented. That is, when a high positive voltage is applied, the gate and (originally) source terminals of $M_{e1}$ that are connected to $V_{DD}$ become a lower voltage relative to the PAD or (originally) drain terminal. Thus, $M_{e1}$ turns on, the ESD pulse flows to $V_{DD}$, and no load is applied to $M_1$ and $M_2$. Similarly, when a high negative voltage is applied, the gate and (originally) source terminals of $M_{e2}$ that are connected to $G_{ND}$ become a higher voltage relative to the PAD or (originally) drain terminal. Thus, $M_{e2}$ turns on, the ESD pulse flows to $G_{ND}$ (the current flows from $G_{ND}$ to PAD), and again no load is applied to $M_1$ and $M_2$. Here, resistances $R_{e1}$ and $R_{e2}$ are often inserted so that the ESD protection transistors $M_{e1}$ and $M_{e2}$ themselves do not break. As shown in Fig. 5.11c, c’, silicide protection for preventing the accumulation of low-resistance silicide is applied in the S/D regions of $M_{e1}$ and $M_{e2}$ to realize resistances $R_{e1}$ and $R_{e2}$. Well resistances without silicide and gate poly resistances without silicide are often used for resistances $R_{e0}$ and $R_{e3}$, as shown in Fig. 5.11d, e.

5.2.3 Miscellaneous Topics Regarding ESD Protection Circuitry

5.2.3.1 Input Buffers and Output Buffers

In general, gate oxide films are more susceptible to breaking than PN junctions. Therefore, as shown in Fig. 5.12a, b, input buffers break more easily than output buffers. However, when a termination resistance $R_t$ is used as in Fig. 5.12c, the transistor is less likely to break due to the ESD discharge flowing through $R_t$.

5.2.3.2 Speed Degradation

When resistances $R_{e0} \sim R_{e3}$ are inserted as in Fig. 5.11b, the transmission speed of IO buffers degrades. Sometimes only $M_{e1}$ and $M_{e2}$ are used without resistances as

![Fig. 5.12](image-url) (a) Output buffer, (b) input buffer, (c) input buffer with termination
5.3 Types of IO Buffers and Their Layout

![Fig. 5.13](image) (a) ESD discharge path for regular MOS, (b) ESD discharge path for SOI

the ESD protection circuit to prevent this degradation of transmission speed, but in this case, the ESD tolerance degrades. Also, while IO buffers themselves have load capacitances (the gate capacitances of $M_1$ and $M_2$ in Fig. 5.11b), the addition of ESD protection circuitry increases the load capacitance (drain capacitances of $M_{e1}$ and $M_{e2}$ in Fig. 5.11b) and invites further speed degradation. From the perspective of ESD protection, the gate widths $W$ of $M_{e1}$ and $M_{e2}$ should be as large as possible. However, this leads to speed degradation due to the increased capacitance. Therefore, there is a trade-off relationship between ESD tolerance and transmission speed. Care is especially needed with the input and output terminals of high-speed, small analog voltages such as the LNA input terminal in an RF circuit.

5.2.3.3 ESD Tolerance in SOI

Silicon on insulator (SOI) has a structure as shown in Fig. 5.13b and is used in ultrahigh-speed LSI. This is because relative to a regular MOS shown in Fig. 5.13a, the source and drain junction capacitances $C_{JS}$ are smaller and thus a low power consumption and fast operation are possible. However, the crystalline structure of the thin silicon layer on top of the buried oxide layer is problematic, and the gate oxide layer tends to break easily. Additionally, a large instantaneous current flows through the transistors for ESD protection ($M_{e1}$ and $M_{e2}$ of Fig. 5.11b). This current density is lower in regular CMOS because the ESD discharge disperses into the substrate, as indicated in Fig. 5.13a. However, the current density in SOI is higher because the path for ESD discharge is narrower as shown in Fig. 5.13b, and damage due to heat can occur. In this way, while SOI is a promising next-generation transistor structure, the lack of ESD tolerance is a weakness.

5.3 Types of IO Buffers and Their Layout

Examples of IO buffers include buffers for internal voltage supply, internal ground, IO supply, IO ground, bias voltages, low-speed digital signal outputs, low-speed digital signal inputs, high-speed digital signal outputs, high-speed digital signal inputs, analog signal outputs, and analog signal inputs. Also, termination resistances are embedded in the signal input and output buffers as necessary, along with ESD protection circuitry. As for the supply lines, various supply lines can be cross-connected with ESD protection circuitry in some cases.
5.3.1 IO Buffer Examples

Some representative examples of IO buffers are shown in Fig. 5.14.

(a) This is for the input and output of low-speed digital signals, where ESD protection circuitry is connected to CMOS inverters. The signals are full swing between $V_{DD}$ and $G_{ND}$ levels. The signals will reflect because there is no termination, and therefore these can only be used for low-speed transmission for which the signal integrity is not affected by the reflections that occur when the signal rises and falls. Also, while these are “low speed,” fairly large transistors are required to be able to drive the several pF of pad capacitance.

(b) This is for the input and output of low-speed digital signals. When the $Z$ terminal is pulled high (H), $M_{z1}$ and $M_{z2}$ both turn off, and the output becomes high impedance (High Z). There are three possible output states of high (H), low (L), and high impedance (High-Z), and therefore this is called a tristate buffer. When receiving signals from tristate buffers, a large resistance $R_{PD}$ is often placed in the input buffer to prevent instability of the internal states due to receiving a High-Z signal and the input becoming indeterminate. By doing so, when the input is High-Z, the input buffer will pull its own input down to the $G_{ND}$ level through $R_{PD}$. This resistance $R_{PD}$ is called the pull-down resistance. To make sure that the $V_{DD}$ level is reached when the signal is H, a resistance value significantly larger than the output impedance of the output buffer must be used for $R_{PD}$. Also, if this resistance is connected to the supply side, it becomes a pull-up resistance, and when the input is High-Z, the voltage is pulled up to $V_{DD}$.

(c) This is for the input and output of high-speed digital signals. ESD protection circuitry and a termination resistance $R_T$ are connected to CMOS inverters. A signal of H will not reach $V_{DD}$, and the voltage level will be determined by the resistive divider between $R_T$ and the on-resistance of $M_1$. A signal of L will go down all the way to $G_{ND}$, Multiple reflections can be prevented by making the on-resistances of $M_1$ and $M_2$ approach $Z_0$. A constant, steady-state current flows when outputting H.

(d) This is called open drain and is a different form for the input and output of high-speed digital signals. For a signal of H, $V_{DD}$ is reached by turning $M_2$ off. The level for a signal of L is determined by the resistive divider of $R_T$ and the on-resistance of $M_2$. Multiple reflections can be prevented by making the on-resistance of $M_2$ approach $Z_0$. A constant, steady-state current flows when outputting L.

(e) A typical example for the input and output of analog signals. By outputting with an NMOS source follower, the impedance seen from the internal pin $A$ is infinite (the gate capacitance of $M_2$). At the same time, the analog voltage can be output from the internal pin with an AC gain of 1 (0 dB). The usable voltage range depends on the value of $R_T$ and the size of $M_2$. Also, care is necessary when using this, because the characteristics change depending on whether the input pin $B$ is, for example, connected to a gate of a MOS transistor and thus
Fig. 5.14 Types of IO buffers: (a) low-speed digital; (b) tristate output and pull-down input; (c) high-speed digital; (d) high-speed digital, open drain; (e) analog, source follower; (f) bias voltage; (g) connecting various supplies to the same voltage
will not carry any current or is connected to the drain and there will be current flow.

(f) This is a buffer used for the input and output of bias voltages. DC current does not flow, and a voltage is assumed to be input and output. If DC current will flow, $R_{e0} \sim R_{e3}$ must be removed. In addition, the $R$ and $C$ can also be removed to input and output analog signals.

(g) This is used to supply the same voltage to the same chip for different means, for example, a 1.8 V supply for digital circuits and a 1.8 V supply for analog circuits. Bidirectional diodes are connected as a countermeasure against ESD, so that, for example, if a high voltage is applied to $V_{DD1}$, $M_{e3}$ and $M_{e4}$ turn on and charge can be released to $V_{DD2}$. Also, when different voltages are applied to the same chip, for example, a 3.3 V IO supply to $V_{DD1}$ and a 1.8 V internal circuit supply to $V_{DD2}$, $M_{e3}$ and $M_{e4}$ are removed and only the reverse-biased diode is used.

### 5.3.2 Supply Rings

In general, the supply for the internal circuits and the supply for IO are separated, because IO consumes a large current and generates noise. Pads are often laid out in the periphery of the chip, and it is common to give the pads their supply and ground by creating rings for IO supply and IO ground as shown in Fig. 5.15. While there exist various types of IO, they are easy to use when their layouts are the same size so that the IO supply, IO ground, and pads are correctly connected simply by replacing the cell. Of course, ESD protection circuitry and termination resistances are also included within the IO cell.

### 5.4 Determining Pin Placement

As mentioned in Sect. 5.1.2, IO on the chip are connected to the routing on the board through the pad, a bonding wire, and the package lead frame. When determining the pin placement, the electrical characteristics of these must also be taken into account.

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**Fig. 5.15** Supply ring
5.4 Determining Pin Placement

5.4.1 Supply Pin

In general, a low impedance is desirable for supply lines. To reduce the bonding wire resistance and contact resistance of the supply lines, multiple supply pins, rather than a single pin, are used. Here, to prevent the voltage from dropping due to the internal supply line resistance of the chip, it is desirable for all circuits to be equidistant from a supply pin. Therefore, it is good to place a second supply pin on the opposite side of the chip, as shown in Fig. 5.15.

The inductance of the supply lines is also problematic. As we know, inductance is determined by the area of the loop of current. Thus, rather than placing the chip \(V_{DD}\) and \(G_{ND}\) far apart as in Fig. 5.16(i), the inductance can be made smaller by placing them next to each other as in (ii). Also, when using multiple pins, rather than placing the pins as VVGG as in (iii), a placement of VGVG as in (iv) will make the inductance smaller.

5.4.2 Shielding

Let’s say \(S_0\) is a high-speed signal or a noise-sensitive analog signal, and cross-talk noise through parasitic capacitance could be injected by adjacently placed signal lines as in (v). Therefore, the signal should be placed between ground lines if possible as in (vi), to prevent cross-talk noise. Also, because the loop area of the signal and ground lines is reduced by doing this, not only will the inductance be reduced, but also the termination to ground will be more effective.

Fig. 5.16 Pin placement
5.4.3 Symmetry

The length of the bonding wires and lead frames differ from pad to pad, and thus not only do the signal transmission times from the package pin to the pad differ but also the voltage and current waveforms due to impedance mismatch. Therefore, for waveforms that change simultaneously, such as those of complementary signals, pins with symmetry in the package shape must be used, not as in (vii) but as in (viii).

Also, because the resistance and inductance of a bonding wire increase with the length, pins toward the middle of the chip with shorter bonding wires should be used for supply lines and important signals.

5.4.4 Assembly and Measurement

Pin placement also affects PCB board design. Things such as the routing of supply, ground, and signal lines on the board as well as the ease of assembly of external decoupling capacitances must also be considered. In addition, IO buffers should be selected with the characteristics of the measurement equipment and cables in mind, and the pin placement should be determined while considering the manageability of measurement.