

Keynote: Distributed Algorithms and VLSI

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Abstract. Shrinking feature sizes and increasing clock speeds are the most visible signs of the tremendous advances in VLSI (Very Large Scale Integration). Modern VLSI chips can no longer be viewed as monolithic blocks of synchronous hardware, where all state transitions occur simultaneously. Moreover, the reduced voltage swing needed for high clock speeds and low power consumption dramatically increases the adverse effects of particle hits, crosstalk and ground bouncing, and, hence, leads to much higher failure rates. As a consequence, modern VLSI devices have much in common with the loosely-coupled distributed systems that have been studied by the fault-tolerant distributed algorithms community for decades. This keynote will address ways of utilizing some of the existing research in the VLSI context, and identify new and challenging distributed computing research problems emanating from this important application domain.

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