

On Bit-Level Systolic Arrays for Least-Squares Digital Contour Smoothing

Ján Glasa

Institute of Informatics, Slovak Academy of Sciences,
Dúbravská cesta 9, 845 07 Bratislava, Slovak Republic
utrrglas@savba.sk

Abstract. In this paper bit-level systolic arrays for the least-squares digital contour smoothing are described. The smoothing is represented by linear operators defined by sparse circulant Toeplitz matrices with integer coefficients. A suitable decomposition of such matrices allows to analyze different bit-level pipelined strategies of the computation and to suggest corresponding bit-level systolic arrays which have a simple regular structure and achieve very high throughputs.

1 Introduction

Development of efficient techniques for the real-time analysis of digital arcs and curves plays an important role in image processing [2,7,8,16,18]. The methods for digital curves analysis can have a principal impact for analysis, representation and characterization of significant regions in digital images and for analysis of shapes of real objects, so that they belong to basic tools of commercial computer vision systems. Serious attention is paid to the introduction of new approaches and methods to improve the estimation accuracy of shape characteristics and invariants. The high speed computation, which is required in many concrete image processing applications [1,4,10,13,14,19], influences the development of VLSI systems utilizing parallelism, such as pipelined architectures, systolic arrays, string processors and wavefront arrays.

In this paper¹ we focus on efficient pipelined calculation of the constrained least-squares digital contour smoothing [15] which is based on the least-squares approximation to functions on equidistant subsets of points by orthogonal polynomials. Such a smoothing is represented by linear operators defined by circulant Toeplitz matrices with integer coefficients which can be efficiently realized. A suitable decomposition of these matrices allows to investigate different pipelined bit-level computation strategies and to suggest bit-level systolic arrays with a simple regular structure and very high throughputs.

In the following, let a digital picture be a finite rectangular array represented by a finite square grid Ω where a distance between neighbouring grid points of Ω is equal to 1.

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A subset of operators $\frac{1}{c}C$ defined by (1) are *feasible* [15], i.e., they fulfil the condition

$$|x_j - x'_j| < \frac{1}{2}, \quad |y_j - y'_j| < \frac{1}{2}, \tag{2}$$

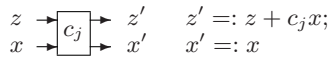
for all j , where x_j, y_j are elements of X and x'_j, y'_j are elements of X' . According to this definition, the feasible operator is defined by the constrained least-squares smoothing with the constraints (2) and it generates points which lie in the interior of the corridor $\bigcup_{j=0}^N \{(u, v) \in R^2 : |x_j - u| \leq \frac{1}{2}, |y_j - v| \leq \frac{1}{2}\}$. It has been shown that all operators on Fig. 1 are feasible [15]. The operator defined by polynomials of the third degree and by seven points allows to perform in some sense "maximal" feasible smoothing. These operators minimize the undersampling, digitizing and quantizing error and so they are able to improve the stability of calculation of invariants which correspond to invariants related to original pre-digitized contours investigated (for more details see [15,6]). Note that in this paper, the effect of noise by which digital images can be corrupted is not considered (it is assumed to be suppressed by a suitable pre-processing technique [3,9,11,12,17]).

2 Word-Level Pipelining of the Calculation

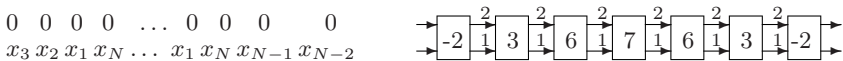
Let us consider the matrix C with coefficients $c_{-3} = c_3 = -2, c_{-2} = c_2 = 3, c_{-1} = c_1 = 6, c_0 = 7$ and let $c = 21$ (see Fig. 1c). The matrix-matrix multiplication CX can be represented by two circulant convolutions

$$cx'_i = \sum_{j=-3}^3 c_j x_{(i-j) \bmod N}, \quad cy'_i = \sum_{j=-3}^3 c_j y_{(i-j) \bmod N}, \tag{3}$$

$i = 0, 1, 2, \dots, N$. The word-level serial calculation as well as the word-level pipelining of (3) is straightforward.



(a)



(b)

Fig. 2. A word-level systolic array for the least-squares 7-point digital contour smoothing by polynomials of the third degree

A linear systolic array for parallel pipelined calculation of the first circulant convolution in (3) is shown on Fig. 2 (for more details see [15]). It has simple cells (Fig. 2a) separated by delay elements controlled by a common clock. The numbers of delay elements at z- and x-connections and the necessary input operations are shown on Fig. 2b. Since the primitive operations performed are operations on the word level, the array is qualified as a *word-level systolic array*. It has the throughputs $(N+13)T$, where T is the execution time of a single cell function.

3 Bit-Level Pipelining of the Calculation

The bit-level pipelining of the calculation of (1) is based on a suitable decomposition of the matrix C . Since the integer coefficients of the matrix C can be represented by sums of powers of 2, it is possible to find such decompositions of C by which the calculation of (1) can be represented by circulant convolutions in which neighbouring coefficients are represented by neighbouring powers of 2. It means that the corresponding multiplications can be carried out by shifting of the x-data.

More formally, the matrix C can be represented by a sum of n matrices $C^{(k)}$ with integer coefficients $c_j^{(k)}$,

$$C = \sum_{k=1}^n C^{(k)}, \quad c_j = \sum_{k=1}^n c_j^{(k)}, \quad (4)$$

which fulfil the following conditions:

- (i) Each non-zero coefficient $c_j^{(k)}$ has the form $c_j^{(k)} = 2^\alpha$, $\alpha \in Z_0^+$.
- (ii) For each couple of neighbouring non-zero coefficients $c_r^{(k)} = 2^\alpha$, $c_s^{(k)} = 2^\beta$, $r < s$ of the matrix $C^{(k)}$, it holds that $|\alpha - \beta| \leq 1$.
- (iii) For each two coefficients $c_p^{(k)} = 2^\alpha$, $c_q^{(k+1)} = 2^\beta$ of matrices $C^{(k)}$, $C^{(k+1)}$, where $c_p^{(k)}$ is the last non-zero coefficient from the set $\{c_j^{(k)}\}_{j=-3}^3$ and $c_q^{(k+1)}$ is the first non-zero coefficient from the set $\{c_j^{(k+1)}\}_{j=-3}^3$, it holds that $|\alpha - \beta| \leq 1$.

The decomposition (4) of the matrix C allows to represent the calculation of CX by two circulant convolutions, [6]

$$cx'_i = \sum_{k=1}^n \sum_{j=-3}^3 c_j^{(k)} x_{(i-j) \bmod N}, \quad cy'_i = \sum_{k=1}^n \sum_{j=-3}^3 c_j^{(k)} y_{(i-j) \bmod N}, \quad (5)$$

$i = 0, 1, \dots, N$. Each particular decomposition of C mentioned above represents a concrete bit-level pipelined systolic implementation strategy of the calculation of (5), in which the neighbouring coefficients are represented by the neighbouring powers of 2. This corresponds to shifting by just one position in the neighbouring

cells of the corresponding array. The procedure how to obtain a particular systolic array completely pipelined on a bit-level for the first circulant convolution in (5) can be summarized as follows (for more details see [15,6]).

The array consists of a sequence of n word-level systolic arrays which have a structure similar to the array shown on Fig. 2. The array cells correspond to the coefficients $c_j^{(k)}$, $j = -3, -2, \dots, 3$, $k = 1, 2, \dots, n$. The cells which correspond to zero coefficients $c_j^{(k)}$ are omitted modifying the numbers of used delay elements. In such a word-level systolic array, each word-level cell can be realized as a linear vertical systolic array of full adders (see Fig. 3a) separated by delay elements. To achieve a systolic array completely pipelined on a bit-level, a horizontal pipelining by delay elements is involved and the input data are scewed to provide the proper data alignment (the corresponding changes of the numbers of delay elements on z - and x -connections are also required, for more details see [15,6]). In the case of 8-bit input data, the intermediate results can be represented by $(8 + \lceil \log_2 21 \rceil + 1) = 14$ -bit numbers. The whole systolic array consists then of 2-dimensional regular matrix of full adders arranged into (at least) 12 columns

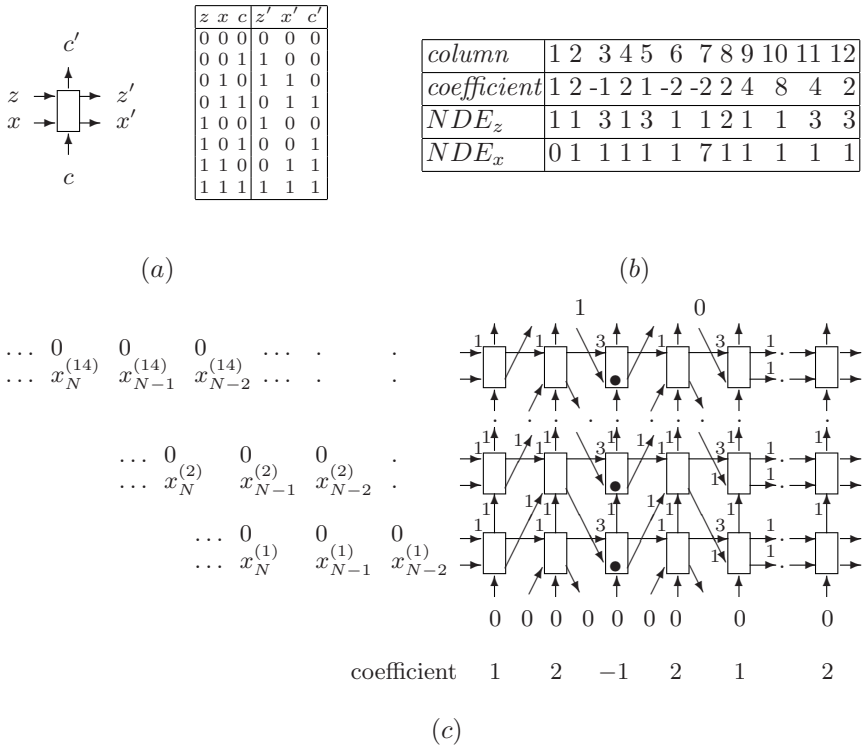


Fig. 3. A bit-level systolic array for the 7-point least-squares digital contour smoothing by polynomials of the third degree: NDE_* - number of delay elements on $*$ -connections

(corresponding to the non-zero coefficients of the matrices $C^{(k)}$) and 14 rows (corresponding to the bits of different significance) which are connected by delay elements. An example of such systolic arrays is shown on Fig. 3. The directions of z- and x-connections are constant for the whole array; the directions of x-connections are constant within one column and change from column to column. The shifting of x-data by just one bit position upwards, downwards, or horizontally, corresponds to the multiplication by 2^1 , 2^{-1} , or 2^0 , respectively. The multiplication by -1 is realized by converting the x-inputs into their 2's complements (inverters are denoted by small black circles, see Fig. 3b). The numbers of delay elements on x- and z-connections, constant within one column, change from column to column. The number of delay elements on c-connections is constant in the whole array. The clock period of such completely pipelined system is controlled by the delay t of a single full adder. Since the primitive operations performed are operations on the bit level, the array is qualified as a *bit-level systolic array*.

Table 1.

j	-3	-2	-1	0	1	2	3
c_j	-2	3	6	7	6	3	-2
$c_j^{(1)}$	0	2^0	2^1	-2^0	2^1	2^0	-2^1
$c_j^{(2)}$	-2^1	2^1	2^2	2^3	2^2	2^1	0

Table 2.

j	-3	-2	-1	0	1	2	3
c_j	-2	3	6	7	6	3	-2
$c_j^{(1)}$	-2^1	2^0	2^1	2^0	2^1	2^0	-2^1
$c_j^{(2)}$	0	2^1	2^2	2^1	2^2	2^1	0
$c_j^{(3)}$	0	0	0	2^2	0	0	0

The first bit-level systolic array for the calculation of (1) has been suggested in [15] (see Fig. 3). This array corresponds to the decomposition of C shown in Table 1. In this case, it holds that $n = 2$ and the number of non-zero coefficients $c_j^{(k)}$ equals to 12 (see Table 1).

Other different decompositions (4) have been used in [5] to achieve better throughputs (an example of such a decomposition is shown in Table 2). For these decompositions it holds that $n = 1$ and the corresponding bit-level systolic arrays have higher throughputs. In comparison with the array from [15], they have a little bit greater number of cells (one extra column of full adders), but in the same time there is a notable decrease of numbers of delay elements between array cells.

Finally, in [6] the complete analysis of all possible decompositions (4) of C has been performed to achieve the maximal throughputs of corresponding bit-level systolic arrays. In order to minimize also the required area of such arrays, the arrays with the minimum number of delay elements used (and with 12x14 cells) have been chosen. The complete set of bit-level systolic arrays for the calculation of (1) is shown on Fig. 4 [6]. The throughputs of these arrays is $(N+36)t$, where t is the delay of a single full adder and N is the number of points of digital contour.

<i>column</i>	1	2	3	4	5	6	7	8	9	10	11	12
<i>coefficient</i>	-1	2	1	-2	-1	2	4	2	4	8	4	-2
NDE_z	1	4	2	1	1	1	1	1	1	1	1	1
NDE_x	0	1	1	1	3	1	2	2	2	1	2	1
<i>coefficient</i>	-1	2	4	2	1	-2	-1	2	4	8	4	-2
NDE_z	1	1	2	3	2	1	1	1	1	1	1	1
NDE_x	0	1	1	1	1	1	3	1	4	1	2	1
<i>coefficient</i>	-1	2	4	2	-1	2	1	-2	4	8	4	-2
NDE_z	1	1	2	2	1	2	2	1	1	1	1	1
NDE_x	0	1	1	1	1	1	1	1	1	6	1	2
<i>coefficient</i>	-1	-2	1	2	-1	2	4	2	4	8	4	-2
NDE_z	1	5	1	1	1	1	1	1	1	1	1	1
NDE_x	0	1	1	2	2	1	2	2	2	1	2	1
<i>coefficient</i>	-1	2	4	-2	1	2	-1	2	4	8	4	-2
NDE_z	1	1	2	4	1	1	1	1	1	1	1	1
NDE_x	0	1	1	1	1	2	2	1	4	1	2	1
<i>coefficient</i>	-1	2	4	2	-1	-2	1	2	4	8	4	-2
NDE_z	1	1	2	2	1	3	1	1	1	1	1	1
NDE_x	0	1	1	1	1	1	1	2	5	1	2	1
<i>coefficient</i>	-1	2	-1	2	1	-2	4	2	4	8	4	-2
NDE_z	1	3	1	2	2	1	1	1	1	1	1	1
NDE_x	0	1	1	1	1	1	4	2	2	1	2	1
<i>coefficient</i>	-1	2	-1	-2	-1	-2	4	8	4	8	4	-2
NDE_z	1	1	3	1	3	1	1	1	1	1	1	1
NDE_x	0	1	1	1	1	1	3	3	2	1	2	1
<i>coefficient</i>	-1	2	-1	-2	-1	-2	4	8	4	8	4	-2
NDE_z	1	1	5	1	1	1	1	1	1	1	1	1
NDE_x	0	1	1	1	3	1	1	3	2	1	2	1
<i>coefficient</i>	-1	2	-1	-2	1	2	4	2	4	8	4	-2
NDE_z	1	3	1	3	1	1	1	1	1	1	1	1
NDE_x	0	1	1	1	1	2	3	2	2	1	2	1
<i>coefficient</i>	-1	2	-1	-2	-1	-2	4	8	4	8	4	-2
NDE_z	1	1	3	3	1	1	1	1	1	1	1	1
NDE_x	0	1	1	1	1	3	1	3	2	1	2	1

Fig. 4. Bit-level systolic arrays for the 7-point least-squares digital contour smoothing by polynomials of the third degree with the maximal throughputs in which the minimal number of the structural elements are used

4 Conclusion

In this paper different bit-level pipelined computation strategies for the real-time calculation of the constrained least-squares digital contour smoothing which represent different bit-level systolic arrays are summerized. They are based on

suitable decomposition of integer coefficients of the circulant Toeplitz matrix, by which the smoothing is represented. The suggested systolic arrays completely pipelined on the bit-level have simple regular structure and achieve very high throughputs. They can be implemented on single VLSI chips and can be used for the purposes of real-time digital contour analysis.

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