Chapter 7
3-Level Buck Converter Microelectronic Implementation

Abstract  This chapter covers the microelectronic design and implementation of the 3-level converter design obtained in Chap. 6. The implementation of such design not only requires the integration of the reactive components and the power switches and drivers, but also includes the additional circuitry required to obtain the appropriate DCM operation. Therefore, the first section covers the design of all the required control circuits (which in this work are called as the secondary control loop). These include the implementation of two different control loops to assure near ideal dead-time switching, as well as the turn-off of the NMOS switches at zero inductor current. Additionally, the building blocks to generate all the required switching signals are also exposed. For all the presented circuits, the corresponding layout design is provided. In the second section, details about the power components layout are explained. Finally, the third section presents transistor-level simulation results from the complete developed system (including the power converter itself and the required control circuits), as well as the general layout distribution.

7.1 Secondary Control Loop

The microelectronic implementation of the 3-level converter design determined in Chap. 6 is based on the implementation of two different parts. The most obvious is the converter itself (inductor and capacitors, as well as power switches and drivers), whereas the second one contains all the complementary circuits that control the converter behavior to approach the expected ideal operation, particularly its switching performance. All these complementary circuits are what, in this work, is called the secondary control loop, to distinguish it from the conventional control loop, that acts on the duty-cycle of the control switching signal in order to get the required performance from the converter, usually output regulation or tracking. This is, the main target of the secondary control loop is to approach the converter operation to its ideal switching behavior, which is assumed by the system-level control loop designer.

In this sense, three important issues must be addressed:

- All the switching signals generation, required for the 3-level converter operation. Because of the DCM operation and the use of synchronous rectification, different
switching signals for both power PMOS switches, as well as for both NMOS switches are required separately. Moreover, an additional signal is required to identify in which half of the whole switching period the converter state is (as will be explained afterwards).

- Because of the synchronous rectification scheme and the DCM operation, NMOS switches must be turned-off when the inductor current reaches 0. Thus, specific circuitry to detect this condition is required.
- In order to reduce the switching power losses, optimum dead-time should be applied between the PMOS turning-off and the NMOS turning-on. In the remaining transitions, no optimum dead-time is required because the DCM operation splits this action by means of the inactivity states ($T'_1$ and $T'_3$).

In Fig. 7.1, the ideal waveforms of the most representative signals corresponding to the 3-level converter are depicted. The secondary control loop should be in charge of achieving that ideal switching behavior. In the figure, some important delays, required in the $s_1$ and $s_2$ signals generation, are highlighted in gray. As explained afterwards, these delays are required for other parts of the circuitry to work.

Apart from these main functions, other interesting functionalities should be performed by the secondary control loop, such as to short-circuit the inductor during the inactivity states, to suppress inductor current and $x$-node voltage noisy oscillations due to the resonance between the inductor and $x$-node parasitic capacitances.

In Fig. 7.2, a block diagram is exposed that not only shows the building blocks corresponding to the secondary control loop, but also the signals that interact with the power plant.

As it can be observed, many signals between each block of the secondary control loop (in light gray in the figure) are required to achieve the desired functionality. Also, many signals are used to interact with the power plant. Although the details on the power plant implementation will be provided in the next section, in the following, a brief explanation list of the input and output signals of the power plant is provided:

- $V_o \rightarrow$ Converter output voltage.
- $V_x \rightarrow$ $x$-node switching voltage.
- $ndP_1, ndP_2 \rightarrow$ Input switching signals of the power drivers corresponding to $P_1$ and $P_2$ power switches.
- $dnN_1, dnN_2 \rightarrow$ Input switching signals of the power drivers corresponding to $N_1$ and $N_2$ power switches.
- $dP_1, dP_2, dN_1, dN_2 \rightarrow$ The four power MOSFET’s gate voltages.
- $V_A, V_B \rightarrow C_x$ capacitor terminals voltages.
- $CC_1, CC_2 \rightarrow$ Signals used to act on 2 NMOS transistors that short-circuit the converter inductor along the inactivity states.

Only 3 external signals are required in order to drive the whole system:

- $CLK \rightarrow$ An square signal used to determine the converter switching frequency. It must have double of the target switching frequency.
Fig. 7.1 Ideal waveforms of the most significative control signals of the 3-level converter, related to $v_x$ and $i_L$ signals

- $I_{\text{bias1}}$ → Input current used to generate the threshold voltage of an NMOS transistor in the $i_L = 0$ condition detection block. Its value should be around $10 \, \mu\text{A}$, although it is not a critical value.
- $I_{\text{bias, D}}$ → This current is used to determine the duty cycle of the PMOS switches control signal. In order to obtain $V_o = 1 \, \text{V}$, its value should be around $14 \, \mu\text{A}$.

In the following sections the functionality of each building block corresponding to the secondary control loop will be explained, and their schematics provided, as well as the corresponding transistor-level simulation results.
Fig. 7.2 Functional blocks scheme corresponding to the 3-level converter microelectronic implementation.
### 7.1.1 Variable Duty-Cycle Generation of the Switching Signal

The main function of this block is to generate an square signal at double of the needed switching frequency, and with variable duty-cycle, in order to establish the $T_1$ and $T_3$ states duration (this is, the PMOS power switches control signal). A single circuit working at double of the converter switching frequency is desirable to assure that the same duration for $T_1$ and $T_3$ states is obtained.

The functional scheme of its microelectronics implementation can be observed in Fig. 7.3.

![Fig. 7.3 Microelectronic implementation of the circuit that allows to adjust the duty-cycle of the PMOS power switches control signal](image)

The circuit operation is straightforward: the input $CLK$ signal is delayed and inverted by a chain of inverters (compressed in the figure as the single inverter $U1$), and the output of the $NAND$ gate is used to charge the $C$ capacitor to the battery voltage each period of the $CLK$ signal. Then, the capacitor is discharged by the current mirror composed by transistors $M1$ and $M2$, being the discharge current imposed by the $I_{bias\_D}$ input current. A chain of inverters (compressed in the single inverter $U3$) is used as a voltage comparator of the $VC$ signal, which allows to obtain an square output signal, at double of the switching frequency and variable duty-cycle ($D\_CLK$).

According to the previous explanation $I_{bias\_D}$ should be considered as the input control signal, which should provided by the primary control loop.

Figure 7.4 shows the most representative signals of the circuit operation, obtained from post-layout simulations (i.e. including all the parasitics from the layout design). The described functionality can be clearly observed. It is noted that the delay of the $U1$ chain of inverters is not critical, but it should just assure that there is enough time to fully charge the capacitor.

The variation of the $D\_CLK$ low-state duration has been studied as a function of the $I_{bias\_D}$ input current. Being the $C$ value of 21.6 fF, and the supply voltage of 3.6 V, a low-state duration of 191.5 ns was achieved for $I_{bias\_D} = 500$ nA, while 4.91 ns was obtained for an input current of 32 $\mu$A. The corresponding post-layout
simulation results can be observed in Fig. 7.5. The obtained span is considered to be appropriate for its application to the 3-level converter implementation, according to the characteristics exposed in Table 6.3.

Finally, the layout corresponding to this block can be observed in Fig. 7.6. Most important components such as the capacitor, the current mirror, the inverter used to cause the signal delay and the NAND gate, are highlighted by black rectangles.

### 7.1.2 \( P_1, P_2 \) and \( s \) Signals Generation

This circuit is designed to generate the switching signals corresponding to the PMOS power switches: \( P_1 \) and \( P_2 \) (which, as such, are active by low-level). Mainly, the input signal is \( D\_CLK \), which has double of the switching frequency and the desired duty-cycle. Thus, this block should toggle the \( D\_CLK \) pulses alternatively towards the \( P_1 \) or the \( P_2 \) corresponding power drivers. The respective inverted signals \( \overline{P_1} \) and \( \overline{P_2} \) are required too.
Fig. 7.5 Variation of the low-state duration of the output signal $D_{\_CLK}$ as a function of the $I_{\text{bias}_D}$ current (post-layout simulation results)

Fig. 7.6 Layout design corresponding to the $D_{\_CLK}$ generation block
In addition to this, the circuit must generate the $s$ signal which is a 50% duty-cycle square signal. Its frequency is the same as the switching frequency, and is used to distinguish between both halves of the switching period. This is, its value should be high during the $T_1$, $T_2$ and $T'_3$ states, and low during the $T_3$, $T_2$ and $T'_1$. Furthermore, its transitions should occur slightly later than those corresponding to the $P_1$ signal fall edges (as observed in Fig. 7.1), because it is required for other circuit blocks. The corresponding inverted signal $s_2$ is also generated in this block.

Figure 7.7 depicts the scheme corresponding to its microelectronic implementation. Regarding to the $s$ signal generation, the circuit is based on the action of two latches ($U_1$ and $U_2$) that are connected in a ring formation by means of the $U_3$ inverter. Since $U_1$ is enabled by high-level whereas $U_2$ is low-level enabled, the obtained functionality corresponds to a Toggle flip-flop activated by the falling-edge of the $D_{\text{CLK}}$ signal. The output of the $U_2$ latch is considered to be the $s$ signal, and $s_2$ is obtained from the output of $U_3$. The non-inverting buffers $U_4$ and $U_5$ are used to generate the desired delay on the $s$ and $s_2$ signals, as well as to buffer them since in the layout implementation long distribution lines for these signals will be required (as it will be shown afterwards). Hence, these buffers present and even number of tapered inverters.

The generation of $P_1$, $P_2$ and their inverted signals, is based in the same idea. However, NOR functions between the corresponding outputs of the Toggle flip-flop (composed by $U_7$, $U_8$, $U_9$, $U_{10}$), and the $D_{\text{CLK}}$ signal are required, since the low state duration from the later must be maintained when generating $P_1$ and $P_2$. In this case, inverters $U_{11}$, $U_{12}$, $U_{15}$ and $U_{16}$ are needed not only to invert the signals, but to buffer them.

In Fig. 7.8, post-layout simulation results are exposed. Not only the required signals generation is clearly observed, but also the required delay between the falling edges of $P_1$ and $P_2$, and the $s$ and $s_2$ signals changes.

To finalize, the layout design corresponding to this circuit block is exposed in Fig. 7.9 (in this case, top metal layers routing supply lines have been removed from the image for the sake of clarity). In the figure, the most important parts of the circuit have been highlighted in black boxes.

### 7.1.3 $dnN_1$ and $dnN_2$ Signals Generation

This block is intended to generate the switching signals that act upon the NMOS power switches gates (by means of their corresponding gate drivers), which finally are $dnN_1$ and $dnN_2$ (see Fig. 7.2). When implementing a DCM operated synchronous rectified 3-level converter, it is necessary to turn-off the NMOS power switches when the inductor current becomes zero, in order to prevent it to reverse, which would reduce the converter output voltage, and increase both switching and conduction losses. This is due to fact that a MOS transistor is a bidirectional switch which does not turn-off automatically as its current is reversed, like diodes do. Just to sum up, note that the duration of the $T_2$ state must be estimated by the circuit in order to turn-off the NMOS switch when $i_L = 0$. 
7.1 Secondary Control Loop

In fact, two equal blocks are used to generate independently both switching signals. Therefore, just one of the blocks will be described here, and just their input and output signals must be accordingly changed. Figure 7.10 shows the microelectronic implementation of this block. In this case, the presented block is the one used to generate $dnN_1$. 

Fig. 7.7 Microelectronic implementation of the circuit that generates de PMOS power switches gate signal, as well as the $s$ signal, which is used to identify which half of the switching period is currently on.
Fig. 7.8 Post-layout simulation results of the $P_1$, $P_2$ and $s$ generation block

The dashed grey box includes the core of the circuit. This simply makes use of input signals about the PMOS switches states and which half of the switching period is currently on to generate the $N_1$ signal (all of them obtained from the block described in Sect. 7.1.2), which is the base of the desired $dnN_1$.

Additionally, information is required to know when the inductor current becomes zero ($i_L = 0$) after a current pulse. Although many considerations on this subject will be provided in another section, here the corresponding part of the circuit will be explained. The main idea is to apply a bidirectional current on the capacitor $C$ to generate a voltage triangular shape that acts as an observer of $i_L$. Therefore, as soon as the voltage ramp goes back to zero (as the inductor current does), the $N_1$ transistor should be turned-off. Consequently, $M1$, $M2$, $M3$ and $M4$ transistors implement a bidirectional current source that outputs a current which is coarsely related to $v_x$ and $V_o$ voltages. Hence, a coarse observer of the inductor current is obtained.

If the $\alpha$-power model of the MOS transistor is used, the following derivation can be applied to this case.
7.1 Secondary Control Loop

NORs and buffer inverters

latches

buffers

Fig. 7.9 Layout design corresponding to the circuit that generates the $P_1$, $P_2$ and $s$ signals

Fig. 7.10 Microelectronic implementation of the circuit that generates the NMOS power transistor switching signal $dnN_1$
• The current injected by the saturated $M_1$ and $M_4$ transistors is called $I_1$ and $I_2$, respectively. Considering that both transistors are of the same type and size:

$$I_1 = k(V_x - V_{TN})^\alpha$$  \hspace{1cm} (7.1)

$$I_2 = k(V_o - V_{TN})^\alpha$$  \hspace{1cm} (7.2)

• Thus, the current applied on the capacitor along $T_1$ is $I_1 - I_2$, and $I_2$ during $T_2$.

• Considering a very high output impedance for the current source, two linear voltage ramps result from the current integration in the capacitor ($V_{ramp}$).

$$v_{T1}(t) = \frac{k(V_x - V_{TN})^\alpha - k(V_o - V_{TN})^\alpha}{C}$$  \hspace{1cm} (7.3)

$$v_{T2}(t) = \frac{-k(V_o - V_{TN})^\alpha}{C}$$  \hspace{1cm} (7.4)

• Since the voltage should return to its initial value at the end of $T_2$ (as $i_L$ does):

$$T_1 \frac{k(V_x - V_{TN})^\alpha - k(V_o - V_{TN})^\alpha}{C} = T_2 \frac{k(V_o - V_{TN})^\alpha}{C}$$  \hspace{1cm} (7.5)

And the inferred $T_2$ duration is:

$$T_2 = T_1 \frac{(V_x - V_{TN})^\alpha - (V_o - V_{TN})^\alpha}{(V_o - V_{TN})^\alpha}$$  \hspace{1cm} (7.6)

• Finally, if it is considered that for deep-submicron technologies the $\alpha$ value is no longer 2 but it becomes closer to 1, and low-$V_T$ transistors are used; it results that, very coarsely, the voltage ramp on the capacitor approaches the inductor current ramp (provided that low output ripple is considered), and the $T_2$ duration can be approximately determined:

$$T_2 = T_1 \frac{V_x - V_o}{V_o}$$  \hspace{1cm} (7.7)

The following step is to detect the zero crossing of $V_{ramp}$. In order to achieve that, the $U2$ inverter is used as a voltage comparator. This is a very compact and very fast (which is required in the present application) voltage comparison structure, together with the $M6$ transistor. Basically, the $M6$ short-circuits the input and output of the inverter during a pre-charge phase (here, it is periodically carried out any switching cycle, along the $T_1$ state). During the pre-charge phase, both inverter input and output reach the inverter threshold voltage (which implicitly becomes the voltage reference of the comparison). Thus, an increase of $V_{ramp}$ from that point sets the comparator output to low, and when $V_{ramp}$ decreases and crosses its initial value, the output of $U2$ becomes high. The inverter $U3$ is used just to sharpen the comparator output.

Figure 7.11 clearly shows the described functionality.
Fig. 7.11 Capacitor voltage ramp generation and voltage comparator operation

The \( M5 \) switch is just intended to window the current source application on the \( C \) capacitor along the \( T3, T2 \) and \( T1' \) states (see Fig. 7.1). As previously mentioned, the \( V_{ramp} \) voltage just acts as a coarse observer of the inductor current, precluding the precise turn-off of the NMOS power switches at the \( i_L = 0 \) moment. Inevitably, the \( T2 \) duration estimation must be adjusted to allow such an accurate action.

As it will be explained in another section of this chapter, it is proposed to sense some converter signals so as to observe whether the NMOS power switches are being turned-off at the \( i_L = 0 \) condition. This information is stored in the \( V_{fb1} \) voltage (for the case of the \( N1 \) power switch), which modifies the output current of a bidirectional current source composed by \( M10 \) and \( M11 \). As a consequence, the slope of \( V_{ramp} \) along the \( T2 \) state is accordingly modified to adjust the right \( T2 \) state duration. The purpose of \( U1 \) and \( M8 \) is to restrict this current adjustment to the \( T2 \) and \( T1' \) states.

Finally, the scheme of Fig. 7.10 shows that once the \( N1 \) signal is generated, it is applied to the starving inverter \( U8 \). The purpose for that is to adjust the delay of the falling edge of the signal sent to corresponding power driver (\( dnN1 \)). This delay adjustment depends on the \( V_{fb,BD1} \) voltage, and its purpose is to obtain ideal dead-times between the \( P1 \) turn-off and the \( N1 \) turn-on, in the \( T1 \to T2 \) transition. It must be observed that the \( dnN1 \) signal is inverted in respect to the \( N1 \) signal, because of the odd number of inverters of the corresponding power driver.

Figure 7.12 exposes the post-layout simulation results of the described circuitry. Although the input signals (\( P1, Vx \) and \( Vo \), in the figure) have been generated by means of ideal voltage sources, the expected functionality can be clearly observed in the most significative generated signals (\( U3 \) out, \( N1, dnN1 \) and \( V_{ramp} \)). In the simulation: \( V_{fb1} = 1.52 \) V and \( V_{fb,BD1} = 2 \) V.
Two particularities around the voltage comparator operation are observed:

- During the pre-charge phase, the comparator reference voltage causes the output of the $U_3$ inverter to go high; however, this does not affect the $N_1$ signal generation.

- The fast response expected from such implementation of a voltage comparator, which causes an input-to-output delay of just 945 ps.

In Fig. 7.13 the variation of the time at which $N_1$ signal goes low (this is, the $N_1$ power transistor turn-off action), can be observed as a function of the $V_{fb1}$ voltage. In this case a sweep of several $V_{fb1}$ values has been carried out.

To clearly show the dependence of the $T_2$ state duration modification as a function of the $V_{fb1}$ voltage, it is exposed in Fig. 7.14. The results have been obtained from the transient waveforms of Fig. 7.13: $T_2$ duration is approximated by the time from the $V_{ramp}$ voltage peak, until the falling edge of the $U_3$ output occurs. A wide range of values ($2.18 \text{ ns} \rightarrow 14.3 \text{ ns}$) with a 750 mV span is observed, and although the dependence becomes highly non-linear, it is monotonic.
7.1 Secondary Control Loop

Fig. 7.13 Transient simulation that shows the variation of the duty-cycle of the $dnN_1$ signal as a function of the $V_{fb1}$ voltage (post-layout simulation results).

Fig. 7.14 $T_2$ duration vs. $V_{fb1}$ voltage characteristic. The results are extracted from the transient simulation of Fig. 7.13.

Finally, Figs. 7.15 and 7.16 show the propagation delay between $N_1$ and $dnN_1$ signals due to the $M7$ starving transistor gate voltage $V_{fb_{BD1}}$. Figure 7.15 presents the transient waveforms of both signals, while Fig. 7.16 depicts the delay characteristic as a function of the $V_{fb_{BD1}}$ voltage. In the later one, it is observed the increase of the delay sensibility as the $V_{fb_{BD1}}$ voltage increases close to the $V_{dd} - V_{TP}$ voltage, which results in $M7$ transistor turn-off. Below the $V_{fb_{BD1}} = 2.5$ V limit.
Fig. 7.15 Transient simulation that shows the variation of the delay between $N_1$ and $dn N_1$ signals as a function of the $V_{fb\_BD}$ voltage (post-layout simulation results).

Fig. 7.16 Delay vs. $V_{fb\_BD}$ voltage characteristic. The results are extracted from the transient simulation of Fig. 7.15.

(not shown in the figure), the delay is almost no further reduced since $M7$ supplies current enough to not affect the propagation delay.

The developed layout corresponding to this circuit block can be observed in Fig. 7.17, where the dimensions are noted and the most significative components are highlighted by means of black boxes.
Although in this section the details on the $dn N_1$ signal generation circuit have been provided, an identic block is used to generate the $dn N_2$ signal and just the input and output signals are accordingly changed. In Fig. 7.18 the right connection scheme is provided.

**Fig. 7.17** Layout design corresponding to the circuit that generates the $dn N_1$ signal

**Fig. 7.18** Microelectronic implementation of the circuit that generates the NMOS power transistor switching signal $dn N_2$
7.1.4 $i_L = 0$ Condition Feedback Loop

In the previous section the circuit-level generation of the signals that cut off the NMOS power switches at the end of the $T_2$ state has been presented. In both Figs. 7.10 and 7.18, a voltage-controlled current source is used to modify the duration of the $T_2$ state, in order to accurately cut off the corresponding NMOS transistor at the time instant at which the inductor current is zero.

Nevertheless, here the main issue is to determine the appropriate value of the $V_{fb1}$ and $V_{fb2}$ voltages. In other words, it is necessary to detect the $i_L = 0$ condition, and if the system is doing it right or not.

In case of an implementation similar to the proposed in the previous section, a manual adjustment of the $V_{fb1}$ and $V_{fb2}$ voltages would do the job, however this presents the obvious disadvantage of having to adjust any different chip, because of the component tolerances. Furthermore, even in case of the same physical implementation, the $T_2$ state duration might change for different application parameters.

Thus, some kind of automatic detection of the $i_L = 0$ condition is required. Different approaches can be used to implement this, based on the direct or indirect detection of that condition:

1. The most obvious proposal is to sense the inductor current by means of a magnetic field sensor, because of the proportional relationship between the inductor current and the generated magnetic field that stores the inductor energy. The main drawback of this solution is that, in a fully integrated environment, it is difficult to implement a magnetic field sensor (specially in standard CMOS processes).
2. Another more feasible way to sense the inductor current is by the series connection with the inductor of a low value resistor. This produces a voltage drop across the resistor proportional to the inductor current, that could be sensed by a differential amplifier. The main drawback of this sensing method are the joule-effect power losses across the resistor, which can not be extremely low because its voltage must be sensed.
3. A similar approach to the previous one is based on the use of the parasitic on-resistor of the NMOS power switch, to sense the voltage across it ($v_{ds}$) [105]. Two main advantages appear with this approach: no additional resistance is added to the inductor current path (which avoids to increase the power losses); and voltage sensing becomes easier, since the source of the NMOS transistor is directly connected to ground. However, the value of the parasitic on-resistance of the NMOS power switch is more difficult to estimate.
4. More complex $i_L = 0$ detection systems require the implementation of some kind of observer, in order to reproduce the inductor current waveform without adding additional resistance to the current path, but with a more accurately determined resistor value [25, 29]. Their main drawback is the requirements of the needed voltage amplifier, in terms of bandwidth, offset and gain.

All these current sensing methods are somehow based on the inductor current waveform reproduction, which may become very interesting when implementing
some kinds of primary control strategies. However, all of them share two important implementation limitations:

- An important source of error in the aforementioned current sensing methods is the delay between the time at which $i_L$ reaches the zero value, and the NMOS power transistor is switched-off. This is, even when the current waveform is reproduced without any delay, a comparator (with a non-zero input-to-output delay, $t_{d_{\text{comp}}}$) is needed to act the corresponding driver, which additionally presents its own propagation delay ($t_d$).

The error committed in this action can be straightforward calculated:

$$\text{Error}_{i_L} = \frac{V_o}{L} (t_d + t_{d_{\text{comp}}}) \quad (7.8)$$

According to the characteristics of the design selected in the Sect. 6.3: $V_o = 1$V, $L = 26.73$ nH, $t_d = 0.79$ ns (the $N_2$ power switch) and supposing $t_{d_{\text{comp}}} = 1$ ns. This results in an error of 67 mA (supposing and offset-free amplifier-comparator combination), which is about 32% of the maximum inductor current.

Thus, it is observed that stringent specifications for the corresponding micro-electronic designs are required. The effect of the propagation delay on the error committed in the $i_L = 0$ condition detection can be clearly observed in Fig. 7.19a.

- Another source of error in the $i_L = 0$ detection in the methods that sense the current through a resistor (may it be explicitly added, or from the power switch) is the equivalent input offset voltage ($V_{\text{offset}}$) of the voltage comparator (and the eventually needed amplifier). Due to the desirable low value resistors ($R_s$) used here, low voltage drops are expected in the current sensing resistor, which might be in the order of the input offset of the voltage comparator. Then, the resulting error committed when attempting to detect the $i_L = 0$ condition can be evaluated as follows:

$$\text{Error}_{i_L} = \frac{V_{\text{offset}}}{R_s} \quad (7.9)$$

If $R_s = 0.31$ $\Omega$ (from the $N_1$ power switch), and $V_{\text{offset}} = 10$ mV (which is a reasonable value if a high speed comparator is designed), then the resulting error in the $i_L = 0$ detection would be of 32.3 mA. Again, this value is considerably high when compared with the expected maximum inductor current. Figure 7.19b conceptually shows this error source.

For all these reasons, in this work, a different method to adjust the $T_2$ state duration, so as to switch off the corresponding NMOS power transistor when the inductor current reaches 0, is proposed.

The method is based on the $x$-node voltage observation, since this voltage presents two clearly different behaviors depending on the inductor current sense at the time instant of the power NMOS switch-off.
**Fig. 7.19** Error mechanisms in the $i_L = 0$ condition detection, by means of current sensing and comparison: *a* due to the propagation delay through the voltage comparator and the power driver; *b* due to the input offset voltage of the comparator.

*If $i_L > 0$ → If the NMOS power transistor is switched off before the inductor current reaches the zero value, the inductor current discharges all the parasitic capacitances connected at the $x$-node, and hence the $v_x$ voltage continues decreasing until the parasitic body-diode (from the body-source PN junction) is turned-on and the inductor current passes through it. With the $v_x$ reduction, the decreasing slope of the inductor current becomes faster. When the inductor current becomes zero, the parasitic diode is turned-off and the inductor would start to resonate with the $x$-node parasitic capacitor (this is an issue that will be treated in another section). The expected behavior can be observed in Fig. 7.20a.*
1.- The NMOS is switch-off before $i_L = 0$

2.- A positive voltage pulse appears in $v_x$

**Fig. 7.20 a** The body diode of the NMOS power switch turns-on as a consequence of a premature cut off of the power transistor ($i_L > 0$). b The inductor current charges the $x$-node parasitic capacitor and a positive voltage pulse appears in $v_x$ voltage, as a consequence of a late cut off of the power transistor ($i_L < 0$)
As observed in the figure, a negative pulse in the $v_x$ voltage appears at the end of the $T_2$ state provided that the power transistor is cut off before the inductor current becomes zero. The peak value of the negative voltage pulse is approximately the forward voltage of the parasitic body diode.

**i_L < 0 →** In case of switching off the power transistor too late (when the inductor current sense has been reversed), the x-node parasitic capacitor is charged and a positive voltage pulse appears in $v_x$, whose value is greater than the $V_o$ voltage. Once again, this is the consequence of the resonance between the inductor and the parasitic capacitor. Figure 7.20b clarifies this behavior.

The magnitude of the positive pulse is always higher than the $V_o$ voltage, and depends on the Error $i_L$ value (among other parameters).

Therefore, two different events can be observed in the x-node voltage depending on a premature or late switching-off action of the NMOS power transistor, that if properly processed can be used to adjust the voltage that controls the current source of the circuits of Figs. 7.10 and 7.18. In fact, just one event can be clearly identified, since the x-node resonance is expected to appear in any case (because of the x-node resonance) but, as it will be explained later, it is enough to develop the proposed adjustment system.

The main consequence of the previous discussion is that the proposed method avoids to directly detect exactly the moment at which $i_L = 0$ is zero. Instead of that, it is easier to detect whether the system operation is appropriate or not, and to determine the sense of the required correction on the adjustment voltages ($V_{fb1}$ and $V_{fb2}$).

Consequently, a circuit has been developed to recursively adjust both $V_{fb1}$ and $V_{fb2}$ voltages. This must be carried out independently for any voltage, since many different parameters may impact on the exact time instant when $i_L = 0$. This is, the parasitic transistor resistance, the power driver designs, the voltage supply of the power drivers, the different kinds of transistor used to implement $N_1$ and $N_2$, and many others determine the exact duration of $T_2$ at each half of the switching period.

The main concept that relies under the design is to detect if any of the aforementioned events occur along the switching cycle, and then, a certain amount of charge is injected or discharged to a capacitor that holds the corresponding $V_{fb}$ voltage (as an analog memory cell). This is easily done by means of the parallel connection of this capacitor ($C_{fb}$), and two different smaller capacitors which are pre-charged to ground or to the supply voltage. Hence, the voltage of the $C_{fb}$ capacitor is modified by discrete increments (positive or negative) any time that one of both observed events appear in the $v_x$ voltage.

This functionality is depicted in the Fig. 7.21. The signals $H_1$ and $H_2$ can take binary values to indicate whether one of the events took place at the end of the last $T_2$ state. Although it has been particularized for the $V_{fb1}$ voltage, an identical counterpart should exist to modify $V_{fb2}$.

In order to properly correct the $T_2$ state duration, if the NMOS is cut off when the inductor current is still positive ($H_1 = 1$), then the $C_{A1}$ capacitor (pre-charged to the ground voltage) is parallel connected to the $C_{fb1}$, so as to decrease its voltage,
Fig. 7.21 Conceptual functionality of the circuit that controls the $V_{fb1}$ voltage

which finally increases the $T_2$ duration. On the other hand, if the inductor current is already negative ($H_2 = 1$) when the NMOS transistor is switched off, the circuit operates to increase the $V_{fb1}$ voltage to decrease the $T_2$ duration.

The detection of both different events has a time discrete binary quantification: they just may occur or not along any switching cycle. As a consequence, the dynamics of such a feedback control loop, depends of the gain between the $V_{fb1}$ and the $T_2$ duration modification (which is non-linear, as observed from the circuit of Sect. 7.1.3), and the relationship of the 3 capacitors of Fig. 7.21. Expression 7.10 determines the evolution of the $V_{fb1}$ voltage for any switching period.

$$V_{fb1}(n + 1) = \frac{C_A Gnd H_1 + C_{fb1} V_{fb1}(n) + C_B V_{bat} H_2}{C_A H_1 + C_{fb1} + C_B H_2}$$  (7.10)

When designing the capacitors values, several considerations should be taken into account:

- First of all, the $C_A1$ capacitor should be larger than $C_B1$ since the positive pulse on the $v_x$ voltage is expected to occur almost for at any switching period (due to the inductor resonance). On the contrary, it is sure that negative pulses will only appear if $i_L > 0$.
- The relationship between the $C_A1$ and $C_B1$ capacitors determines the minimum voltage attainable by the $C_{fb1}$ capacitor (7.11).

$$V_{fb1_{min}} = \frac{V_{bat} C_{B1}}{C_A1 + C_{B1}}$$  (7.11)

- The larger the $C_A1$ and $C_B1$ capacitors (in front of $C_{fb1}$), the faster the loop response. Unfortunately, the steady state will be established in a periodic behavior surrounding the optimum value, resulting in suboptimum transistor switchings.
Additionally, the dynamics is also affected by the relationship between $C_{A1}$ and $C_{B1}$, since both events may occur at the same switching period.

- The $C_{fb1}$ capacitor is connected to the voltage supply ($V_{bat}$) rather than the ground, because this assures the NMOS transistor commutation (although sub-optimal), at the startup of the circuit.

In Fig. 7.22, several MATLAB simulations showing the $V_{fb1}$ evolution for different values of the capacitors are presented. Since the simulation does not take into

![Figure 7.22](image-url)

**Fig. 7.22** $V_{fb}$ evolution for 3 different sets of capacitors values, being the initial voltage 1.8 V: 
- The target voltage is $V_{iL}=0 = 1$ V; 
- The target voltage is $V_{iL}=0 = 2.5$ V
account any switching converter, an arbitrary voltage value has been set \((V_{iL=0} = 1\ \text{V}\) and \(V_{iL=0} = 2.5\ \text{V}\)) to establish whether the \(i_L\) value at the switching moment is positive or negative.

From the results of Fig. 7.22 the values for each capacitor were selected: \(C_{fb} = 5\ \text{pF}\), \(C_A = 200\ \text{fF}\) and \(C_B = 50\ \text{fF}\).

To detect both expected events at the end of the \(T_2\) state, a single MOS transistor is used as a voltage comparator. From its static \(I_{ds} = f(V_{gs})\) characteristic, any MOS transistor can be used as a voltage comparator, current \(I_{ds}\) is zero or not, depending on whether the gate-to-source voltage is below or above than the threshold \(V_T\). Thus, the input voltage is the \(V_{gs}\) difference, while the implicit voltage reference is its threshold. This approach yields a very fast and compact voltage comparator, even though the voltage threshold is not easily determined. Fortunately, in the proposed application this is not critical, since the negative pulses to detect are expected to present a peak value equal to the forward bias voltage of a PN diode (which should be higher than \(V_T\), specially for low-\(V_T\) transistors). In case of a positive overshot, it is also expected to be greater than \(V_o + V_T\). Additionally, the threshold voltage can be pre-compensated in order to drop the voltage reference down to zero.

Based on all these operating concepts, the finally developed circuit is depicted in Fig. 7.23. It is observed that some parts of the circuit are replicated for every adjustment voltage control.

Transistor \(M4\) is used to detect the negative pulses in \(v_x\) due to a premature power transistor cut-off, and its threshold voltage is pre-compensated by the \(M2\), \(M3\) and \(M5\) current mirrors. \(M1\) is in charge to restore the drain of \(M4\) to the supply voltage at any switching period, to allow the detection of the corresponding event, since the drain of \(M4\) goes low when a negative pulse is detected. Signals \(A1\) and \(A2\) are used to window the events detection by means of controlling the voltage supply of \(U4\) and \(U6\) inverters, which in turn control the connection of capacitors \(C_{A1}\) and \(C_{A2}\) to \(C_{fb1}\) and \(C_{fb2}\).

Regarding the detection of positive pulses, a similar circuitry is used. \(M13\) acts as a voltage comparator between \(v_x\) and \(V_o + V_{TP}\), and \(M14\) is used to discharge its drain node down to ground, to allow a subsequent detection. Then, the pulse detection is windowed by the signals \(A1\) and \(A2\), and \(U9\) and \(U11\) inverters, which control the connection of capacitors \(C_{B1}\) and \(C_{B2}\).

The pre-charge of \(C_{A1}, C_{A2}, C_{B1}\) and \(C_{B2}\), is carried out by the corresponding \(P1\) and \(P2\) signals (and their inverted counterparts), along the \(T1\) and the \(T3\) states.

In Fig. 7.24, transistor-level simulation results are presented: the proposed circuit is applied to the designed 3-level converter. As it can be observed, the circuits independently adjust the \(V_{fb1}\) and \(V_{fb2}\) voltages, to reduce the error committed in the \(T_2\) duration estimation. In this case, the initial value of both feedback voltages was set to half the input battery (1.8 V). The same periodic behavior around the optimum value observed in the MATLAB simulations also appears here, resulting in a certain error in the \(T_2\) duration estimation.

In Figs. 7.25a and 7.25b, details on the \(v_x\) voltage and the inductor current are provided, namely at the beginning and at the end of the feedback loop adjustment.
As observed in the details in Figs. 7.25b, the $T_2$ duration has been corrected until the current values (at the switching-off moment) of 6.6 and 8.6 mA for the $dN_1$ and $dN_2$ signals, respectively. In contrast, at the beginning of the simulation where the correction voltages ($V_{fb1}$ and $V_{fb2}$) have not been adjusted, the inductor current values at the time instant of switching-off the NMOS transistors are 37 and 47 mA, respectively. Therefore, the feedback loop is able to compensate many of the unknown parameters that may impact on the exact $T_2$ state duration, such as the power drivers propagation delay ($t_d$), the exact inductor value, the parasitic resistances in the inductor current path, etc...
The precision on the final results could be increased by reducing the values of $C_{A1}$, $C_{A2}$, $C_{B1}$ and $C_{B2}$ capacitors to reduce the voltage steps on the $V_{fb1}$ and $V_{fb2}$ voltages. Unfortunately, this would also increase the setting time of the feedback loop.
In Fig. 7.26 the designed layout for this circuit block is presented. The capacitors used to modify the correction voltages are highlighted by black boxes, although the much larger \( C_{fb1} \) and \( C_{fb2} \) capacitors have not been included to allow a better observability of the layout view. The largest element that is observed in the figure is the \( M_6 \) transistor used as a MOS capacitor to filter the switching noise introduced in the \( M_4 \) gate. Also both transistors used as a voltage comparators (\( M_4 \) and \( M_{13} \)) have been marked with black arrows.

### 7.1.5 Dead-Time (\( t_{BD} \)) Adjustment Feedback Loop

This functional block is intended to avoid the body-diode conduction as well as the current shot-through.

The body-diode conduction is due to an excessive dead-time between the power PMOS switching-off, and the corresponding NMOS switching-on actions. During this transition, the inductor current has its maximum value and the simultaneous off-state of both power switches forces the inductor current to discharge the \( x \)-node parasitic capacitor until the parasitic body-diode of the NMOS power transistor is forward biased and conducts the inductor current. Obviously, this increases the power losses in front of the synchronous rectification operation expected from the NMOS power switch.

On the other hand, a too short dead-time (or even negative) may result in current shot-through. Mainly, this is due to the simultaneous conduction of both power switches which causes a short-circuit of the input battery or the \( C_x \) capacitor (in the 3-level converter case). Once again, this can dramatically reduce the power efficiency, and even damage the input battery.
Consequently, an ideal operation requires to adjust the dead-time so as to separate the PMOS switching-off and the NMOS switching-on actions, just the precise time to allow the inductor current to discharge the x-node parasitic capacitor until its voltage equals the voltage-drop due to the on-resistance of the NMOS power transistor, thereby producing a zero-voltage-switching (which minimizes the switching losses).

Figure 7.27 depicts these 3 situations.

\[ \text{Body-diode conduction} \]

\[ \text{Shot-through} \]

\[ \text{Ideal dead-time} \]

Fig. 7.27  Body-diode conduction and shot-through lossy mechanisms in front of the ideal dead-time operation

Such functionality is particularly challenging when miniaturization and on-chip integration is pursued and hence switching DC-DC converters operating in the range of tens of MHz are targeted. Optimum utilization of a synchronous rectifier depends on dead-time selection. Optimum dead-times depend on circuit parameters, process/temperature variations, and operating conditions, and therefore the impact upon efficiency is greater at higher switching frequencies.

Past approaches for adjusting dead-time encompass the straightforward use of fixed dead-times (usually implemented via nonoverlapping clock schemes), in which case their values have to be conservative to be robust in front of process variations and hence dead-times are often far from optimum with notable efficiency penalties. Ideal diode emulation [112] might be a solution for very low switching frequencies but impractical for miniaturized converters.

Interesting works implementing dead-time optimization systems can be pointed out here. In [94] Stratakos et al. propose an adaptive control scheme, however an snubber capacitor is used to slow-down the fall and rise times of the x-node voltage transitions (which may increase the global switching losses). In [113] a control loop is implemented to dynamically adjust the dead-time, but it is supposed that the power transistors are switch-on when their $V_{gs}$ voltage is higher than their voltage threshold. Unfortunately, in deep-submicron technologies the threshold between the on and off states of a power transistor is not clearly established.
Other proposals include DLL-based approaches [114, 115], predictive gate drives [116] and efficiency optimization [117, 118], which require switch or input/output voltage and current sensing, and require specialized drivers. A recent different approach [119] is based on the fact that both for too-long or too-short dead-time the duty cycle increases to compensate the loss. For optimum dead-times, no body diode conduction occurs and the duty-cycle command has minimum value, provided that the output is regulated. A digital controller implementation enables sensorless dead-time optimization approach by an optimization performed by searching for the dead-times that minimize the duty cycle command.

In case of DCM operation in classical buck and 3-level converters, this phenomena appears just in the $T_{on} \rightarrow T_{off}$ states transition (which for the 3-level converter becomes the $T_1 \rightarrow T_2$ and $T_3 \rightarrow T_2$ transitions), since the opposite transition is split and separated by the inactivity state.

In this work, it is proposed to apply a feedback loop to dynamically adjust the dead-time to achieve the ideal operation. Inevitably, the dead-time ($t_{BD}$) adjustment is based on a variable propagation delay of the PMOS and NMOS power transistors gate signals. Since only $T_1 \rightarrow T_2$ and $T_3 \rightarrow T_2$ state transitions need this correction, just the rising edges of these four signals ($dN_1$, $dN_2$, $dP_1$ and $dP_2$) need to be delayed (or advanced). In order to achieve this functionality, starved inverters are used in all of the signals generation circuits. In case of the driving signals generation for the $N_1$ and $N_2$ power transistors, the starved inverters were included in the circuits presented in Sect. 7.1.3, whereas those corresponding to the $P_1$ and $P_2$ transistors are included in the present section.

The voltages applied to the gates of the starving transistors are also adjusted depending on the detection of the body-diode conduction or the shot-through events. Because of its similarity, the body-diode conduction is detected by a very similar circuit as the used in Sect. 7.1.4 to detect the negative pulses in $v_x$.

Unfortunately, the detection of the shot-through event is much less straightforward. To detect just a negative dead-time (this is, that the NMOS gate voltage goes high before the PMOS gate voltage) is not enough, since even a small positive dead-time could result in the simultaneous conduction of both power transistors, due to non-instantaneous gate voltages transitions and the different voltage levels that switch-on or switch-off the power transistors (see Fig. 7.28).

![Fig. 7.28 Body-diode conduction even in case of a small positive dead-time (this is, that the PMOS gate voltage goes high before the NMOS gate voltage)](image-url)
The only magnitude which really identifies the presence of the shot-through event due to the simultaneous conduction of both power switches is the current spike produced by the short-circuit. Although this idea holds for a 3-level converter, it is easier to understand it in case of a classical Buck converter.

According to the ideal operation above described, no current should flow between both power transistors. Thus, just in case of a shot-through conduction a current spike flows between them. As a result, this is the magnitude to be sensed to detect this kind of event.

Unfortunately, this spike could last for tens of picoseconds, and even worse, it is not desirable to add any component to that part of the power plant, in order to avoid increasing conduction or switching losses.

Consequently, in this work it is proposed to create an observer of such situation and sense the current spike by means of a series connected capacitor. In this perspective, two smaller transistors are used to emulate the power transistors. Obviously, although their corresponding channel width is much smaller, they are of the same kind, present the same length, are supplied from the same nodes and are actuated by the same gate power drivers. In fact, in the layout design, if possible, they could be placed as one of the fingers of the power transistors, to reduce possible mismatching issues. The proposed basic idea is exposed in Fig. 7.29.

This circuit corresponds to the shot-through detection for the case of the $P_2-N_2$ transistors pair (note the voltage supply $V_A-V_B$ from the $C_X$ capacitor terminals), which might happen in the $T_3 \rightarrow T_2$ states transition. However, the corresponding counterpart for the $P_1-N_1$ pair can be straightforwardly derived.

Transistors $M_1$ and $M_5$ are scaled versions of both power MOSFETs, since no high power must be driven and their gates are driven by the corresponding power drivers outputs ($dP_2$ and $dN_2$), which are not expected to drive much additional capacitive load. The capacitor $CBD_2$ is used to sense and storage the eventual current spikes flowing from $M_1$ to $M_5$. The purpose of $M_3$ is to short-circuit the capacitor along the whole $T_3$ state (connecting both terminals to $V_A$), to allow the detection of a new subsequent event. $M_2$ and $M_4$ act as an inverter that should detect the voltage state of the $V_{s1}$ node (this is the reason to share the same voltage supply), and the size of both transistors must be designed to properly set the corresponding thresh-
old voltage. Finally, the $U1$ inverter should reconstruct the output of the previous inverter.

Hence, before the states transition, the $V_{s1}$ sensing node is connected to the voltage supply $V_A$. After that, if no current spike is produced $V_{s1}$ goes down to $V_B$. However, if the shot-through event takes place along the states transition due to simultaneous conduction, a current spike flows through both transistors and the capacitor, which stores the corresponding charge and acquires a certain voltage level depending on the strength of the shot-through event. Thus, the $V_{s1}$ node is not equal to ground after the transition, which can be sensed by the following inverters. In other words, if the shot-through event takes place the output of $U1$ is high along the $T_2$ state, whereas it is low if the considered event does not happen.

According to the previous explanation, the lower the capacitor value, the higher the voltage achieved, and the easier to sense it. Unfortunately, the charge injection due to the clock-feedthrough issue across the parasitic capacitors and the gate voltage changes of $M1$ and $M5$, is also stored in the capacitor. Thus, a rather complex trade-off must be faced when scaling the power transistors, setting the capacitor value and the channel sizes of the $M2$ and $M4$ transistors.

In order to observe the $CBD2$ voltage ($V_{s1} - V_{s2}$) change when the shot-through happens, transistor-level simulation results are shown in Fig. 7.30. In this case, the $dN_2$ signal was delayed in respect of the $dP_2$, with negative ($dN2$ goes up before $dP2$) and positive values. Then, the capacitor voltage is measured after the states transition ($T_2$ state) and depicted as function of the delay. Additionally, several curves are plotted for different capacitor values so as to observe the impact of this

![Fig. 7.30](image.png)

**Fig. 7.30** Shot-through existence relationship with the delay between both power MOSFETs gates signals ($dP_2 \rightarrow dN_2$), and the observation of a current spike on the $P_2$ source terminal during the $T_3 \rightarrow T_2$ transition.
magnitude upon the capacitor voltage change. Furthermore, the presence of a current spike in the $P_2$ source (due to the shot-through event) was observed, and it is represented as a binary magnitude, where 2 means its presence, and 0 its absence.

From these results, it is concluded that the optimum capacitor value at which the voltage change due to the current spike is maximized (which is desirable to make the detection easier), is not the lower one as expected, because of the aforementioned charge-injection issues that preclude the $V_{s1}$ voltage to go low when no shot-through is detected. Additionally, it is observed that the capacitor is able to detect the shot-through event, storing the injected charge. In case of very low positive and even negative $t_{BD}$ values, it is observed that the $C_{BD2}$ capacitor voltage saturates to the supply voltage (in this case 1.8 V, as the power driver).

In the herein presented design, the capacitor values were established as $C_{BD1} = 70$ fF and $C_{BD2} = 100$ fF, as a trade-off between the capacitor voltage change and the time required to discharge it. The consequent voltage swing at the $V_{s1}$ node must be taken into account when designing both $M2$ and $M4$ transistors, as well as the $U1$ inverter.

The results of transient transistor-level simulations are included in Fig. 7.31. Both possible cases are depicted, and the output of the $U1$ inverter along the $T2$ state is observed to properly distinguish the presence or not of the shot-through conduction. To show the presence or not of the shot-through conduction, the source current of

![Image](https://via.placeholder.com/150)

**Fig. 7.31** Transistor-level simulation results of the shot-through event detection: a the $t_{BD} = 0$ causes the shot-through conduction; b $t_{BD} = 400$ ps precludes it
The circuit finally developed for the body-diode and the shot-through events correction is presented in Fig. 7.32.
In the circuit design, the capacitor values are $C_{A1} = C_{A2} = 20 \text{ fF}$, $C_{B1} = C_{B2} = 60 \text{ fF}$. As observed, greater impact on the feedback voltage modification has been determined for the shot-through event detection. The reason for this is that it is a more dangerous event (it could damage the input battery), which requires to avoid it as soon as it appears.

The feedback capacitors $C_{f,BD1}$ and $C_{f,BD2}$ present a value of $1 \text{ pF}$, which is much smaller than their counterparts of the Sect. 7.1.4. This is required because four feedback loops exist in the secondary control loop, which interact between them through the converter operation. As a result, two different values were used for the feedback capacitors to separate the dynamics from these feedback loops.

Apart from the circuits that are in charge of detecting the body-diode conduction as well as the shot-through events (to modify the delay of the power MOSFETs signals generation), other required additional circuits have been highlighted by means of gray boxes.

The two boxes on the top of the figure are required to change the voltage levels of the power drivers outputs $dN_1$ and $dN_2$ from their floating voltage supply (due to the self-driving scheme, presented in Sect. 5.3), to the amplitude of the voltage supply of the control circuits ($V_{bat}$). These signals are required to properly determine the observation windows at which the body-diode and the shot-through events must be detected. This is carried out by means of the $U_{18}$ and $U_{19}$ NOR gates that supply the corresponding inverters allowing or not their operation. In Fig. 7.33, the appropriate operation of the circuit corresponding to the $dN_2$ signal is shown, by means of the observation of the input signal $dN_2$ and the outputs $N_{2p}$ and $\overline{N_{2p}}$.

**Fig. 7.33** Transistor-level simulation results of the circuit in charge of changing the voltage levels of the power driver output $dN_2$ (with floating power supply), to the battery voltage levels.
On the bottom, two starving inverters are used to adjust the delay of the PMOS power switches driving signals, in the same way as the one used to modify the delay of the NMOS counterparts in Sect. 7.1.3.

The global operation of the whole presented circuit to adjust the dead-time when applied to the 3-level converter, can be observed in Fig. 7.34: both feedback voltages are shown, and their evolution towards the proper dead-time ($t_{BD}$) adjustment.

![Fig. 7.34 Transistor-level simulation results from the application of the proposed circuitry to adjust the dead-time on the designed 3-level converter](image)

The voltage glitches observed in $V_{fb_{BD1}}$ and $V_{fb_{BD2}}$ are due to the charge injection of the corresponding switches that connect the capacitors in parallel.

In Figs. 7.35a, b, details of the $v_x$ voltage and the source current of both PMOS power transistors ($i_{SP1}$ and $i_{SP2}$) are provided, at the beginning and at the end of the feedback loop adjustment. Power transistors gates signals are also shown. However, in this case, the source-to-gate voltage for the PMOS transistors is shown instead of the gate voltage, to better show the potential signals overlap.

In these figures, it is clear how the feedback loop is capable to adjust the dead-time until almost eliminating the body-diode conduction, without falling into the shot-through conduction. In Fig. 7.35a, two body-diode conduction events are observed that last for about 800 and 550 ps, whereas they have disappeared in Fig. 7.35b.

Additionally, no current spikes are observed in $i_{SP1}$ and $i_{SP2}$ in the transition towards the $T_2$ state. The only observed spikes occur at the beginning of $T_1$ and $T_3$ as a result of the charge spent in the parasitic capacitors of the power plant.

The developed layout design for the circuit implementation proposed in this section is presented in three different figures: Fig. 7.36 shows the main part of the
7.1 Secondary Control Loop

Fig. 7.35 Results of the $V_{fb,BD1}$ and $V_{fb,BD2}$ adjustment by means of the feedback loop, on the $v_x$ voltage and source current of both PMOS power transistors ($i_{sP1}$ and $i_{sP2}$): a when the voltage is still to be adjusted; b after the feedback loop correction

Fig. 7.36 Layout design corresponding to the main part of the circuit that adjusts the $V_{fb,BD1}$ and $V_{fb,BD2}$ voltages to avoid the body-diode and the shot-through conduction
Fig. 7.37 Layout design corresponding to the circuit that changes the voltage levels of the signals applied to the gates of the NMOS power transistors.

circuit, Fig. 7.37 depicts the layout design of the circuits in charge of changing the voltage levels of the NMOS power switches gates signals, and Fig. 7.38 corresponds to the layout of the circuits that modify the signals propagation delay by means of starving inverters.

Once again, the feedback capacitors have not been included in the layout view of the Fig. 7.36, because their large size might reduce the visibility of the rest of the circuit.

### 7.1.6 Inductor Short-Circuit

In the DCM operation of classical buck converters, noisy resonant oscillations may appear in the \( x \)-node voltage and the inductor current as well, because of the resonance between the inductor and the \( x \)-node parasitic equivalent capacitor. This kind of oscillations becomes unavoidable because of the different energy states of the capacitor at the end of \( T_{\text{off}} \) (\( v_x = 0 \)) and at the end of \( T_i \) (\( v_x = V_o \)), even though the inductor current is zero. Due to the similarity between their operation, these undesired oscillations along the inactivity states also exist in a DCM operated 3-level converter. Obviously, it is desired to cancel this behavior to avoid interfering other circuits that might exist in the surroundings of the converter (specially, in case of a Powered-System-On-Chip implementation).
In Fig. 7.39, these oscillations can be clearly observed. They correspond to transistor-level simulation results where the selected design of the 3-level converter is implemented without the inductor short-circuit.

The most common way to suppress this issue is to short-circuit the inductor along the $\bar{T}_1'$ and $\bar{T}_3'$ states [105], to dissipate the remaining energy in the parasitic resis-
tance of the short-circuit path as soon as possible. Because of the effectiveness and simplicity of this method, it has been adopted in the present design.

As exposed in Fig. 7.40, two NMOS transistors ($W_{ch} = 100 \mu m$) are used to short-circuit the inductor. To drive these transistors, two different 3-input NOR gates determine the inactivity states, based on the information from the signals corresponding to the PMOS transistors ($P_1$ and $P_2$), the signals that identify the half of the switching period ($s$ and $s_2$), and the gate signals of the NMOS power switches.

To guarantee that the NMOS power transistor has been switched-off before the inductor short-circuit (otherwise it could result in the output capacitor $C_o$ short-circuit), the output of the corresponding power driver ($dN_1$ or $dN_2$) is used in the NOR gate (because it includes the signal generation and the driver delays). However, because of the floating voltage supply of the power drivers, the voltage levels of these signals need to be adapted to the control circuitry voltage supply, which is constant and equal to $V_{bat}$. Since this voltage adaption is already carried out in the dead-time adjustment circuit (Sect. 7.1.5), just the signals generated there are needed ($N_{1P}$ and $N_{2P}$).

The results of the application of the presented circuit to the 3-level converter are shown in Fig. 7.41. In this case, $v_x$ as well as the short-circuit signals $CC_1$ and $CC_2$ are depicted, and the effect upon the oscillations reduction is clearly observed.

In the figure, it is observed a relatively slow rising edge of both $CC_1$ and $CC_2$ signals. This is because a simple logic gate must charge and discharge the relatively large transistor that short-circuits the inductor.

To conclude this section, the designed layout corresponding to this circuit is presented in Fig. 7.42. Only the NOR gates can be observed, since $M1$ and $M2$ have been placed closer to the main inductor to avoid increasing the parasitic capacitance of the $x$-node.
7.1 Secondary Control Loop

Fig. 7.41 Oscillation cancellation along the inactivity states due to the inductor short-circuit

Fig. 7.42 Layout design corresponding to the NOR gates that determine the inductor short-circuit along the converter inactivity states $T_1'$ and $T_3'$

7.1.7 Overall Layout Design of the Secondary Control Loop

In Fig. 7.43 the layout design and placement of the overall secondary control loop circuitry can be observed, where the main building blocks have been highlighted by black dotted boxes. In this case, the two top metal layers have been excluded for the sake of the circuits visibility. These two layers are mainly used to implement the power supply lines, as well as to route the longest signals paths (since they present lower parasitic capacitance coupled to substrate).
7.2 Power Plant Implementation

This section presents the power plant layout implementation, which includes the reactive components, the power switches and their drivers, and the two transistors used to short-circuit the inductor (as explained in Sect. 7.1.6). Since components values are determined by the design space exploration results, only the layout design is explained in each case.
7.2 Power Plant Implementation

7.2.1 $C_o$ Capacitor

Recalling the design details obtained from Table 6.5, the output capacitor ($C_o = 25.89 \text{nF}$) is composed by a matrix of 7219 MOSCAPs, each of them with a channel length and width of 3.58 and 159.5 $\mu\text{m}$, respectively. According to this data, a rather square matrix is designed, which only presents the apertures required to place the inductor bonding pads. The resulting layout distribution and its dimensions are presented in Fig. 7.44. As explained in the MOSCAP matrix presentation (Sect. 3.2), only the three bottom metal layers ($\text{metal-1, -2 and -3}$) are required for its implementation.

![Fig. 7.44 MOSCAP matrix used to implement the output capacitor of the converter](image)

7.2.2 $C_x$ Capacitor

From the same table as in case of $C_o$, the design data corresponding to the $C_x$ capacitor are obtained. In this case, the capacitor design should fit the same area as the occupied by the $C_o$ capacitor ($5.07 \text{mm}^2$), resulting in 5.07 nF. Thus, as observed in Fig. 7.45, the $C_x$ capacitor layout design presents a shape similar to the $C_o$ capacitor, but in this case only the two top metal layers ($\text{metal-4 and -5}$) are used, in addition to the special MMC layer that the manufacturer provides to implement MIM ($\text{Metal-Insulator-Metal}$) capacitors.

Due to technological limitations, a single large capacitor could not be designed. Instead, a matrix of 507 capacitors of 10 pF each is required.
Fig. 7.45 Layout design corresponding to the $C_x$ capacitor. In this case a matrix of 507 capacitors of 10 pF each is required.

### 7.2.3 Inductor

From the layout design point of view, only the appropriate bonding-pads distribution is needed for the inductor implementation. According to the data from Table 6.4, a three turns spiral with an external side length of 2.3 mm is to be implemented. According to the bonding-wire manufacturer, a minimum distance between wires of 50 $\mu$m must be respected, as well as a distance between pads centers of 100 $\mu$m. Therefore, a design that accomplishes all these specifications is carried out.

Figure 7.46 shows the overall pads distribution. As expected, double pads connected by wide metal paths are used in the spiral vertices, since two straight bonding wires need to be connected, whereas the input and output terminals of the inductor require single bonding pads. The resulting bonding wires are depicted by means of dashed gray lines.

In Fig. 7.47, more details on the designed bonding pads are shown.

### 7.2.4 Power Drivers Layout

The power drivers design is also based on the results of the design space exploration, presented in Chap. 6. As stated before, a particular power driver design for each different power transistor must be addressed.
Fig. 7.46 Overall distribution of the bonding pads required to implement the triangular spiral corresponding to the inductor design.

Fig. 7.47 Details of the different bonding pads designs, required to build the whole triangular spiral.
In Table 7.1, the channel widths of all the transistors that compose all the four different power drivers can be found. Since the power drivers corresponding to the $P_1$ and $N_1$ transistors make use of input – output transistors, their length is $L_{ch} = 0.34 \mu m$. On the other hand, the core transistors that compose the drivers for the $P_2$ and $N_2$ power switches present a channel length of $L_{ch} = 0.24 \mu m$. Additionally, in the later case, the PMOS transistors of each inverter are low-$V_T$ transistor, since this selection reduces the driver energy consumption (according to the corresponding characterization developed before the drivers design).

Furthermore, all the NMOS transistors that compose the four drivers are placed in a PWELL separated from the substrate (which is possible in Triple-Well processes, as the one used to implement the design), in order to avoid the latch-up issue (which in this case is particularly prone to appear, because of the large size of the power drivers last stages). In case of the power drivers corresponding to the $P_2$ and $N_2$, the use of a separate PWELL for the NMOS transistors is a must, since their sources and substrates need to be connected to the floating $v_B$ voltage, instead of ground. This is an issue that does not affect the PMOS transistors since the corresponding NWELL can always be connected to any different voltage higher than ground.

In Figs. 7.48, 7.49, 7.50 and 7.51, it is presented the layout design corresponding to the four power drivers of the $P_1$, $P_2$, $N_1$ and $N_2$ power switches, respectively.
Fig. 7.49 Layout design of the power driver that acts the $P_2$ power transistor

Fig. 7.50 Layout design of the power driver that acts the $N_1$ power transistor

Fig. 7.51 Layout design of the power driver that acts the $N_2$ power transistor
The main guidelines to follow in the design of the power drivers layout is to reduce both the parasitic capacitances due to the wide metal paths interconnections, while keeping low values of the parasitic resistance of such paths. Hence, it is very interesting to put all the transistors as close as possible to each other. Although this could increase the possibilities of the latch-up issue, the use of triple-well NMOS transistors precludes it.

Moreover, many guard rings are placed surrounding the power drivers so as to reduce the substrate interferences on the nearby circuits, corresponding to the secondary control loop.

### 7.2.5 Power Transistors Layout

The developed design for each of the power MOSFETs is quite straightforward. The PMOS transistors present the low-$V_T$ characteristic (since it results in lower parasitic on-resistance values), and NMOS are placed in a PWELL separated from the substrate to reduce the injected interferences to the substrate. Furthermore, in case of the $N_2$ power transistor, its placement in a separated PWELL is mandatory, since its source and body terminals are connected to $v_B$.

In this work, the layout design of the power MOSFETs has been determined to follow the classical finger structure so as to make it simple. Nevertheless, some guidelines have been followed in their design.

- It is interesting to use the widest possible metal paths to reduce the overall parasitic resistance of the power switch. In this perspective, it is also interesting to use as many metal layers as possible to route the power paths.
- The polysilicon gate terminals of the power transistor are connected at both ends of each finger by means of the polysilicon and the metal-1 layers so as to reduce the gate resistance, which is directly related with the resistive switching losses (explained in Sect. 3.4.2.2).
- The wider the fingers, the higher the gate resistance because of the distributed RC circuit corresponding to the gate polysilicon. Additionally, the equivalent transistor on-resistance is also increased because of the narrow connections along the fingers. However, reducing too much the fingers width ($W_{finger}$) will increase its number (for a given transistor channel width). The later results in a width increase of the overall power transistor structure, which implies an increase of the gate connection capacitance, plus a more difficult access from the power driver output (expected to be smaller), that finally would also increase the gate resistance. Thus, the fingers length is a trade-off between the gate terminal resistance and the power switch on-resistance, and the gate capacitance that must be driven by the power driver.
- Furthermore, the overall size of each transistor structure is also determined by the dimensions of the terminals to be connected (this is, the inductor bonding pad, the $C_x$ contacts, or the input and output power paths.)
In order to further reduce the gate resistance, any power transistor is subdivided into different sections that group several fingers, and then, all of them are parallel connected. This allows to short-circuit each group gate terminals at both sides, by means of metal-1 strips.

In Fig. 7.52 the four designed power transistors are shown. The same scale is used in all of them and their dimensions are noted, for a better comparison of their final shape and dimensions.

![Fig. 7.52 Layout design of the four power transistors. All of them are depicted at same scale and their dimensions are noted, for a better comparison between their final shape and size](image)

As it could be expected, $P_1$ and $N_1$ present the wider structure, since they connect the external power paths to the $C_x$ capacitor, presenting both of them very wide contact surfaces. However, the dimensions of the corresponding drivers preclude the design of extremely wide structures (i.e. higher number of shorter fingers). On the contrary, the bonding pad used to connect the inductor presents smaller dimensions, which demands for transistor structures with lower number of longer fingers. This is the case of the transistors $N_2$ and $P_2$.

In Fig. 7.53, details of the $P_1$ layout design are presented as an example of the developed structures.

![Fig. 7.53 Details of the developed layout design for the $P_1$ transistor](image)
And finally, Fig. 7.54 shows, as an example, the connection between $N_2$ and its corresponding driver.

### 7.2.6 Overall Layout Design of the Power Plant

In this section an overall view of the whole layout design corresponding to the power plant is presented in Fig. 7.55. This figure includes all the reactive elements and the power switches and drivers.

![Diagram](image-url)
Figure 7.56 shows a better view of the power transistors and drivers, to clarify their distribution around the bonding-pad of the inductor (x-node). Furthermore, in this figure, the transistors used to short-circuit the inductor along the inactivity states (as explained in Sect. 7.1.6) are also marked.

### 7.3 Complete Converter Design and Results

In this section, the most relevant results from transistor-level simulations corresponding to the complete converter design are presented. Additionally, the complete layout design joining the converter itself plus the whole secondary control loop is exposed. In all the presented waveforms, the switching frequency was established to \( f_s = 18.64 \text{ MHz} \), and the output load was set to \( I_o = 50 \text{ mA} \), since it was observed that the developed circuit was unable to operate at the selected switching frequency \( f_s = 37.28 \text{ MHz} \).

First of all, the most significant waveforms corresponding to the converter functionality are depicted. Figure 7.57 depicts the stabilization of the four feedback loops corresponding to the secondary control.

The results show that after the feedback voltages adjustment, the output voltage increases towards 1 V. Since this is achieved without any modification of the \( I_{bias_{,D}} \).
(that determines the $T_1$ and $T_3$ duration), it is observed that the proper dead-time adjustment and the NMOS power switches cut-off at $i_L = 0$ moment, increases the power efficiency (which results in a output voltage increase). Furthermore, an stabilization is also observed in the $C_x$ capacitor voltage, after the feedback loops adjustment.

In the results of Fig. 7.57 it is also observed the reduction of the positive and negative peaks of the inductor current and the $v_x$ voltage, as a result of the secondary control loop operation.

In order to provide a clearer scope on the most significant generated signals of the whole system, Fig. 7.58 depicts them for a narrow temporal span. In this case, the gate voltages of all the PMOS power transistors are shown as the source-to-gate
voltage, for a better observation of the dead-time between their falling edges and the corresponding NMOS switches gates voltages. As a visual reference, the $v_x$ voltage is also exposed.

Figure 7.59 presents a detailed view of the most representative voltage waveforms resulting from the operation of the complete system, such as the voltage at the terminals of the $C_x$ capacitor ($v_A$ and $v_B$) and the output voltage ripple, all of them referred to the $v_x$ voltage waveform, so as to better identify the different converter states.
Finally, in Fig. 7.60, the most significant current waveforms are presented. In this case the input battery current ($i_{bat}$) is shown as well as the current sourced or provided by the $C_x$ capacitor ($i_{C_x}$). In addition to this, the current sourced by the power drivers ($i_{driver}$) corresponding the $P_1$ and $N_1$ power switches is depicted as the difference between the battery current and the current sourced by the $P_1$ transistor ($i_{sp1}$). Inductor current is shown, as well, for which only a small oscillation is observed (thanks to the inductor short-circuit system).

From all the presented transistor-level simulation results, it is concluded that the desired operation is achieved by the proposed system, including not only the power devices, but also the secondary control loop. Unfortunately, the developed system
was unable to work at the obtained switching frequency from the design space exploration results carried out in Chap. 6. Consequently, the output current was reduced to 50 mA and the switching frequency to $f_s = 18.64$ MHz, in order to keep the proportionality $k = \frac{f_s}{I_o}$.

Then, the output voltage ripple (Fig. 7.62) and the power efficiency (Fig. 7.61) are measured for different output current values, while keeping the proportionality between the output current and the switching frequency (which implies to keep constant the $I_{bias,D}$ current value).

As observed, the power efficiency obtained from the transistor-level simulation results closely matches the predicted from the design space exploration results,
Transistor-level simulation results, without the action of the dead-time and the $i_L = 0$ circuits adjustment.

Fig. 7.61 3-level converter efficiency as a function of the output current, contrasted against the resulting from the presented models. Power efficiency corresponding to transistor-level simulation results is also depicted for the case of deactivating the adaptive dead-time and $i_L = 0$ adjustment feedback loops. In this case, adjustment voltages were set to $V_{fb1/2} = 2\text{ V}$ and $V_{fb01/2} = 0.8\text{ V}$.

Transistor-level simulation results.

Fig. 7.62 Output voltage ripple of the implemented 3-level converter design as a function of the output current, contrasted against the resulting from the presented models.
7.3 Complete Converter Design and Results

**Fig. 7.63** Output voltage evolution as a function of the output current

**Fig. 7.64** Global view of the whole developed system
which validates the presented loss models (at least in front of the models provided by the foundry). Furthermore, it is observed that the power efficiency is kept relatively constant for about two decades of output current values. Additionally, this figure depicts transistor-level simulation results corresponding to the case of cancelling the effect of the secondary control feedback loops. In this case, the adjustment voltages were set to $V_{fb1/2} = 2\,\text{V}$ and $V_{fbBD1/2} = 0.8\,\text{V}$, which produced an efficiency reduction of a 5%, approximately.

As regards the output voltage ripple, it is observed that it is higher than the level predicted from the presented models. However, this could be expected since the output ripple model presented for the 3-level converter does not include the effect of the $C_o$ and the $C_x$ capacitors ESRs (because of its high complexity). Moreover, it did not include the effect of the self-driving scheme to supply the power drivers from the $C_x$ capacitor. Obviously this increases the $v_{C_x}$ voltage swing which, in turn, increases the output ripple.

To finish with the simulation results, the evolution of the output voltage RMS value as function of the output current is exposed in Fig. 7.63. From the figure, it is observed that the output voltage is kept constant for a wide range of output current values. This implies that the power efficiency reduction as the output current becomes lower is due to the higher input current demand, rather than to the output voltage decrease.

![Secondary control loop](image)

**Fig. 7.65** Zoomed view of the secondary control loop components around the power switches and drivers
The layout view of the overall designed system is presented in Figs. 7.64 and 7.65 (that offers a zoomed view of the secondary control loop elements distribution around the power switches).

In the closer view of Fig. 7.65, the feedback capacitors of the blocks that adjust the $T_2$ state duration as well as the dead-time, can be clearly seen.

Also, other elements not presented in this chapter are observed. However, they are not part of the converter complete system, but they were added to the design just to help the test of the chip (e.g. to buffer some internal voltage signals which are needed to be observed through the package pins).