33

Reduction of cycle time in manufacturing using simulation

A.W. Chan
Integrated Manufacturing Technologies Institute
National Research Council of Canada
Montreal Road M50, Ottawa, Canada, K1A 0R6
tel: 1-613-993-9437, fax: 1-613-941-1571
e-mail: albert.chan@nrc.ca

A. Satir
Department of Decision Sciences and MIS
Concordia University
Montreal, Canada, H3G 1M8
tel: 1-514-848-2974, fax: 1-514-848-2824
e-mail: ats@vax2.concordia.ca

V. J. Thomson
Department of Mechanical Engineering
McGill University
817 Sherbrooke Street West, Montreal, Canada, H3A 2K6
tel: 1-514-398-2597, fax: 1-514-398-7365
e-mail: thomson@mecheng.mcgill.ca

Abstract

A shop floor model of a large electronics manufacturer was developed to study the reduction of manufacturing cycle time. The model followed the manufacture of electronic systems from printed circuit board preparation, through board assembly and test, to final system assembly and system testing.

Simulation allowed the evaluation of four different tactics for manufacturing cycle time reduction. These were: the effect of setup, breakdown and lot size on printed circuit board (PCB) assembly; the implementation of a total pull tactic on a

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production line; the comparison of improved quality in manufacture and rework; and the effect of balancing personnel across shifts.

The study used actual production data. Conclusions about the study and the effectiveness of alternative tactics are presented.

Keywords

Shop floor simulation, manufacturing cycle time, electronics manufacturing

1 INTRODUCTION

The spectrum of manufacturing operations can be classified from make-to-stock (MTS), where all products are standardized, at one extreme, to engineer-to-order (ETO), where the customer specifies the purpose of the product, at the other. In between these extremes in the manufacturing spectrum are assemble to-order (ATO) and make-to-order (MTO) type operations. ATO involves an environment where major components and subassemblies are held in stock awaiting customer orders and can be treated either as a unique environment by itself or the first step from an MTS to an MTO environment. In an MTO environment, products are made to customer requests, usually involving a large engineering component.

The manufacturing technologies (such as FMS, robotics, CIM) and management based approaches (such as supply chain management, JIT, BPR) that have been implemented over the last two decades enable enterprises to compete on time-based performance, especially in ETO, ATO and MTO environments. Time reduction at all phases and levels of manufacturing from order processing to shipment is emerging as a pivotal issue in this respect.

Modeling and analytical aspects of cycle time reduction are studied in Karmarkar (1987), Kingsman et al (1989), Hill and Khosla (1992), Lockamy III (1993) as well as Miltenburg and Sparling (1996) among others. Frameworks for analyzing lead time related issues are developed in Kingsman et al (1989) incorporating a hierarchy of lead times that add up to total delivery lead time. Certain input/output control procedures are proposed. A cost/benefit analysis based framework for lead time reduction is argued in Hill and Khosla (1992). Lockamy III's framework, on the other hand, is based on a study of six large manufacturing organizations. Performance measures by various functions are proposed for lead time management. Mathematical models are developed to study cycle time in Karmarkar (1987) and Miltenburg and Sparling (1996). In the former study, the impact of lot sizing and work-in-process stocks on lead time is studied. In the latter article, three models in the form of a stochastic, Markov chain and a queuing model are developed to study cycle time management in MTO, ATO and MTS environments.

Approaches and techniques for lead time reduction are discussed in Hopp et al (1990). The overall conclusion is that the most effective factors in lead time reduction are the decrease in mean flow time and flow time variance. A study by Handfield and Pannesi (1995) focuses on how firms can achieve a time-based

advantage in MTO manufacturing environments through: i) cross functional design participation, ii) just-in-time purchasing, iii) improved supplier delivery and quality performance, and iv) lot size reduction. A structural model and relevant measures were developed. The model was tested using interview data with managers in forty plants from nine industries. Findings suggest the significance of factors (ii) and (iii) on lead time based competitiveness.

Rather than focusing on a limited number of factors as in many of the articles reviewed, this study covers a wider range of operational factors and analyzes their impact on lead time. The production line studied in this article operates in a hybrid environment of MTS and MTO. The study objectives, factors studied and their impact on cycle time are discussed in the following sections.

2 STUDY OBJECTIVE

The authors in collaboration with a large manufacturer of electronics equipment developed a computer model/simulation of the supplier's manufacturing operations in order to assess the potential benefits of applying simulation technologies to the study of its manufacturing and business operations, as well as to understand how overall manufacturing cycle time can be shortened. The project examined the drivers and the effects of reducing manufacturing cycle time, where manufacturing cycle time was defined as the time from work orders arriving on the shop floor to the point when fabricated items are deemed to be finished goods. The study had two major objectives: a) to determine how to achieve a reduced manufacturing cycle time, and b) to investigate the effects that reduced time would have on other functions in the enterprise, e.g., order fulfillment, production planning, etc.

A Manufacturing Enterprise Model was developed, comprising three submodels: an Order Fulfillment Submodel, an Inventory Submodel, and a Shop Floor Submodel. The Order Fulfillment Submodel was composed of those business processes from receiving a customer order to invoicing of the customer including order entry, custom product configuration, material planning, production scheduling, and distribution. The Shop Floor Submodel was composed of those processes from reception of work orders to placing finished goods into inventory. A separate Inventory Submodel was created to track ordered components, work-in-process (WIP), and finished goods. The points of communication between the submodels are the work orders which come from the central planning function, the components which are controlled and purchased by the planning and purchasing functions, and which are drawn upon by the shop floor, and finished goods which are placed in inventory by the shop floor, and then, delivered to the customer by distribution as part of the order fulfillment function. More detail about this integrated modeling approach is in Chan and Thomson (1997).

The present paper deals with the study of tactics which allow the reduction of manufacturing cycle time and discusses the Shop Floor Submodel only.

3 SHOP FLOOR STUDIES

The Shop Floor Submodel was developed using ProModel, a Windows based tool for simulating and analyzing discrete part manufacturing systems. The model was based on the production facility of the participating electronics manufacturer. A typical line starts with board preparation and screen printing (application of solder). A number of automated steps for component placement, including surface mount, automatic insertion, mold seal, and connector assembly is performed. These are, then, followed by a before-wave, wave (soldering) and after-wave assembly sequence. In-circuit testing is performed next, followed by mechanical assembly into system units. The system units are, then, passed through a series of testing stages, including functional test, post-functional test and environmental test, where they have to be tested in conjunction with other system units. Having passed all the foregoing tests, a system may still undergo system test and customer requested field acceptance testing. The model terminates at finished goods inventory. A schematic of this process is shown in Figure 1.

The specific studies for manufacturing cycle time reduction were based on data supplied by the electronics manufacturer for several days of production. Four different tactics to reduce cycle time were investigated:

1. variation of setup, breakdowns, and lot size parameters
2. use of a complete 'pull' tactic across the assembly and test sections
3. improvement of quality, and
4. changes in the distribution of personnel employed across shifts.

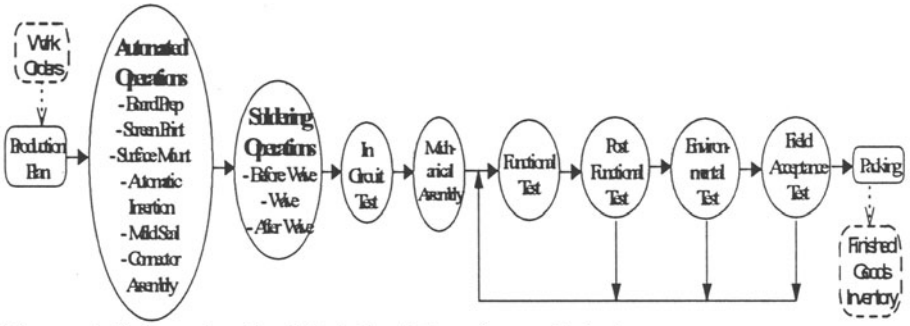

Figure 1 Schematic of printed circuit board manufacturing processes

4.1 Impact of lot size, setup times and downtimes

The Shop Floor Submodel was used to study the impact of lot size, setup time, breakdown frequencies and repair times on the assembly time for the assembly section of the PCB production line as described above. Products assembled on the line were grouped into six families. Data for setup, processing and repair times and breakdown frequencies were gathered for each station/product combination from company files and through stopwatch studies in certain cases. All parameters of the model were assumed to be deterministic, with the exception of breakdown

occurrences, which were assumed to follow a Poisson distribution. The model was validated to assess the degree to which it corresponded to the real system being simulated. The comparison between the model's findings in term of the distribution of various times and the company's actual data for the validation period was quite favorable, as illustrated in Table 1. The comparison was for one machine which was typical of other machines in the line. Since the line was balanced, the idle time was completely due to the effects of setup and downtime from other machines, i.e., machines were either blocked or starved for work. Downtime was the sum of intervention time to failed stations and repair time.

Table 1 Distribution of operating times for a typical workstation

	Setup (%)	Processing (%)	Idle (%)	Downtime (%)
Model	14.5	19.5	50.0	16.0
Actual	14.0	20.0	48.0	18. 0

Two separate days of operations were simulated on the line. Each 24 hour day is denoted by sample 1 and sample 2. The input data used to simulate these two days was deemed to be appropriate since the data cover most of the product types made by the manufacturer. Also, the total number of boards processed in both days was quite large. The performance measures used to evaluate the impact of a given factor were: i) throughput time, i.e., the number of hours required to process 275 and 295 PCBs, in sample 1 and 2, respectively, and ii) throughput rate per day, i.e., the number of PCBs assembled per 24 hours. When the former measure was of concern, a terminating type simulation was run, where the simulation starts and ends at a defined state/time. In such a case, the behavior of the system over this particular period of time is of interest, rather than its steady state behavior.

While all other parameters were at base levels and breakdowns were disabled, simulations with lot sizes of 14, 10, 7, 5, 3 over a 24 hour period provided the throughput rates in terms of PCBs assembled given in Table 2. A lot size of 7 was used in other scenarios since it was the actual lot size used by the manufacturer.

Table 2 Variation in output with change in lot size

Lot size	Sample 1 (Number of PCBs)	Sample 2 (Number of PCBs)
14	378	392
10	355	351
7	327	345
5	280	285
3	226	235

The impact of varying setup time was tested at three levels, while breakdowns were disabled: base (current) level (1), half of base level (0.5), and zero setup time

(0). The total throughput time for assembling 275 and 295 PCBs in sample 1 and 2 for each setup time is given in Table 3.

Table 3 Reduction in production time with a reduction in setup

Setup time	Sample 1 (Hours)	Sample 2 (Hours)
Base (1)	17.63	19.27
Half (0.5)	16.81	16.61.
Zero (0)	13.91	14.56

Another set of experiments was carried out by varying the degree of downtime due to breakdowns at three levels: base (current) level (1), half of base level (0.5) and zero downtime (0). The throughput time required to assemble the 275 and 295 PCBs in sample 1 and 2, respectively, is given in Table 4.

Table 4 Reduction in production time with a reduction in downtime

Downtime	Sample 1 (Hours)	Sample 2 (Hours)
Base (1)	30.17	29.30
Half (0.5)	22.73	23.20
Zero (0)	17.63	19.27

Table 5 shows the relative increase in production for setup time and downtime reductions using a lot size of 7.

Table 5 Proportion of production increase with reductions in setup and downtime

	Sample 1	Sample 2	Average
Half setup time	1.05	1.16	1.11
Zero setup time	1.27	1.32	1.30
Half downtime	1.33	1.26	1.30
Zero downtime	1.71	1.52	1.62

It is evident that increases in production are higher when downtime is reduced compared to similar, proportional decreases in setup time. This indicates that quicker intervention to breakdowns and reduced repair times would have a larger impact in reducing the assembly time. This finding has implications for the company in terms of its preventive maintenance and repair practices.

4.2 Total pull tactic

The Shop Floor Submodel was used to study the effects of using a complete 'pull' tactic from finished goods to the start of the board assembly section. The actual production line being studied operated by pulling orders from finished goods to the start of the testing section and by 'pushing' lots of circuit boards through the assembly section. There was a small buffer between the board assembly and testing sections which acted as a 'regulator' between the processing of lots of boards and the assembly and test of systems.

The following assumptions were incorporated into the model:

a) a pull of 1 was defined as the boards required to build a complete system,
b) like boards were processed as one lot, i.e., while one system of boards was pulled each time, there were multiples of certain boards.

The original system had a lot size of 7 boards which was used during the assembly section of the line and into the in-circuit test station. In the simulations for a pull system, scenarios with lot sizes of 1, 4 and 7 boards were performed. The results for lot sizes of 1 and 4 are compared to those of a lot size of 7 in Table 6.

Table 6 The effect of a pull tactic for different lot sizes

Tactic	Reduction in cycle time	Reduction in throughput
Pull with lot size 1	45%	35%
Pull with lot size 4	15%	5%

As can be seen from Table 6, manufacturing cycle time can be reduced by 45% through the use of a total pull tactic. This was due to two main factors: first, the elimination in some cases or a reduction in the use of buffers in others along the production line, and secondly, a reduction in delay times for the various groups of boards where they waited for testing facilities, i.e., essentially, waiting times in queues which operated on a first-in-first-out basis. There were no substantial reduction in actual workstation processing times.

Nevertheless, three drawbacks were noted. First, adopting a complete pull system meant that the effective lot size was reduced; this increased the amount of setup time, thereby, reducing assembly line utilization and throughput. This had a large effect. Secondly, the reduction in the use of buffers in the testing area did reduce cycle time, but it also decreased testing facility utilization and throughput; this had a small effect. Overall, throughput was reduced due to these two factors as indicated in the above results. A third factor was the increased exposure to downtime due to possible component shortages. This was not simulated in the scenarios, but is an obvious consequence of reduced buffer size. This could be overcome by having an appropriate ordered component stocking policy.

While studying the different lot sizes, especially the lot size of 1, different operating rules for the testing facilities were tried in order to overcome some of the observed shortcomings and to determine optimum procedures. These different operating rules had minimum effect (less than 5%) on the cycle time or throughput.

4.3 Quality

Due to product variety and complexity many errors occur during the assembly of circuit boards. This is the state-of-the-art in the circuit board manufacture and will probably remain so since the desire for more variety and complexity is always pushing the capabilities of assembly lines.

In the production line studied, there were four test areas: in-circuit test, functional test, post-functional test and environmental test. The first pass yield rate of the complete testing section was about 40%, i.e., 40% of the boards tested successfully passed the tests at all four test areas the first time. The yield was this low due to the high component density and requirement for high precision placement. The effects of two different tactics that address quality were studied: first, an improved assembly quality or better first pass yield rate; second, different repair tactics leaving the first pass yield rate alone.

For the first tactic, the first pass yield rate was individually improved at each of the four different test areas. This had very little effect on reducing the overall cycle time. It was also noted in the simulations that any improvement in any single workstation, assembly or test, had very little effect on decreasing cycle time due to the highly balanced nature of the line. First pass yield rates were improved at all test areas uniformly by 10%; this gave a first pass yield rate in the testing section of the production line of about 58%. This improved overall yield rate resulted in a reduced total cycle time of about 6.5%.

When PCBs fail tests at the testing areas, they are sent to repair stations for rework. Repair operations are such that boards being repaired can take a number of repair cycles for them to pass successfully through the testing section. Simulations were done assuming that the number of repair cycles at each test center was reduced by one repair cycle. This reduced total manufacturing cycle time by 6%.

Due to some simplifying assumptions in the original models, the magnitude of the reduction in cycle time for simulations of quality improvement is underestimated. However, the interesting conclusion from the study is not so much the magnitude of cycle time reduction, but that improved repair tactics can have the same effect as significantly improving the first pass yield rate. Significantly improving rates is very difficult, if not impossible, due to the determination of precise causes for failures and the cost or inviolability of better equipment, but it is most often feasible to improve repair processes so that total rework is lowered.

4.4 Balancing personnel across shifts

One of the important considerations for operating the production lines is the allocation of workers to the various stages of the assembly and testing processes. While the utilization of human resources on the automated portion of the production line is fairly routine, the assignment of operators to the manual portion

of the production line, particularly to the various assembly and test stations, could have a significant impact on productivity. As well, the balancing of the number of workers for the different shifts in a day (or week) could have a dramatic effect on the formation of bottlenecks, and thus, WIP and throughput. Yet any changes to current practices must be justified to the work force. The Shop Floor Submodel helped to address this important issue.

The Shop Floor Submodel was applied to study the impact of various resource allocation strategies on overall manufacturing cycle time. One of the studies involved the balancing of workers across the different shifts in a working day. The assembly operations on a printed circuit board production line include before-wave and after-wave, which are labor intensive operations, and a large number of manual workstations are involved. As well, the functional testing operation is a key step in the testing sequence for any printed circuit board. Not only is this a labor intensive operation, but the testing equipment deployed is highly dependent on the type of circuit board being tested. Again, a large number of manual workstations with technicians of various skill levels have to be utilized. The Shop Floor Submodel was designed so that the number of workstations (thus, workers) deployed on any shift during the day/week for these locations can be varied easily via a spreadsheet, thereby, facilitating the experimentation of different worker assignment strategies.

In order to focus the study on the effects of shift balancing, a series of experiments was conducted to identify the needed levels of resources that are commensurate with given input volumes. The number of workstations at various locations along the production line was successively reduced until the utilization rate was reasonable (75 to 100%), and not an excessive amount of slack was experienced for a given quantity of blank circuit boards being pushed from the beginning of the production line. Once this level was identified, it was used as a reference level for shift balancing experiments. Suppose this level was found to be 15 workstations per day for the Functional Testing operation for a certain type of circuit board. In this case, the fully balanced scenario would call for a deployment of 5 workstations for each of the 3 shifts in a day. One unbalanced scenario could involve using 7, 5 and 3 workstations respectively for the 3 shifts in a day. Assuming there were actually 7 workstations available for this type of Functional Testing on the shop floor, then a highly unbalanced scenario could be 7, 7 and 1 workstations respectively for the 3 shifts.

An appropriate level of resource allocation was first identified separately for each of the operations on the production line where shift balancing strategies were being considered. Where different workstations or test sets were involved for different board types, this level was identified for each of those board types as well. With these levels serving as reference points, personnel balancing strategies for each group of workstations were tried individually as well as aggregately. In each case, the effect on overall production cycle time was compared. Multiple replications were run to even out the effects of random fluctuations in processing times and probabilistic failure rates.

The results of shift balancing experiments showed that if strategies to balance the deployment of workers over the 3 shifts of a day were applied to individual groups of workstations, such as before-wave, or after-wave, or functional testing, the impact on cycle time was not significant. However, if the same strategies were applied to multiple groups of workstations, i.e., on a larger scale, then, the difference in cycle time could be significant. Specifically, if a shift balancing strategy was applied across the board to all applicable workstations on the production line, there was a reduction in overall cycle time for the fully balanced scenario over the highly unbalanced scenario of between 15 to 20%. This result is both intuitive and conforms to theoretical analysis. In other words, it is reasonable to expect that the overall cycle time on the production line to be shorter when the 3 shifts are fully balanced when compared to a highly unbalanced scenario. The 15 to 20% reduction is lower than the theoretical difference because the shift balancing strategy is applicable only to some of the workstations on the line.

5 SUMMARY

Simulation was an excellent method for evaluating different tactics for the reduction of manufacturing cycle time. The favorable comparison of validated models to actual production results gave a high degree of confidence to the findings.

Lot size, setup and downtime
Lot size showed no optimum value; lower values gave lower cycle times, but reduced throughput also occurred. The ability to reduce manufacturing cycle time by decreasing downtime showed much greater potential than reducing setup time.

A total pull tactic
A total pull tactic greatly reduced manufacturing cycle time; however, there was a significant, simultaneous reduction in throughput. More studies are being undertaken to determine if this can be overcome.

Quality
The interesting conclusion that improved repair procedures can have as large an effect as an improved first pass yield rate for reducing cycle time was obtained. This is being investigated by the company and further research is ongoing in order to better predict the magnitude of the reduction.

Shift balance
Balancing personnel and equipment utilization across shifts reduced manufacturing cycle time compared to unbalanced operations. Only a 15 to 20% reduction was observed since balance/imbalance was only applicable to a few workstations.

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BIOGRAPHY

Albert W. Chan is a Senior Research Officer in the Integrated Manufacturing Technologies Institute at the National Research Council of Canada. He received a B.Sc. in Mathematics from the University of Minnesota, and a M.Sc. and Ph.D. in Industrial Engineering from the University of Florida. His research interests include simulation and computer modeling, decision support systems, and process modeling and re-engineering of business and industrial systems.

Ahmet Satir is a professor of production/operations management at Concordia University. His current research interests focus on supply chain management and just-in-time manufacturing systems.

Vince Thomson is the Werner Graupe Professor for Manufacturing Automation in the Department of Mechanical Engineering at McGill University. He has been involved in manufacturing and information technology related research for 20 years at McGill and the National Research Council (Ottawa). His research has ranged from shop floor control and production scheduling to the present interest in process management in manufacturing.