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Research Article

Theory and Practice of "Striping" for Improved ON/OFF Ratio in Carbon Nanonet Thin Film Transistors

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ABSTRACT

A new technique to reduce the influence of metallic carbon nanotubes (CNTs)—relevant for large-scale integrated circuits based on CNT-nanonet transistors—is proposed and verified. Historically, electrical and chemical filtering of the metallic CNTs have been used to improve the ON/OFF ratio of CNT-nanonet transistors; however, the corresponding degradation in ON-current has made these techniques somewhat unsatisfactory. Here, we abandon the classical approaches in favor of a new approach based on relocation of asymmetric percolation threshold of CNT-nanonet transistors by a technique called "striping"; this allows fabrication of transistors with ON/OFF ratio >1000 and ON-current degradation no more than a factor of 2. We offer first principle numerical models, experimental confirmation, and renormalization arguments to provide a broad theoretical and experimental foundation of the proposed method.

KEYWORDS

Nanonet, Carbon nanotube, flexible electronics, thin film transistors

Introduction

Since the year 2000, there have been many reports of a new class of devices called nanonet network thin-film transistors (NN-TFTs), whose channel material is composed of nanocomposites of carbon nanotubes (CNTs) or Si/ZnO nanowires (NWs) (Figs. 1(a) and 1(b)) [1–11]. It has often been suggested that this technology might be a higher performance alternative to now-dominant amorphous silicon (a-Si) and poly-silicon (poly-Si) technologies for applications in flexible electronics, transparent displays, etc. While the progress has been rapid—especially for CNT NN-TFTs, evolving from single resistors to RF transistors within a span of few years—there has been a persistent perception that large scale integration of CNT NN-TFT technology will be challenging (if not impossible) due to "contamination from metallic tubes" [12, 13].

It is well known that in a typical ensemble of CNTs, approximately two-thirds of the tubes are semiconducting and one-third metallic [14]. Since the conductivity of the metallic tubes cannot be controlled by gate voltage, the ON/OFF ratio of short channel transistors—where a proportionate fraction of both metallic and semiconducting tubes bridge

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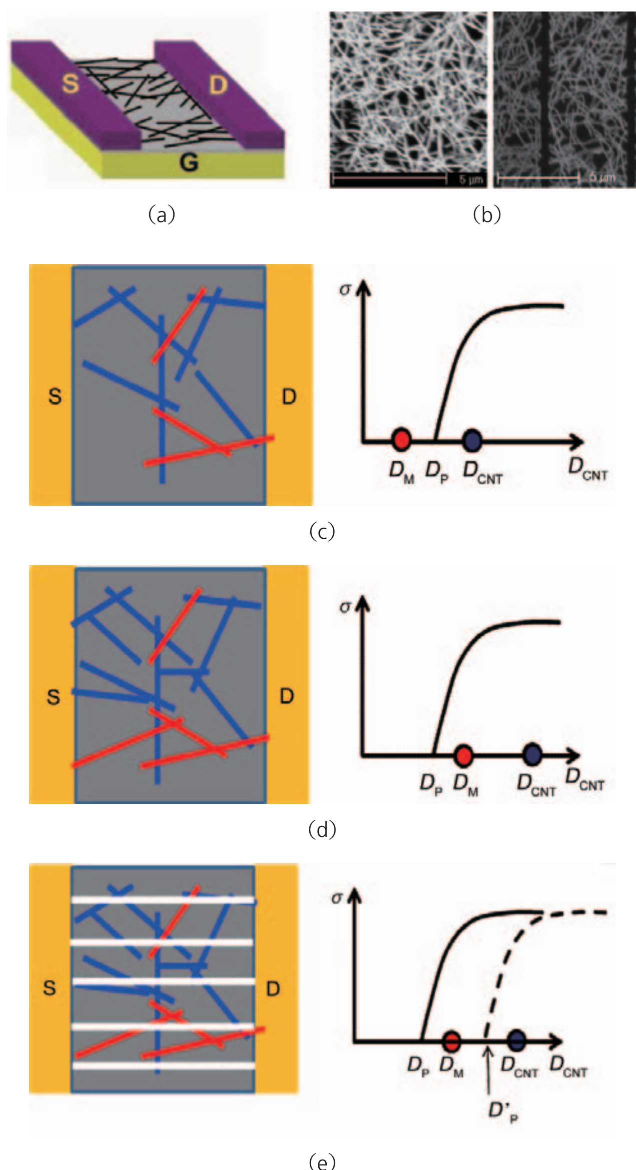

Figure 1 (a) Schematic illustration showing the CNT nanonet thin film transistor. (b) SEM images of the network before and after striping. The stripes are etched using the oxygen plasma process. The scale bar in both SEM images is 5 μm. (c) Nanonet with density (D_{CNT}) higher than the percolation threshold (D_P), but m-CNT density (D_M) less than D_P. The right panel is a plot of conductance (σ) vs density (D_{CNT}) illustrating various densities. The conductance is negligible if the density is below percolation density. (d) Nanonet with $D_{CNT} > D_M > D_P$. (e) Striped nanonet obtained from that in (d). As the striping breaks conducting paths, the entire solid curve in the right panel shifts to the dotted curve

the source (S) and drain (D) directly—cannot exceed ~3. This ratio is unacceptably small for large scale integration of transistors that demand an ON/OFF ratio of at least ~10^3–10^4. Such high ON/OFF ratio is possible for longer channel CNT NN-TFTs where individual tubes do not thread the S/D directly, so that carriers must percolate from source to drain by hopping through a percolating path of a network of sticks. As long as the percolation threshold (D_P, see Fig. 1(c)) is smaller than the density of CNTs (D_{CNT}) but larger than that of the metallic tubes (D_M), all percolation paths from S/D must involve the at least one semiconducting segment. Gate modulation of this "weakest-link" ensures high ON/OFF ratio.

There are however three specific challenges to this approach of ensuring high ON/OFF ratio for all transistors in an integrated circuit (IC): First, the requirement that $D_M<D_P<D_{CNT}$ dictates use of relatively low-density nets with correspondingly reduced ON-currents. Second, since an IC typically includes transistors of various channel lengths (L_C), widths (W_C), and stick length (L_{stick}) and since the finite size percolation threshold depends on L_C, W_C, and L_{stick} (i.e., $D_P = f(W_C, L_C, L_{stick})$) [15], ensuring $D_M<D_P<D_S$ requires L_C- and W_C- specific tailoring of L_{stick} for every group of transistors. Otherwise, the shift in D_P could violate $D_M<D_P<D_S$ and degrade the ON/OFF ratio to unacceptably low values. Even if a combination of such stick lengths could be produced, solution processing precludes delivery of tubes of specific lengths to specific transistors. Third and finally, L_{stick} of CNTs produced by classical techniques is not monodisperse and the inherent statistical distribution of L_{stick} in as-processed CNTs translates to a statistical distribution of D_P in various transistors across the IC. Once again, the distribution of D_P enhances the probability of accidental shorts in one of the many transistors in the IC [13], which would render the entire IC non-functional.

To solve this "metallic-contamination" issue and to address the three limitations of NN-TFTs discussed above, researchers have developed several "purification" techniques to ensure $D_S/D_M >> 2$ [16]. Briefly, these techniques include removal of metallic CNTs (m-CNTs) by chemical [17] or mechanical means prior to device fabrication [18] or *in situ* resistive [12, 19] and inductive filtering of the m-CNTs after fabrication of the transistors [20]. There is a debate whether chemical filtering modifies the properties of remaining semiconducting CNTs (s-CNTs), because device properties of such purified films have not been reported in Ref. [21]. On the

other hand, both resistive and inductive filtering has been shown to degrade ON-current significantly (because the protocol burns at least some s-CNTs along with m-CNTs) [20]. Moreover, it is not clear if the technique is scalable because while it is possible to burn m-CNTs in individual transistors by turning off the s-CNTs by gate bias and by adjusting the drain voltage, it is not clear how to translate this protocol to an IC configuration where the electrodes are interconnected and there is only a limited access to individual transistors.

In this paper, we describe the theory and demonstration of a new *in situ* technique called "striping" that simultaneously addresses the three concerns of "metallic contamination" discussed above. This method also been recently used to demonstrate the first practical medium scale circuit using NN-TFTs [1]. Striping is based on the idea that instead of reducing D_M to address the "metallic contamination" problem, one might alternatively tailor D_P for individual transistors to solve the problem of ON/OFF ratio. In simple terms, since $D_P \sim k/L^2_{stick}$ [22] (where k is a constant), D_P can be modified by tailoring L_{stick}. This modification of D_P cannot be done prior to fabrication of the devices, because each L_C requires a different L_{stick}, as discussed above. This modification is also difficult to achieve after device fabrication, because one cannot possibly find and cut to size all the randomly oriented tubes after fabrication. Striping resolves this dilemma by recognizing that percolation theory requires that L_{stick} in the expression for D_P refers to effective tube length and so long as the "average" tube-length $\langle L_{stick,eff}\rangle$ is reduced by any means, the *in situ* transistor-specific modification of percolation threshold can be easily achieved.

Briefly, the technique of striping involves the procedure shown in Fig. 1(a). Given a high-density CNT network of a given L_C, L_{stick}, and D_S/D_M, striping involves defining specific channel width (W_{stripe}) in strips. Striping reduces L_{stick} of a fraction of tubes near the stripe, which in turn translates into an overall reduction in effective $\langle L_{stick,eff}\rangle$ in the channel. This procedure—as we have mentioned before—allows transistor-specific modulation in D_P of the transistors. Intuitively speaking, in a transistor with a density of tubes above the percolation threshold (see Fig. 1(d)), there are many parallel paths carrying current from source to drain. In the striping method, the goal is to break these paths (Fig. 1(e)) by using finite stripes for individual transistors. Note that striping not only solves the L_C-specific percolation problem, but also reduces the intrinsic process-induced fluctuation of D_P due to the distribution of L_{stick}. The reduced spread of D_P reduces the chances of accidental shorting of S/D in large scale ICs.

It is obvious from the above discussion that the critical element of the striping is the definition of stripe width W_{stripe} as a specific function of L_C, L_{stick}, and D_{CNT}. Below we use the stick percolation model to develop a prescription for W_{stripe} and then validate our predictions by systematic experiments.

1. Theoretical models and summary of the fabrication process

We constructed a sophisticated first principles numerical stick percolation model for NN-TFTs by generalizing the random-network theory which has been described in several earlier publications [8, 22, 23]. Briefly, the model randomly populates a two-dimensional (2-D) grid by sticks of fixed length (L_{stick}) and random orientation (σ), and determines the ON-current I_{ON} through the network by solving the percolating electron transport through individual sticks. In contrast to classical percolation of homogenous sticks, the NN-TFT is a heterogeneous network: as noted above, one-third of the CNTs are metallic and remaining two-thirds are semiconducting. Since L_C and L_{stick} are much larger than the phonon mean free path, linear-response transport within individual stick segments of this random stick-network system is well described by drift-diffusion theory [8]. Also, small source drain voltage (V_{SD}) and gate valtage (V_G) obviate the need to solve the Poisson equation explicitly.

The key difference between the previously published models and the model used in this paper is this: Typically the width of the simulation domain is much smaller than the actual width of the transistors. Previously, this necessitated the use of periodic boundary conditions (PBC) for all sticks that

crossed the edge of the transistors. Finite width W_{stripe} related effects are fundamental to the operation of the transistors produced through striping and as such these transistors can no longer be treated by PBC. Instead, we use reflecting boundary conditions (RBC) for the potential and charge for all sticks that are "cut" by stripe lines to simulate the performance of striped NN-TFTs.

In order to validate the theory of striping, we fabricated arrays of SWNT TFTs with various combinations of L_C, W_{stripe}, and tube density (D_{CNT}). Uniform SWNT thin films were first synthesized by the chemical vapor deposition method on SiO_2 (100 nm) Si wafers. The tube density was controlled by adjusting the dilution ratio of the catalyst solution. Source/drain electrodes were patterned by the lift-off method with standard photolithography and electron-beam evaporation. Each device was isolated through oxygen reactive ion etching (RIE) while CNTs in the channel region were protected by a patterned layer of photoresist. Either phase-shift lithography or photolithography generated photoresist stripes, with variable W_{stripe}, aligned to the electron transport direction of each TFT. Subsequent oxygen RIE removed CNTs in the exposed area and transformed the stripe pattern to an underlying nanonet network as shown in Fig. 1(b). Removing the photoresist layer by acetone soaking completed the device fabrication process. The measurements of device ON-current and ON/OFF ratio were carried out in air, using a semiconductor parameter analyzer (Agilent, 4155C). Details of the methods of fabrication and characterization are described in detail elsewhere [24].

2. Results and discussion

Figure 2 shows the simulation results for ON-current (I_{ON}) and ON/OFF ratio of striped transistors for various widths, channel lengths, and stick lengths, plotted against the scaling variables W_{stripe}/L_{stick} and L_C/W_{stripe}, respectively. The nanonets have several intermingled parallel paths and the stripes break some of them depending on the stripe width decreasing both ON- and OFF- currents. Figure 2(a) shows that for a given channel length, the decrease in ON-current is relatively minor—approximately a factor of two as the W_{stripe}/L_{stick} is reduced from 15 to 0.3. The relatively benign effect on the ON-current of striping should be compared with about an order of magnitude reduction in the ON-current due to electrical filtering methods [12, 19]. Experimental results for transistors with the same dimensions are plotted in Fig. 2(b) and these measurements validate the scaling predictions from the percolation theory remarkably well.

Obviously, high ON-current is of little value if the ON/OFF ratio is not improved simultaneously. Figure 2(c) plots the ON/OFF ratio as a function of the scaling variable L_C/W_{stripe}, the channel length normalized by the width (W_{stripe}), which is the

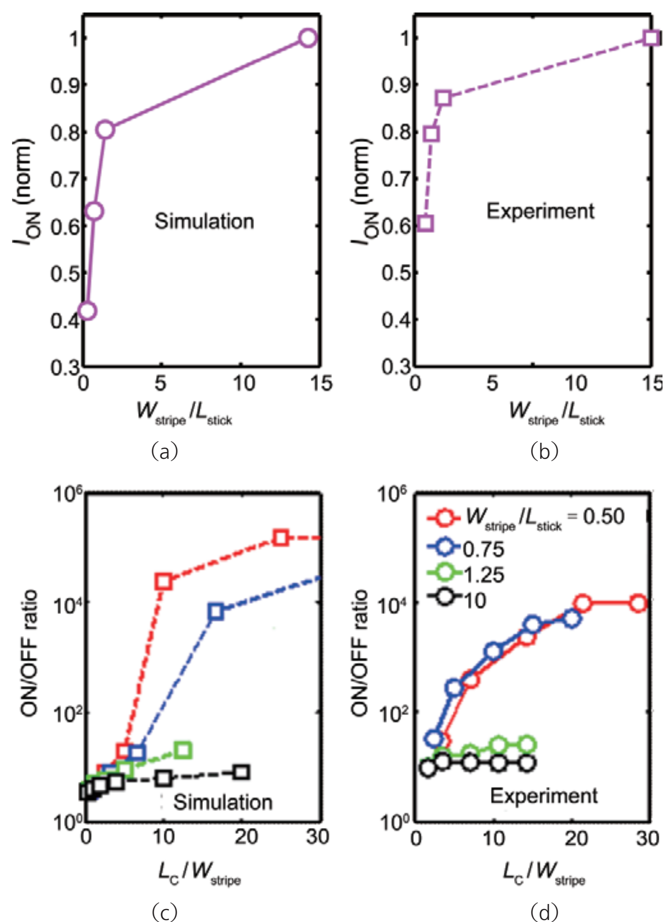

Figure 2 Variation in (a) simulated and (b) experimental ON-current (I_{ON}) with effective stripe width (W_{stripe} / L_{stick}) for tube density D_{CNT}= 40/μm^2 and effective channel length L_C / W_{stripe}=15. The ON-current decreases as the stripe width is reduced as more and more intersecting parallel paths are broken. The simulations match the experiments quite well. Variation in (c) experimental and (d) simulated ON/OFF ratio with effective channel length L_C/W_{stripe} for various values of effective stripe width W_{stripe}/L_{stick} for tube density D_{CNT} = 40/μm^2

effective stick length after the striping. The different curves are for different $W_{\text{stripe}}/L_{\text{stick}}$. At large widths with $W_{\text{stripe}}/L_{\text{stick}}$ >~1, the ON/OFF ratio is small, because in a wide device (compared to the stick length), there is always a finite probability that a metallic subnetwork would be able to bridge the S/D directly. Only a negligible fraction of the tubes is affected by striping and the length of the sticks after striping $\langle L_{\text{stick,eff}}\rangle$ is hardly suppressed by this process. As such D_{P} does not change appreciably and the ON/OFF ratio remains pegged at small values (~10), as seen in the black and green curves in Fig. 2(c). On the other hand, for $W_{\text{stripe}}/L_{\text{stick}}$ <1, the many cross-bridging percolation paths are interrupted, and the probability of an all-metallic subnetwork threading the S/D is reduced. Thus, the striping process pushes the percolation threshold into the D_{M} – D_{CNT} interval, i.e., $D_{\text{M}}<D_{\text{P}}<D_{\text{CNT}}$, with a corresponding dramatic increase in the ON/OFF ratio (Fig. 2(c), red and blue curves). However, if the channel length remains small (i.e., $L_{\text{C}}/W_{\text{stripe}}$ <5) only a few sticks are needed to bridge S/D. A metallic subnetwork can still bridge the S/D with finite probability when the ON/OFF ratio is small (<10^2) as shown in Fig. 2(c). Figure 2(d) shows the corresponding experimental results and they match the simulation results closely.

Obviously, there are many practical technological challenges that have to be solved before this methodology can be widely adopted. In this paper, we set out to explore the fundamentals of the technique so that the trade-offs and scaling issues of the methodology become well-documented. Having said that, let us briefly suggest some options: The average tube length can be adjusted via controlling the CVD synthesis parameters, e.g., catalyst species and growth time duration. In addition, since W_{stripe} can be reduced to tens of nanometers, which is solely defined through lithography, the requirement of $L_{\text{C}}/W_{\text{stripe}}$ >10 can generally be satisfied without sacrificing L_{C} through adjusting W_{stripe} (even if L_{stick} cannot be adjusted effectively).

To explore the predictions discussed above, a large number of devices with various L_{C}, W_{stripe}, and D_{CNT} were fabricated and characterized. Despite all the idealization inherent in the model and its inability to mimic the details of the physical process, once plotted against the scaled variables identified by theory ($W_{\text{stripe}}/L_{\text{stick}}$), the experimental results for the ON/OFF ratio of the corresponding transistors (Fig. 2(b)) support the theoretical trends almost exactly, showing very similar trends in ON/OFF ratio to those anticipated by the theory.

3. Optimization and generalization

The wide ranging simulation and measurement data discussed above suggest that the condition for excellent ON/OFF ratio and good ON-current is possible with striping provided that $W_{\text{stripe}}/L_{\text{stick}}$ ~1 and L_{C}/W_{stripe} >10. Specifically, for example, for a technology with 5 μm design rules, i.e., $L_{\text{C}} \geqslant 5$ μm, stripe separation should be ~0.5 μm, and the CNT length should be chosen as ~0.5 μm to ensure high yield ICs.

To complete the discussion on optimization of the striping method, let us briefly discuss the fluctuation in the tube density D_{CNT}, which plays an important role in determining the device performance (Fig. 3) and device-to-device fluctuations (Fig. 4). A higher density network with lower L_{C} is desired for higher ON-current, although an increased probability of all metallic paths decreases the ON/OFF ratio of the device. Figure 3 shows the simulation and experimental results for ON-current and ON/OFF ratio as a function of tube density for different stripe widths. Note that the ON-current has linear dependence on density for the higher density networks shown in Fig. 3. Note that the average tube length is difficult to control for a random CNT network and we have normalized the results with respect to the average tube length [22]. Figures 3(a) and 3(b) show that the ON-current has a linear dependence on density. This is expected for a network with densities much higher than percolation threshold. The increased density causes a larger number of percolating paths. These simulations can be used to optimize the device parameters such as density (D_{CNT}), channel length (L_{C}), and stripe width (W_{stripe}), given the required constraints on the device performance. The ON/OFF ratio decreases with higher tube density and is found to be appreciably high (>10^3) for all densities

if W_{stripe}/L_{stick} <1 and if the channel length is at least 10 times the width of the transistor. The ON/OFF ratios of these devices depend mainly on the fraction of useful (>10^3) devices, e.g., a single metallic path in a total of 100 paths can significantly decrease the ON/OFF ratio of the device to ~100. In Figs. 3(c) and 3(d) we see that the ON/OFF ratio decreases monotonically with the tube density. Higher densities increase the probability of an all metallic path, decreasing the ON/OFF ratio. Also, lower striping widths (W_{stripe}/L_{stick}) have a larger chance of cutting an all metallic path, hence the ON/OFF ratio is higher for lower W_{stripe}/L_{stick}.

Due to statistical nature of nanonet-TFTs (and by analogy to the random dopant fluctuation issue in classical complementary metal oxide semiconductor (CMOS) devices), we expect some variation in ON-current from one transistor to next. Apart from issues related to average ON-current and ON/OFF ratio discussed in relation to Fig. 3, the fluctuation in the ON-current and ON/OFF ratio must also be within acceptable limits for practical large scale IC design. Figure 4(a) shows the variation in normalized standard deviation (NSD) for the ON-current (normalized with respect to the average ON-current) with tube density for various values of W_{stripe}/L_{stick}. The variation in ON-current is due to the variation in the number of connecting paths from S/D. Devices with lower numbers of connecting paths are affected far more by these variations than devices with higher numbers of connecting paths. In the devices with higher numbers of connecting paths, the variation reduces due to an averaging effect. The standard deviation in Fig. 4(a), shows two trends consistent with this argument. Firstly, the standard deviation increases for lower tube densities. Secondly, striping with smaller W_{stripe}/L_{stick} leads to fewer connected paths (Fig. 3(a)) which causes higher standard deviations. For unstriped devices of large width, NSD is small (~0.05) which means only about 5%–10% variation in ON-current between different transistors. Figure 4(a)

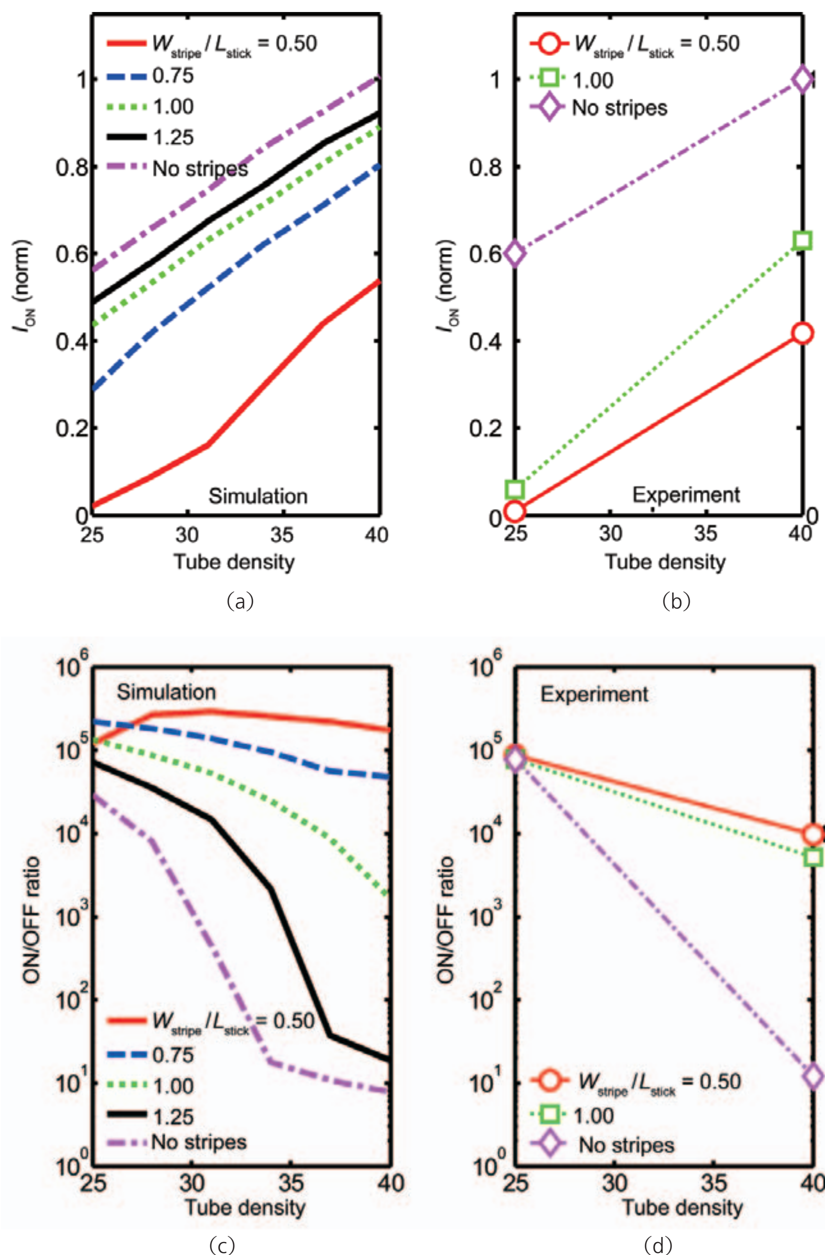

Figure3 Plots of (a), (c) simulated and (b), (d) experimental ON-current (I_{ON}) and ON/OFF ratio vs tube density D_{CNT} as a function of normalized stripe widths W_{stripe}/L_{stick}. The normalized channel length L_C/L_{stick} is held fixed at 25 for the simulations. The tube density plays an important role in determining the device performance. Note that the simulated curves for ON-current and ON/OFF ratio are statistical averages of 200 transistors. While the sample size is adequate for almost all simulations, the slight non-monotonicity of the ON/OFF ratio (b) at W_{stripe}/L_{stick}=0.5 and at lower densities (25–30) is most likely an artifact of finite sample size

shows that NSD values do change with striping; however, as long the design rule (i.e., W_{stripe}/L_{stick} ~1) is followed; specifically, provided W_{stripe}/L_{stick} = 1–1.25, NSD variation remains essentially unchanged with respect to the unstriped transistors (5%–10%) even in the unlikely scenario of 50% fluctuation in the original target density of 25 sticks/μm^2.

The importance of following the design rule of W_{stripe}/L_{stick} ~1 is further illustrated in Fig. 4(b) which shows the fraction ($f_{ON/OFF}$) of devices with high (>10^3) ON/OFF ratios for various densities. It is clear that striping reduces the sensitivity of the ON/OFF ratio to fluctuations in tube density. Indeed, while for W_{stripe}/L_{stick}>1, $f_{ON/OFF}$ decreases monotonically with density, when W_{stripe}/L_{stick} <1, $f_{ON/OFF}$ is close to 1, i.e., approximately 100% of the transistors have high ON/OFF ratios, even with 20%–50% variation in the target tube density of 25 sticks/μm^2.

The numerical simulation and experimental confirmation of the scaling relationship above provide simple, intuitive guidelines for transistor scaling. Before we conclude, however, let us offer a simple renormalization argument of the above scaling relationship so as not to obscure the physical basis of asymmetric percolation that underlies the robustness and generality of the striping technique. Understanding the renormalization argument may also allow development of other techniques that achieve the same result, without following the specific prescription proposed in this paper.

The reason striping allows an easy manipulation of the percolation threshold is because a finite stripe allows tailoring of the percolation threshold in between that of a 1-D chain of resistors (D_P=1) and a 2-D resistor network (D_P=0.5). The precise value of D_P for a finite width resistor on a square lattice is obtained from the recurring renormalization condition that (see Fig. 5) [15]

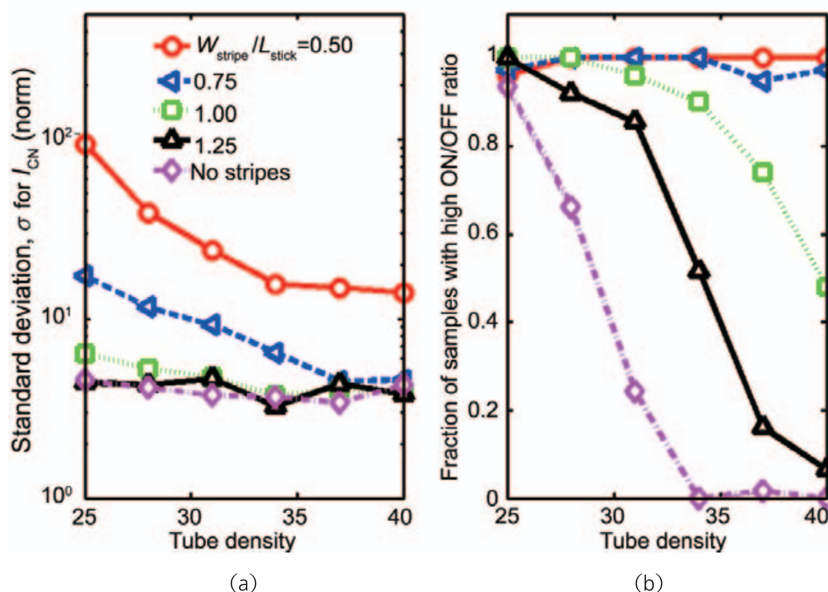

Figure 4 (a) Plot of normalized standard deviation of ON-current (I_{ON}) vs tube density for various W_{stripe}/L_{stick}. Here, L_C = 25 μm. The normalized standard deviation is high for lower density and smaller W_{stripe}/L_{stick}. (b) Fraction of samples with high ON/OFF ratio as a function of tube density for various W_{stripe}/L_{stick}

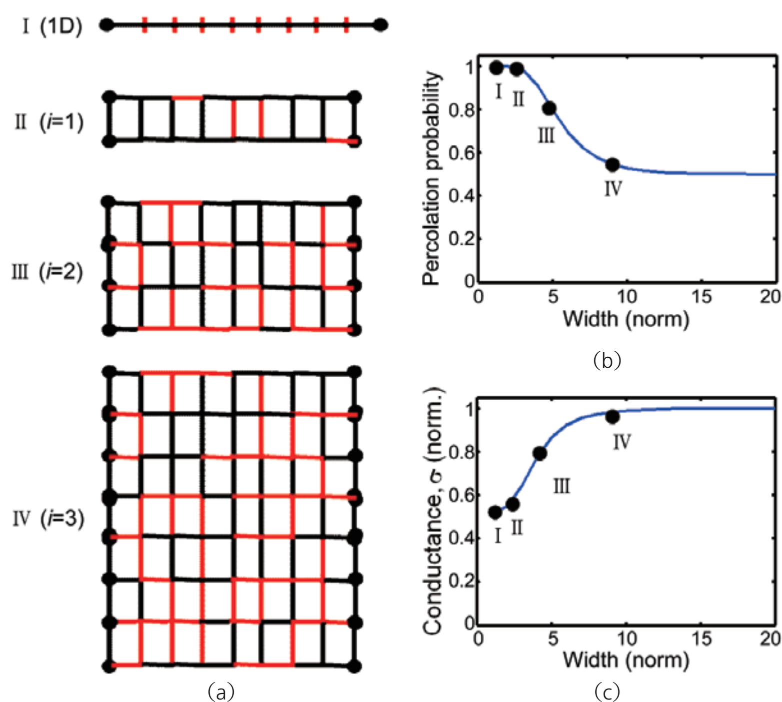

Figure 5 (a) Schematic showing transition of channels from 1-D to 2-D with width *i*. Random sections of the grid are occupied (black) with a probability of 0.5 (bond percolation threshold for an infinite 2-D network). The percolation threshold in finite width samples is defined by the condition that one certain occupation probability of the grid ensures current flow from S/D

$$D_{\mathrm{P},i}={}^{5}_{\mathrm{p},i+1}-5D^{4}_{\mathrm{p},i+1}+2D^{3}_{\mathrm{p},i+1}+2D^{2}_{\mathrm{p},i+1}$$

where $D_{\mathrm{P},j}$ is the percolation threshold of the resistor of width 2^j and length N. Assuming $D_{\mathrm{P},1}\rightarrow 1$ for a quasi-1-D conductor, the solution of the recurrence relationship ($D_{\mathrm{P},1}\rightarrow D_{\mathrm{P},2}\rightarrow D_{\mathrm{P},3}\rightarrow D_{\mathrm{P},4}\cdots\rightarrow D_{\mathrm{P},a}$, etc.) as plotted in Fig. 5(b) shows a dramatic transition in percolation threshold from 1 to 0.5 as width of the resistor (i.e., stripe width) passes through a critical value. Moreover, for a lattice whose elements are filled with probability, $D_{\mathrm{P},i}$ the condition of conductivity, scaling requires that [15]

$$\frac{\sigma_{i+1}}{2\sigma_i}=\frac{1}{D_{\mathrm{P},i}}[D^{5}_{\mathrm{p},i+1}+\frac{23}{3}D^{4}_{\mathrm{p},i+1}(1-D_{p,i+1})+18D^{3}_{\mathrm{p},i+1}(1-D_{\mathrm{p},i+1})^2+4D^{2}_{\mathrm{p},i+1}(1-D_{\mathrm{p},i+1})^3]$$

Here σ_i is the conductance of the network with width 2^i and percolation threshold $D_{\mathrm{P},i}$. The presence of the "2" in the denominator of the left-hand side represents the factor of two renormalizations of the network at successive levels. For very wide transistors, a factor of two scaling of transistor width scales the current by $2\mu/\upsilon\sim 2\times 1.93=3.86$, as expected from the 2-D conductivity exponent [25]. However, as the width of the transistor is reduced, many of the percolation paths are broken and the 2-D conductivity exponent reduces from 1.93 to 1; in other words, current scales linearly with conductor width. This procedure explains how the factor of two reductions in the ON-current due to striping (Figs. 2(a), 3(a), and 5(c)) is a consequence of the finite-size percolation threshold and is not specific to the particular network or simulation model being discussed.

4. Conclusions

In summary, we have provided a theory of a highly effective alternative method called striping to increase the ON/OFF ratio of a CNT NN-TFT without significantly reducing the per-width ON-current. Compared to traditional techniques of increasing ON/OFF ratio like electrical or chemical filtering, the *in situ* method appears scalable and versatile, and appropriate for large scale integrated circuits. Both theory and experiments suggest that if the stripe width is so defined that $W_{\mathrm{stripe}}/L_{\mathrm{stick}}<1$ and $L_{\mathrm{C}}/W_{\mathrm{stripe}}>10$, high ON/OFF ratio and high ON-current are easily ensured. Note that reduction in $W_{\mathrm{stripe}}/L_{\mathrm{stick}}$ significantly below unity may not be acceptable from the point of view of parameter fluctuation (Fig. 4) and may otherwise have to be managed by various fluctuation-resilient circuit techniques. Apart from the numerical simulation and experimental results, our renormalization argument suggests that this technique is really a general approach, fundamentally rooted in the asymmetric percolation threshold of heterogeneous networks.

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References

[1] Cao, Q.; Kim, H. S.; Pimparkar, N.; Kulkarni, J. P.; Wang, C.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **2008**, *454*, 495–500.

[2] Duan, X. F.; Niu, C. M.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. High-performance thin-film transistors using semiconductor nanowires and nanoribbons. *Nature* **2003**, *425*, 274–278.

[3] Novak, J. P.; Lay, M. D.; Perkins, F. K.; Snow, E. S. Macroelectronic applications of carbon nanotube networks. *Solid State Electron*. **2004**, *48*, 1753–1756.

[4] Novak, J. P.; Snow, E. S.; Houser, E. J.; Park, D.; Stepnowski, J. L.; McGill, R. A. Nerve agent detection using networks of single-walled carbon nanotubes. *Appl. Phys. Lett*. **2003**, *83*, 4026–4028.

[5] Snow, E. S.; Novak, J. P.; Campbell, P. M.; Park, D.

Random networks of carbon nanotubes as an electronic material. *Appl. Phys. Lett.* **2003**, *82*, 2145–2147.

[6] Szleifer, I.; Yerushalmi-Rozen, R. Polymers and carbon nanotubes—Dimensionality, interactions and nanotechnology. *Polymer* **2005**, *46*, 7803–7808.

[7] Zhou, Y. X.; Gaur, A.; Hur, S. H.; Kocabas, C.; Meitl, M. A.; Shim, M.; Rogers, J. A. p-channel, n-channel thin film transistors and p–n diodes based on single wall carbon nanotube networks. *Nano Lett*. **2004**, *4*, 2031–2035.

[8] Kumar, S.; Murthy, J. Y.; Alam, M. A. Percolating conduction in finite nanotube networks. *Phys. Rev. Lett*. **2005**, *95/6*, 066802.

[9] Pimparkar, N.; Guo, J.; Alam, M. A. Performance assessment of sub-percolating nanobundle network transistors by an analytical model. *IEDM Tech.Digest* **2005**, *21*, 541–544.

[10] Kang, S. J.; Kocabas, C.; Ozel, T.; Shim, M.; Pimparkar, N.; Alam, M. A.; Rogers, J. A. High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes. *Nat. Nanotechnol*. **2007**, *2*, 230–236.

[11] Cao, Q.; Hur, S. H.; Zhu, Z. T.; Sun, Y.; Wang, C.J.; Meitl, M. A.; Shim, M.; Rogers, J. A. Highly bendable, transparent thin-film transistors that use carbon-nanotube-based conductors and semiconductors with elastomeric dielectrics. *Adv. Mater*. **2006**, *18*, 304.

[12] Collins, P. C.; Arnold, M. S.; Avouris, P. Engineering carbon nanotubes and nanotube circuits using electrical breakdown. *Science* **2001**, *292*, 706–709.

[13] Kumar, S.; Blanchet, G. B.; Hybertsen, M. S.; Murthy, J. Y.; Alam, M. A. Performance of carbon nanotube-dispersed thin-film transistors. *Appl. Phys. Lett*. **2006** ,*89*, 143501.

[14] Datta S. *Quantum Transport: Atom to Transistor*, 2nd ed.; Cambridge University Press: Cambridge, 2005.

[15] Stauffer, D.; Aharony, *A. Introduction to Percolation Theory*; Taylor and Francis: London, 1992.

[16] Haddon, R. C.; Sippel, J.; Rinzler, A. G.; Papadimitrakopoulos, F. Purification and separation of carbon nanotubes. *MRS Bull*. **2004**, *29*, 252–259.

[17] Wang, C.; Cao, Q.; Ozel, T.; Gaur, A.; Rogers, J. A.; Shim, M. Electronically selective chemical functionalization of carbon nanotubes: Correlation between Raman spectral and electrical responses. *J. Am. Chem. Soc*. **2005**, *127*, 11460–11468.

[18] Arnold, M. S.; Stupp, S. I.; Hersam, M. Enrichment of single-walled carbon nanotubes by diameter in density gradients. *Nano Lett*. **2005**, *5*, 713–718.

[19] Seidel, R.; Graham, A. P.; Unger, E.; Duesberg, G. S.; Liebau, M.; Steinhoegl, W.; Kreupl, F.; Hoenlein, W. High-current nanotube transistors. *Nano Lett*. **2004**, *4*, 831–834.

[20] Pimparkar, N.; Guo, J.; Alam, M. A. Performance assessment of subpercolating nanobundle network thin-film transistors by an analytical model. *IEEE T. Electron Dev*. **2007**, *54*, 637–644.

[21] Li, Y. M.; Mann, D.; Rolandi, M.; Kim, W.; Ural, A.; Hung, S.; Javey, A.; Cao, J.; Wang, D. W.; Yenilmez, E.; Wang, Q.; Gibbons, J. F.; Nishi, Y.; Dai, H. J. Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced CVD method. *Nano Lett*. **2004**, *4*, 317–321.

[22] Pimparkar, N.; Kumar, S.; Cao, Q.; Rogers, J. A.; Murthy, J. Y.; Alam, M. A. Current-voltage characteristics of long-channel nanobundle thin-film transistors: A "bottom-up" perspective. *IEEE Electron Dev. L*. **2007**, *28*, 157–160

[23] Pimparkar N.; Kocabas C.; Kang S. J.; Rogers J. A.; Alam M. A. *Electron Dev. Lett*. **2007**, *28*, 593–595.

[24] Kocabas, C.; Pimparkar, N.; Yesilyurt, O.; Alam, M. A.; Rogers, J. A. Experimental and theoretical studies of transport through large scale, partially aligned arrays of single-walled carbon nanotubes in thin film type transistors. *Nano Lett*. **2007**, *7*, 1195–1202.

[25] Seager, C. H.; Pike, G. E. Percolation and conductivity: A computer study. *Phys. Rev. B* **1974**, *10*, 1421.